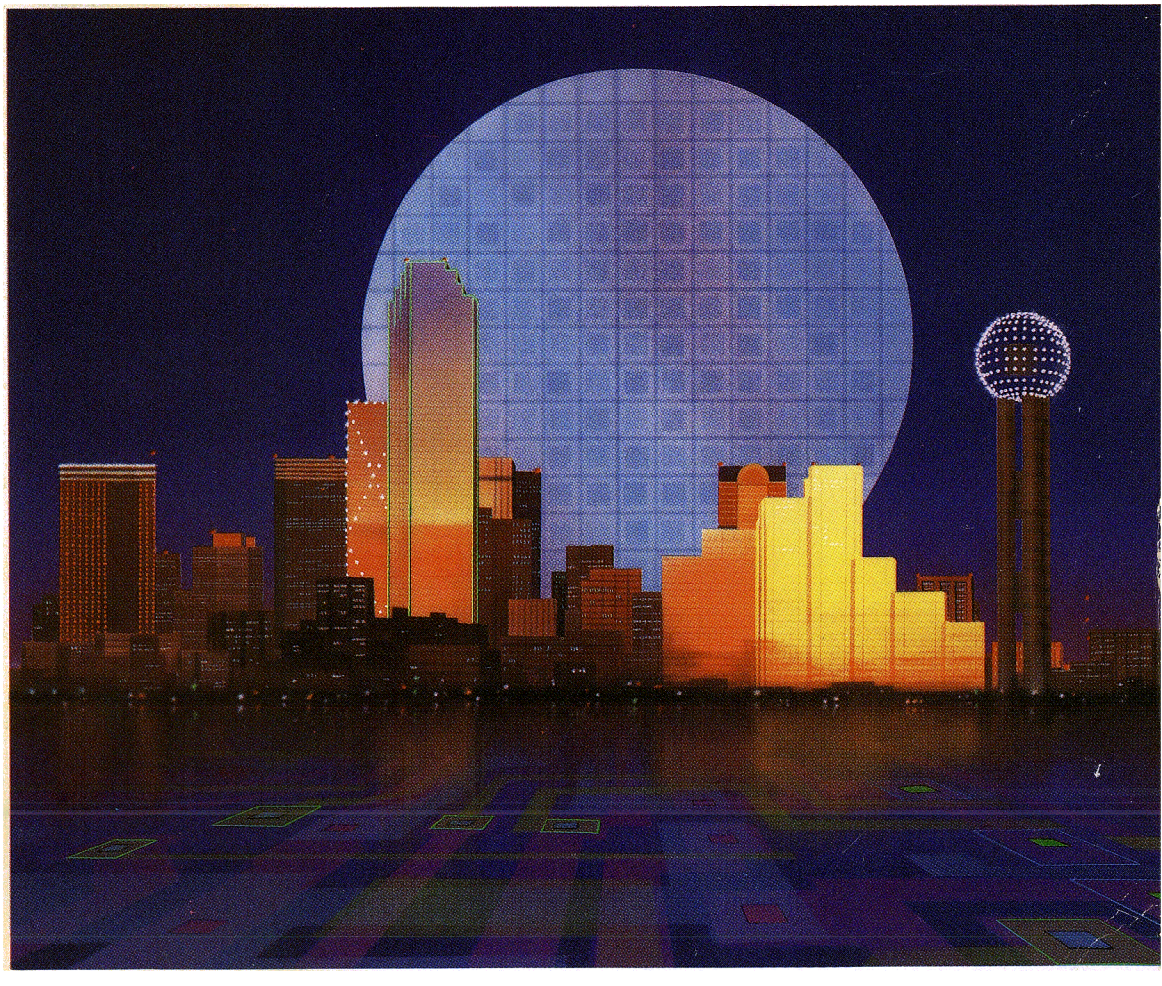
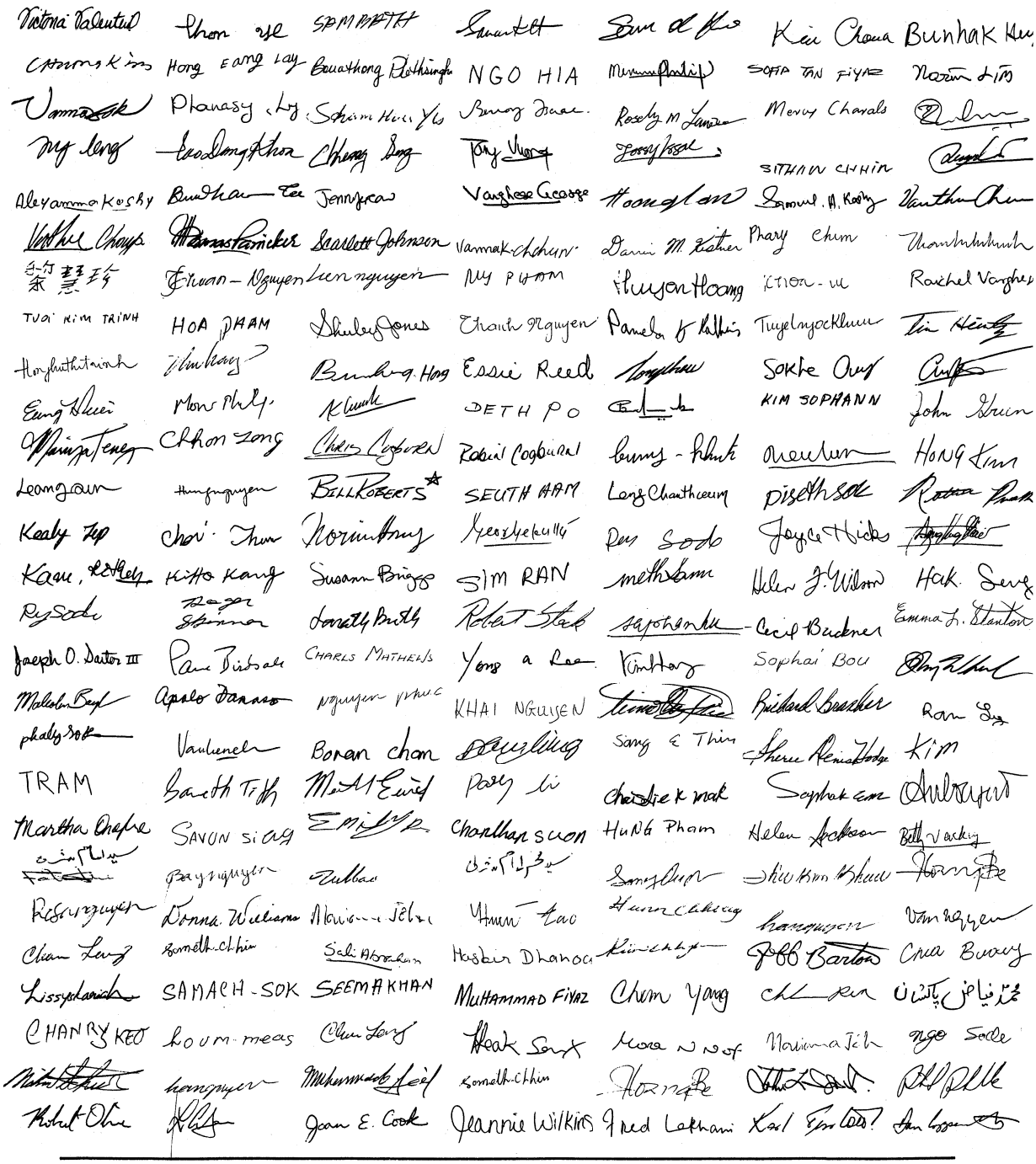
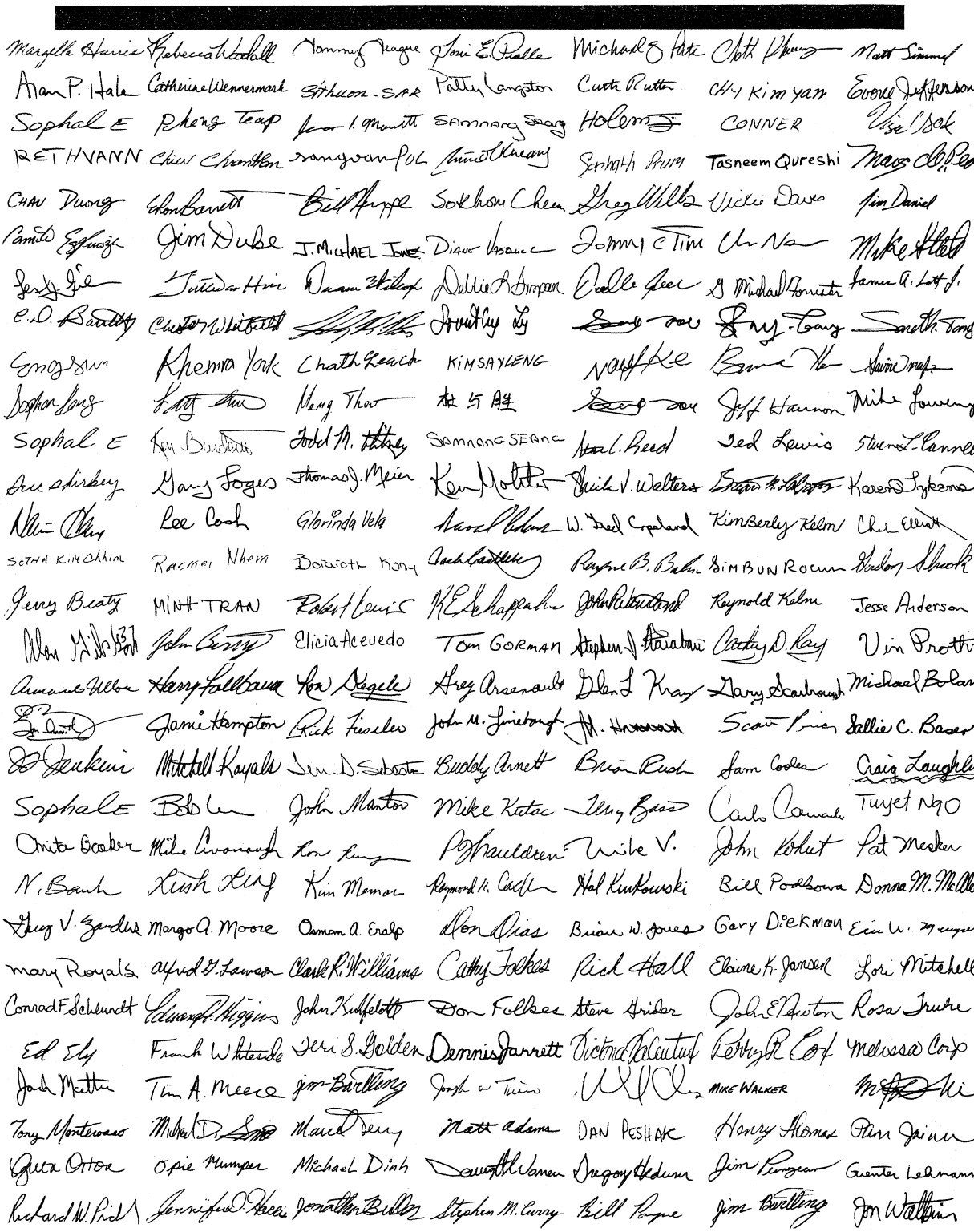
DALLAS SEMICONDUCTOR

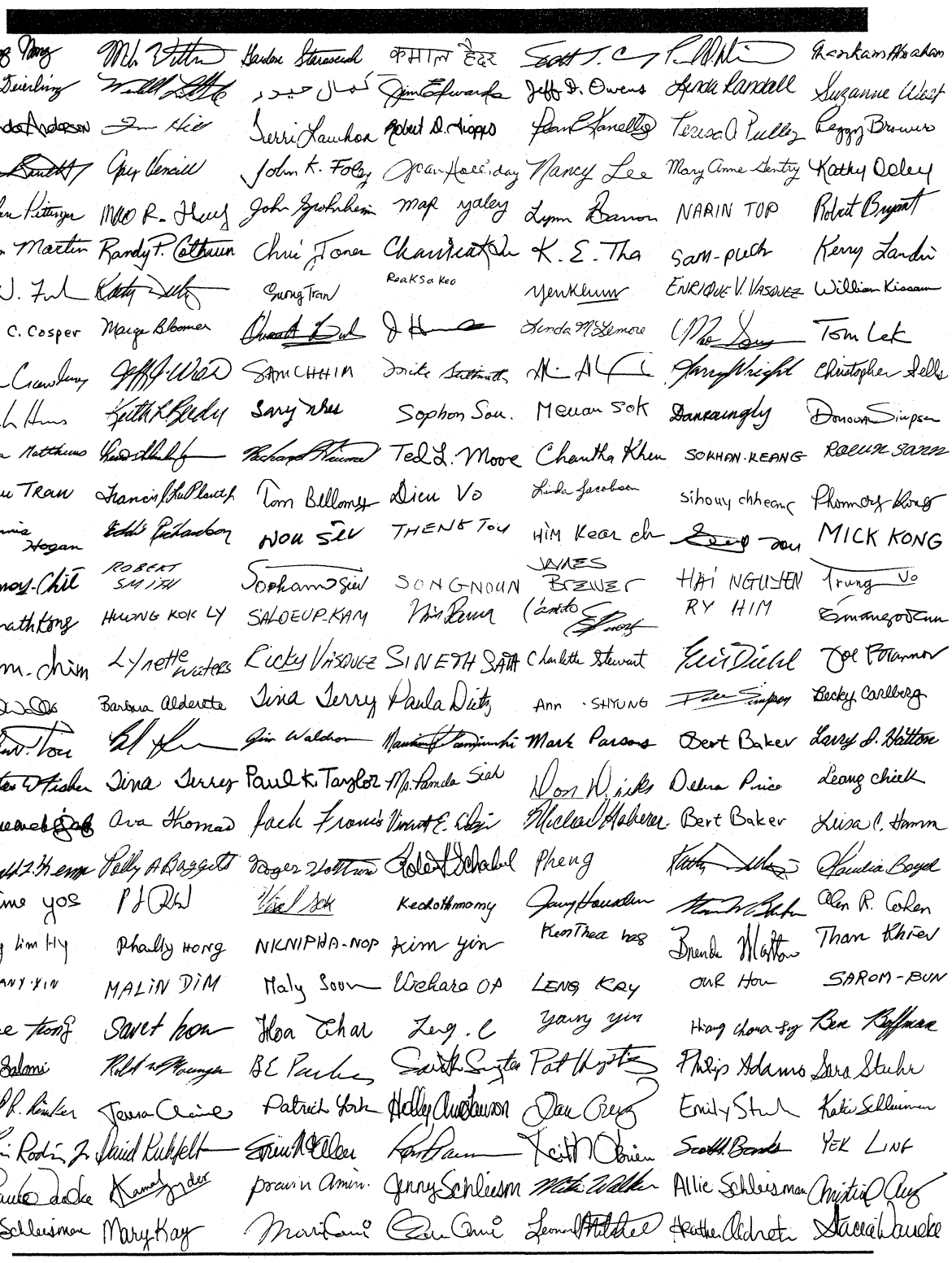
1990-1991
PRODUCT DATA BOOK



Quality Completes Our Innovation







General Information

SELECTION GUIDE

User Insertable Memory

Accessories

Security Products

Integrated Battery Backup

System Extension

SIP Stik™ Prefabs

Accessories

Automatic Identification

Telecommunications

Teleservicing

PRODUCT LIST

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
* These Line Items are the standard versions. Other non-asterisked variations may be available upon special request from the factory with extended lead times.				
*DS0010	SOFTWARE	N/A	DS0010	
*DS1000	14-Pin DIP	-40 to +85	DS1000-xxx	xxx = 025 to 500ns
	14-Pin DIP Sheared NC	-40 to +85	DS1000K-xxx	xxx = 025 to 500ns
*	8-Pin DIP	-40 to +85	DS1000M-xxx	xxx = 025 to 500ns
	14-Pin GULLWING	-40 to +85	DS1000G-xxx	xxx = 025 to 500ns
	8-Pin GULLWING	-40 to +85	DS1000H-xxx	xxx = 025 to 500ns
*	16-Pin SOIC	-40 to +85	DS1000S-xxx	xxx = 025 to 500ns
*DS1005	14-Pin DIP	-40 to +85	DS1005-xxx	xxx = 060 to 250ns
	14-Pin DIP Sheared NC	-40 to +85	DS1005K-xxx	xxx = 060 to 250ns
*	8-Pin DIP	-40 to +85	DS1005M-xxx	xxx = 060 to 250ns
	14-Pin GULLWING	-40 to +85	DS1005G-xxx	xxx = 060 to 250ns
	8-Pin GULLWING	-40 to +85	DS1005H-xxx	xxx = 060 to 250ns
*	16-Pin SOIC	-40 to +85	DS1005S-xxx	xxx = 060 to 250ns
*DS1007	16-Pin DIP	-40 to +85	DS1007-xxx	xxx = 001 to 999
	16-Pin GULLWING	-40 to +85	DS1007G-xxx	xxx = 001 to 999
*	16-Pin SOIC	-40 to +85	DS1007S-xxx	xxx = 001 to 999
*DS1010	14-Pin DIP	-40 to +85	DS1010-xxx	xxx = 050 to 500ns
	14-Pin GULLWING	-40 to +85	DS1010G-xxx	xxx = 050 to 500ns
*	16-Pin SOIC	-40 to +85	DS1010S-xxx	xxx = 050 to 500ns
*DS1012	8-Pin DIP	-40 to +85	DS1012M-xxx	xxx = 001 to 999
	8-Pin GULLWING	-40 to +85	DS1012H-xxx	xxx = 001 to 999
*	8-Pin SOIC	-40 to +85	DS1012S-xxx	xxx = 001 to 999
*DS1013	14-Pin DIP	-40 to +85	DS1013-xxx	xxx = 015 to 150ns
*	8-Pin DIP	-40 to +85	DS1013M-xxx	xxx = 015 to 150ns
	14-Pin GULLWING	-40 to +85	DS1013G-xxx	xxx = 015 to 150ns
	8-Pin GULLWING	-40 to +85	DS1013H-xxx	xxx = 015 to 150ns
*	16-Pin SOIC	-40 to +85	DS1013S-xxx	xxx = 015 to 150ns
DS1020	16-Pin DIP	-40 to +85	DS1020-25	0.25ns Steps
	16-Pin DIP	-40 to +85	DS1020-50	0.50ns Steps
	16-Pin DIP	-40 to +85	DS1020-100	1.00ns Steps
	16-Pin DIP *	-40 to +85	DS1020-200	2.00ns Steps
	16-Pin GULLWING	-40 to +85	DS1020G-25	0.25ns Steps
	16-Pin GULLWING	-40 to +85	DS1020G-50	0.50ns Steps
	16-Pin GULLWING	-40 to +85	DS1020G-100	1.00ns Steps
	16-Pin GULLWING	-40 to +85	DS1020G-200	2.00ns Steps

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1020	16-Pin SOIC	-40 to +85	DS1020S-25	0.25ns Steps
	16-Pin SOIC	-40 to +85	DS1020S-50	0.50ns Steps
	16-Pin SOIC	-40 to +85	DS1020S-100	1.00ns Steps
	16-Pin SOIC	-40 to +85	DS1020S-200	2.00ns Steps
*DS1200	10-Pin DIP	0 to +70	DS1200	
	10-Pin DIP	-40 to +85	DS1200N	
*	16-Pin SOIC	0 to +70	DS1200S	
	16-Pin SOIC	-40 to +85	DS1200SN	
*DS1201		0 to +70	DS1201	
*DS1202	8-Pin DIP	0 to +70	DS1202	
	8-Pin DIP	-40 to +85	DS1202N	
*	16-Pin SOIC	0 to +70	DS1202S	
	16-Pin SOIC	-40 to +85	DS1202SN	
*DS1203S-B1	8-Pin SOIC	0 to +70	DS1203S-B1	
	8-Pin SOIC	-40 to +85	DS1203SN-B1	
*DS1204U		0 to +70	DS1204U-G01	Generic Code #1
*		0 to +70	DS1204U-G02	Generic Code #2
*		0 to +70	DS1204U-G03	Generic Code #3
*		0 to +70	DS1204U-G04	Generic Code #4
*		0 to +70	DS1204U-G05	Generic Code #5
		0 to +70	DS1204U-xxx	xxx = 001 to 999
*		0 to +70	DS1204U-G1C	Generic Code #1 w/cap
*		0 to +70	DS1204U-G2C	Generic Code #2 w/cap
*		0 to +70	DS1204U-G3C	Generic Code #3 w/cap
*		0 to +70	DS1204U-G4C	Generic Code #4 w/cap
*		0 to +70	DS1204U-G5C	Generic Code #5 w/cap
DS1205	16-Pin SOIC	0 to +70	DS1205S	
	16-Pin SOIC	-40 to +85	DS1205SN	
*DS1206	14-Pin DIP	0 to +70	DS1206	
	14-Pin DIP	-40 to +85	DS1206N	
*	16-Pin SOIC	0 to +70	DS1206S	
	16-Pin SOIC	-40 to +85	DS1206SN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS1207		0 to +70	DS1207-G01	Generic Code #1
*		0 to +70	DS1207-G02	Generic Code #2
*		0 to +70	DS1207-G03	Generic Code #3
*		0 to +70	DS1207-G04	Generic Code #4
*		0 to +70	DS1207-G05	Generic Code #5
		0 to +70	DS1207-xxx	xxx = 001 to 999
*		0 to +70	DS1207-G1C	Generic Code #1 w/cap
*		0 to +70	DS1207-G2C	Generic Code #2 w/cap
*		0 to +70	DS1207-G3C	Generic Code #3 w/cap
*		0 to +70	DS1207-G4C	Generic Code #4 w/cap
*		0 to +70	DS1207-G5C	Generic Code #4 w/cap
*DS1209S-B1	16-Pin SOIC	0 to +70	DS1209S-B1	
	16-Pin SOIC	-40 to +85	DS1209SN-B1	
*DS1210	8-Pin DIP	0 to +70	DS1210	
*	8-Pin DIP	-40 to +85	DS1201N	
	8-Pin GULLWING	0 to +70	DS1210G	
	8-Pin GULLWING	-40 to +85	DS1210GN	
*	16-Pin SOIC	0 to +70	DS1210S	
*	16-Pin SOIC	-40 to +85	DS1210SN	
*DS1211	20-Pin DIP	0 to +70	DS1211	
	20-Pin DIP	-40 to +85	DS1211N	
	20-Pin GULLWING	0 to +70	DS1211G	
	20-Pin GULLWING	-40 to +85	DS1211GN	
*	20-Pin SOIC	0 to +70	DS1211S	
	20-Pin SOIC	-40 to +85	DS1211SN	
*DS1212	28-Pin DIP	0 to +70	DS1212	
	28-Pin DIP	-40 to +85	DS1212N	
*	28-Pin PLCC	0 to +70	DS1212Q	
	28-Pin PLCC	-40 to +85	DS1212QN	
*DS1213B	Socket	0 to +70	DS1213B	
*DS1213C	Socket	0 to +70	DS1213C	
*DS1213D	Socket	0 to +70	DS1213D	
*DS1215	16-Pin DIP	0 to +70	DS1215	
*	16-Pin DIP	-40 to +85	DS1215N	
*	16-Pin GULLWING	0 to +70	DS1215G	
	16-Pin GULLWING	-40 to +85	DS1215GN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS1215	16-Pin SOIC	0 to +70	DS1215S	
	16-Pin SOIC	-40 to +85	DS1215SN	
*DS1216B	Socket	0 to +70	DS1216B	
*DS1216C	Socket	0 to +70	DS1216C	
*DS1216D	Socket	0 to +70	DS1216D	
*DS1216E	Socket	0 to +70	DS1216E	
*DS1216F	Socket	0 to +70	DS1216F	
*DS1217A		0 to +70	DS1217A 16K-25	16K Bit Density
*		0 to +70	DS1217A 64K-25	64K Bit Density
*		0 to +70	DS1217A 128K-25	128K Bit Density
*		0 to +70	DS1217A 192K-25	192K Bit Density
*		0 to +70	DS1217A 256K-25	256K Bit Density
*DS1217M		0 to +70	DS1217M 1/2-25	1/2Megabit Density
*		0 to +70	DS1217M 1-15	1 Megabit Density
*		0 to +70	DS1217M 2-25	2 Megabit Density
*		0 to +70	DS1217M 3-25	3 Megabit Density
*		0 to +70	DS1217M 4-25	4 Megabit Density
*DS1220AB/AD		0 to +70	DS1220AB	200ns
*		0 to +70	DS1220AB-150	150ns
		0 to +70	DS1220AB-120	120ns
		0 to +70	DS1220AB-100	100ns
		-40 to +85	DS1220AB-IND	200ns
		-40 to +85	DS1220AB-150-IND	150ns
		-40 to +85	DS1220AB-120-IND	120ns
		-40 to +85	DS1220AB-100-IND	100ns
*		0 to +70	DS1220AD	200ns
*		0 to +70	DS1220AD-150	150ns
		0 to +70	DS1220AD-120	120ns
		0 to +70	DS1220AD-100	100ns
		-40 to +85	DS1220AD- IND	200ns
		-40 to +85	DS1220AD-150-IND	150ns
		-40 to +85	DS1220AD-120-IND	120ns
		-40 to +85	DS1220AD-100-IND	100ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS1220Y		0 to +70	DS1220Y	220ns
*		0 to +70	DS1220Y-150	150ns
		0 to +70	DS1220Y-120	120ns
		0 to +70	DS1220Y-100	100ns
		-40 to +85	DS1220Y-IND	200ns
		-40 to +85	DS1220Y-150-IND	150ns
		-40 to +85	DS1220Y-120-IND	120ns
		-40 to +85	DS1220Y-100-IND	100ns
*DS1221	16-Pin DIP	0 to +70	DS1221	
	16-Pin DIP	-40 to +85	DS1221N	
*	16-Pin SOIC	0 to +70	DS1221S	
	16-Pin SOIC	-40 to +85	DS1221SN	
*DS1222	14-Pin DIP	0 to +85	DS1222	
	14-Pin DIP	-40 to +85	DS1222	
*	16-Pin SOIC	0 to +70	DS1222S	
	16-Pin SOIC	-40 to +85	DS1222SN	
*DS1223		0 to +70	DS1223	
*DS1225AB/AD		0 to +70	DS1225AB	200ns
*		0 to +70	DS1225AB-170	170ns
*		0 to +70	DS1225AB-150	150ns
		0 to +70	DS1225AB-120	120ns
		0 to +70	DS1225AB-100	100ns
		-40 to +85	DS1225AB-IND	200ns
		40 to +85	DS1225AB-170-IND	170ns
		-40 to +85	DS1225AB-150-IND	150ns
		-40 to +85	DS1225AB-120-IND	120ns
		-40 to +85	DS1225AB-100-IND	100ns
*		0 to +70	DS1225AD	200ns
*		0 to +70	DS1225AD-170	170ns
*		0 to +70	DS1225AD-150	150ns
		0 to +70	DS1225AD-120	120ns
		0 to +70	DS1225AD-100	100ns
		-40 to +85	DS1225AD-IND	200ns
		-40 to +85	DS1225AD-170-IND	170ns
		-40 to +85	DS1225AD-150-IND	150ns
		-40 to +85	DS1225AD-120-IND	120ns
		-40 to +85	DS1225AD-100-IND	100ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS1225D/E		0 to +70	DS1225D-100	100ns
*		0 to +70	DS1225D-70	70ns
		-40 to +85	DS1225D-100-IND	100ns
		-40 to +85	DS1225D-70-IND	70ns
*		0 to +70	DS1225E-100	100ns
*		0 to +70	DS1225E-70	70ns
		-40 to +85	DS1225E-100-IND	100ns
		-40 to +85	DS1225E-70-IND	70ns
*DS1225Y		0 to +70	DS1225Y	200ns
*		0 to +70	DS1225Y-170	170ns
*		0 to +70	DS1225Y-150	150ns
		0 to +70	DS1225Y-120	120ns
		0 to +70	DS1225Y-100	100ns
		-40 to +85	DS1225Y-IND	200ns
		-40 to +85	DS1225Y-170-IND	170ns
		-40 to +85	DS1225Y-150-IND	150ns
		-40 to +85	DS1225Y-120-IND	120ns
		-40 to +85	DS1225Y-100-IND	100ns
*DS1227	20-Pin DIP	0 to +70	DS1227	
	20-Pin DIP	-40 to +85	DS1227N	
*	20-Pin SOIC	0 to +70	DS1227S	
	20-Pin SOIC	-40 to +85	DS1227N	
*DS1230Y/AB		0 to +70	DS1230AB	200ns
*		0 to +70	DS1230AB-150	150ns
		0 to +70	DS1230AB-120	120ns
		0 to +70	DS1230AB-100	100ns
		0 to +70	DS1230AB-70	70ns
*		0 to +70	DS1230Y	200ns
*		0 to +70	DS1230Y-150	150ns
		0 to +70	DS1230Y-120	120ns
		0 to +70	DS1230Y-100	100ns
		0 to +70	DS1230Y-70	70ns
*DS1231	8-Pin DIP	0 to +70	DS1231-20	20
*	8-Pin DIP	0 to +70	DS1231-35	35
*	8-Pin DIP	0 to +70	DS1231-50	50
*	8-Pin DIP	-40 to +85	DS1231N-20	20
*	8-Pin DIP	-40 to +85	DS1231N-35	35
*	8-Pin DIP	-40 to +85	DS1231N-50	50
	8-Pin GULLWING	0 to +70	DS1231G-20	20
	8-Pin GULLWING	0 to +70	DS1231G-35	35
	8-Pin GULLWING	0 to +70	DS1231G-50	50

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1231	8-Pin GULLWING	-40 to +85	DS1231GN-20	20
	8-Pin GULLWING	-40 to +85	DS1231GN-35	35
	8-Pin GULLWING	-40 to +85	DS1231GN-50	50
*	16-Pin SOIC	0 to +70	DS1231S-20	20
*	16-Pin SOIC	0 to +70	DS1231S-35	35
*	16-Pin SOIC	0 to +70	DS1231S-50	50
	16-Pin SOIC	-40 to +85	DS1231SN-20	20
	16-Pin SOIC	-40 to +85	DS1231SN-35	35
	16-Pin SOIC	-40 to +85	DS1231SN-50	50
*DS1232	8-Pin DIP	0 to +70	DS1232	
*	8-Pin DIP	-40 to +85	DS1232N	
*	8-Pin GULLWING	0 to +70	DS1232G	
	8-Pin GULLWING	-40 to +85	DS1232GN	
*	16-Pin SOIC	0 to +70	DS1232S	
*	16-Pin SOIC	-40 to +85	DS1232SN	
*DS1234	14-Pin DIP	0 to +70	DS1234	
	14-Pin DIP	-40 to + 85	DS1234N	
*	16-Pin SOIC	0 to +70	DS1234S	
	16-Pin SOIC	-40 to + 85	DS1234SN	
*DS1235Y/AB		0 to +70	DS1235ABW	200ns
*		0 to +70	DS1235ABW-150	150ns
		0 to +70	DS1235ABW-120	120ns
		0 to +70	DS1235ABW-100	100ns
*		0 to +70	DS1235YW	200ns
*		0 to +70	DS1235YW-150	150ns
		0 to +70	DS1235YW-120	120ns
		0 to +70	DS1235YW-100	100ns
*DS1236	16-Pin DIP	0 to +70	DS1236	10% Monitor
	16-Pin DIP	0 to +70	DS1236-5	5% Monitor
	16-Pin DIP	-40 to +85	DS1236N	10% Monitor
	16-Pin DIP	-40 to +85	DS1236N-5	5% Monitor
*	16-Pin SOIC	0 to +70	DS1236S	10% Monitor
	16-Pin SOIC	0 to +70	DS1236S-5	5% Monitor
	16-Pin SOIC	-40 to +85	DS1236SN	10% Monitor
	16-Pin SOIC	-40 to +85	DS1236SN-5	5% Monitor
*DS1237	16-Pin DIP	0 to +70	DS1237-x	x = 1 to 8
	16-Pin DIP	-40 to +85	DS1237N-x	x = 1 to 8
*	16-Pin SOIC	0 to +70	DS1237S-x	x = 1 to 8
	16-Pin SOIC	-40 to +85	DS1237SN-x	x = 1 to 8

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS1239	16-Pin DIP	0 to +70	DS1239	10% Monitor
	16-Pin DIP	0 to +70	DS1239-5	5% Monitor
	16-Pin DIP	-40 to +85	DS1239N	10% Monitor
	16-Pin DIP	-40 to +85	DS1239N-5	5% Monitor
*	16-Pin SOIC	0 to +70	DS1239S	10% Monitor
	16-Pin SOIC	0 to +70	DS1239S-5	5% Monitor
	16-Pin SOIC	-40 to +85	DS1239SN	10% Monitor
	16-Pin SOIC	-40 to +85	DS1239SN-5	5% Monitor
*DS1243Y		0 to +70	DS1243Y	200ns
*DS1244Y		0 to +70	DS1244Y	200ns
*DS1245Y/AB		0 to +70	DS1245AB-120	120ns
*		0 to +70	DS1245AB-100	100ns
*		0 to +70	DS1245Y-120	120ns
*		0 to +70	DS1245Y-100	100ns
*DS1250		0 to +70	DS1250	
*DS1253			DS1253	
*DS1255C	Kit	N/A	DS1255C	
*DS1255U			DS1255U	
*DS1259	16-Pin DIP	0 to +70	DS1259	
	16-Pin DIP	-40 to +85	DS1259N	
*	16-Pin SOIC	0 to +70	DS1259S	
	16-Pin SOIC	-40 to +85	DS1259SN	
DS1260		0 to +70	DS1260-25	250 mAHr
*		0 to +70	DS1260-50	500 mAHr
*		0 to +70	DS1260-100	1000 mAHr
*DS1262	28-Pin DIP	0 to +70	DS1262	
	28-Pin DIP	-40 to +85	DS1262N	
*	28-PinSOIC	0 to +70	DS1262S	
	28-Pin SOIC	-40 to +85	DS1262SN	
*DS1267	14-Pin DIP	0 to +70	DS1267-10	10K ohms
*	14-Pin DIP	0 to +70	DS1267-50	50K ohms
*	14-Pin DIP	0 to +70	DS1267-100	100K ohms

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1267	14-Pin DIP	-40 to +85	DS1267N-10	10K ohms
	14-Pin DIP	-40 to +85	DS1267N-50	50K ohms
	14-Pin DIP	-40 to +85	DS1267N-100	100K ohms
*	16-Pin SOIC	0 to +70	DS1267S-10	10K ohms
*	16-Pin SOIC	0 to +70	DS1267S-50	50K ohms
*	16-Pin SOIC	0 to +70	DS1267S-100	100K ohms
	16-Pin SOIC	-40 to +85	DS1267SN-10	10K ohms
	16-Pin SOIC	-40 to +85	DS1267SN-50	50K ohms
	16-Pin SOIC	-40 to +85	DS1267SN-100	100K ohms
*DS1275	8-Pin DIP	0 to +70	DS1275	
	8-Pin DIP	-40 to +85	DS1275N	
*	8-Pin SOIC	0 to +70	DS1275S	
	8-Pin SOIC	-40 to +85	DS1275SN	
*DS1277	24-Pin DIP	0 to +70	DS1277	
	24-Pin DIP	-40 to +85	DS1277N	
*DS1280	44-Pin Flat Pack	0 to +70	DS1280FP-44	
	44-Pin Flat Pack	-40 to +85	DS1280FPN-44	
*	80-Pin Flat Pack	0 to +70	DS1280FP-80	
	80-Pin Flat Pack	-40 to +85	DS1280FPN-80	
	68-Pin PLCC	0 to +70	DS1280Q-68	
	68-Pin PLCC	-40 to +85	DS1280QN-68	
*DS1281	10-Pin DIP	-0 to + 70	DS1281	
	10-Pin DIP	-40 to +85	DS1281N	
*	16-Pin SOIC	-0 to + 70	DS1281S	
	16-Pin SOIC	-40 to +85	DS1281SN	
*DS1283	28-Pin DIP	0 to +70	DS1283	
	28-Pin DIP	-40 to +85	DS1283N	
*	28-Pin SOIC	0 to +70	DS1283S	
	28-Pin SOIC	-40 to +85	DS1283SN	
*DS1284	28-Pin DIP	0 to +70	DS1284	
	28-Pin DIP	-40 to +85	DS1284N	
*	28-Pin PLCC	0 to +70	DS1284Q	
	28-Pin PLCC	-40 to +85	DS1284QN	
*DS1285	24-Pin DIP	0 to +70	DS1285	
	24-Pin DIP	-40 to +85	DS1285N	
*	28-Pin PLCC	0 to +70	DS1285Q	
	28-Pin PLCC	-40 to +85	DS1285QN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS1286		0 to +70	DS1286	
*DS1287		0 to +70	DS1287	
*DS1287A		0 to +70	DS1287A	
*DS129X		0 to +70	DS1290	
*	16-Pin DIP	0 to +70	DS1291	
	16-Pin DIP	-40 to +85	DS1291N	
*		0 to +70	DS1292	
*	24-Pin DIP	0 to +70	DS1293	
	24-Pin DIP	-40 to +85	DS1293N	
*DS1336	16-Pin DIP	0 to +70	DS1336	
	16-Pin DIP	-40 to +85	DS1336N	
*	16-Pin SOIC	0 to +70	DS1336S	
	16-Pin SOIC	-40 to +85	DS1336SN	
*DS1360	20-Pin DIP	0 to +70	DS1360	
	20-Pin DIP	-40 to +85	DS1360N	
*	20-Pin SOIC	0 to +70	DS1360S	
	20-Pin SOIC	-40 to +85	DS1360SN	
*DS1385	24-Pin DIP	0 to +70	DS1385	
	24-Pin DIP	-40 to +85	DS1385N	
*	28-Pin SOIC	0 to +70	DS1385S	
	28-Pin SOIC	-40 to +85	DS1385SN	
*DS1386		0 to +70	DS1386-8	8K x 8
		0 to +70	DS1386-32	32K x 8
* DS1387		0 to +70	DS1387	
* DS139X	28-Pin DIP	0 to +70	DS1395	
	28-Pin DIP	-40 to +85	DS1395N	
*	28-Pin SOIC	0 to +70	DS1395S	
	28-Pin SOIC	-40 to +85	DS1395SN	
*		0 to +70	DS1397	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS199X		-20 to +50	DS1990	Non-Stick
		-20 to +50	DS1990R	Removable Self-Stick
		-20 to +50	DS1990P	Permanent Self-Stick
*		-20 to +50	DS1991	Non-Stick; 2 Years
		-20 to +50	DS1991L	Non-Stick; 5 years
		-20 to +50	DS1991R	Removable Self-Stick; 5 Years
		-20 to +50	DS1991LR	Removable Self-Stick; 5 Years
		-20 to +50	DS1991P	Permanent Self-Stick; 2 Years
		-20 to +50	DS1991LP	Permanent Self-Stick; 5 Years
*		-20 to +50	DS1992	Non-Stick; 2 Years
		-20 to +50	DS1992L	Non-Stick; 5 years
		-20 to +50	DS1992R	Removable Self-Stick; 5 Years
		-20 to +50	DS1992LR	Removable Self-Stick; 5 Years
		-20 to +50	DS1992P	Permanent Self-Stick; 2 Years
		-20 to +50	DS1992LP	Permanent Self-Stick; 5 Years
*DS2009	28-Pin DIP	0 to +70	DS2009-35	35ns
*	28-Pin DIP	0 to +70	DS2009-50	50ns
*	28-Pin DIP	0 to +70	DS2009-65	65ns
*	28-Pin DIP	0 to +70	DS2009-80	80ns
*	28-Pin DIP	0 to +70	DS2009	120ns
*	28-Pin DIP	-40 to +85	DS2009N-35	35ns
*	28-Pin DIP	-40 to +85	DS2009N-50	50ns
*	28-Pin DIP	-40 to +85	DS2009N-65	65ns
*	28-Pin DIP	-40 to +85	DS2009N-80	80ns
*	28-Pin DIP	-40 to +85	DS2009N	I20ns
*	32-Pin PLCC	0 to +70	DS2009R-35	35ns
*	32-Pin PLCC	0 to +70	DS2009R-50	50ns
*	32-Pin PLCC	0 to +70	DS2009R-65	65ns
*	32-Pin PLCC	0 to +70	DS2009R-80	80ns
*	32-Pin PLCC	0 to +70	DS2009R	120ns
*	32-Pin PLCC	-40 to +85	DS2009RN-35	35ns
*	32-Pin PLCC	-40 to +85	DS2009RN-50	50ns
*	32-Pin PLCC	-40 to +85	DS2009RN-65	65ns
*	32-Pin PLCC	-40 to +85	DS2009RN-80	80ns
*	32-Pin PLCC	-40 to +85	DS2009RN	120ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS2010	28-Pin DIP	0 to +70	DS2010-50	50ns
*	28-Pin DIP	0 to +70	DS2010-65	65ns
*	28-Pin DIP	0 to +70	DS2010-80	80ns
*	28-Pin DIP	0 to +70	DS2010	120ns
*	28-Pin DIP	-40 to +85	DS2010N-50	50ns
*	28-Pin DIP	-40 to +85	DS2010N-65	65ns
*	28-Pin DIP	-40 to +85	DS2010N-80	80ns
*	28-Pin DIP	-40 to +85	DS2010N	120ns
*	32-Pin PLCC	0 to +70	DS2010R-50	50ns
*	32-Pin PLCC	0 to +70	DS2010R-65	65ns
*	32-Pin PLCC	0 to +70	DS2010R-80	80ns
*	32-Pin PLCC	0 to +70	DS2010R	120ns
*	32-Pin PLCC	-40 to +85	DS2010RN-50	50ns
*	32-Pin PLCC	-40 to +85	DS2010RN-65	65ns
*	32-Pin PLCC	-40 to +85	DS2010RN-80	80ns
*	32-Pin PLCC	-40 to +85	DS2010RN	120ns
* DS2011	28-Pin DIP	0 to +70	DS2011-50	50ns
*	28-Pin DIP	0 to +70	DS2011-65	65ns
*	28-Pin DIP	0 to +70	DS2011-80	80ns
*	28-Pin DIP	0 to +70	DS2011	120ns
*	28-Pin DIP	-40 to +85	DS2011N-50	50ns
*	28-Pin DIP	-40 to +85	DS2011N-65	65ns
*	28-Pin DIP	-40 to +85	DS2011N-80	80ns
*	28-Pin DIP	-40 to +85	DS2011N	120ns
*	32-Pin PLCC	0 to +70	DS2011R-50	50ns
*	32-Pin PLCC	0 to +70	DS2011R-65	65ns
*	32-Pin PLCC	0 to +70	DS2011R-80	80ns
*	32-Pin PLCC	0 to +70	DS2011R	120ns
*	32-Pin PLCC	-40 to +85	DS2011RN-50	50ns
*	32-Pin PLCC	-40 to +85	DS2011RN-65	65ns
*	32-Pin PLCC	-40 to +85	DS2011RN-80	80ns
*	32-Pin PLCC	-40 to +85	DS2011RN	120ns
* DS2012	28-Pin DIP	0 to +70	DS2012-50	50ns
*	28-Pin DIP	0 to +70	DS2012-65	65ns
*	28-Pin DIP	0 to +70	DS2012-80	80ns
*	28-Pin DIP	0 to +70	DS2012	120ns
*	28-Pin DIP	-40 to +70	DS2012N-50	50ns
*	28-Pin DIP	-40 to +85	DS2012N-65	65ns
*	28-Pin DIP	-40 to +85	DS2012N-80	80ns
*	28-Pin DIP	-40 to +85	DS2012N	120ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS2012	32-Pin PLCC	0 to +70	DS2012R-50	50ns
*	32-Pin PLCC	0 to +70	DS2012R-65	65ns
*	32-Pin PLCC	0 to +70	DS2012R-80	80ns
*	32-Pin PLCC	0 to +70	DS2012R	120ns
*	32-Pin PLCC	-40 to +85	DS2012RN-50	50ns
*	32-Pin PLCC	-40 to +85	DS2012RN-65	65ns
*	32-Pin PLCC	-40 to +85	DS2012RN-80	80ns
*	32-Pin PLCC	-40 to +85	DS2012RN	120ns
*DS2013	28-Pin DIP	0 to +70	DS2013-50	50ns
*	28-Pin DIP	0 to +70	DS2013-65	65ns
*	28-Pin DIP	0 to +70	DS2013-80	80ns
*	28-Pin DIP	0 to +70	DS2013	120ns
*	28-Pin DIP	-40 to +85	DS2013N-50	50ns
*	28-Pin DIP	-40 to +85	DS2013N-65	65ns
*	28-Pin DIP	-40 to +85	DS2013N-80	80ns
*	28-Pin DIP	-40 to +85	DS2013N	120ns
* DS2015	18-Pin DIP	0 to +70	DS2015	
	18-Pin DIP	-40 to +85	DS2015N	
* DS2130	28-Pin DIP	0 to +70	DS2130	
	28-Pin DIP	-40 to +85	DS2130N	
*	28-Pin PLCC	0 to +70	DS2130Q	
	28-Pin PLCC	-40 to +85	DS2130QN	
* DS2157/8		0 to +70	DS2157	
*		0 to +70	DS2158	
* DS2160	24-Pin DIP	0 to +70	DS2160	
	24-Pin DIP	-40 to +85	DS2160N	
*	28-Pin PLCC	0 to +70	DS2160Q	
	28-Pin PLCC	-40 to +85	DS2160QN	
* DS2165	24-Pin DIP	0 to +70	DS2165	
	24-Pin DIP	-40 to +85	DS2165N	
*	28-Pin PLCC	0 to +70	DS2165Q	
	28-Pin PLCC	-40 to +85	DS2165QN	
* DS2167K	Kit	N/A	DS2167K	
* DS2167/8	24-Pin DIP	0 to +70	DS2167	
	24-Pin DIP	-40 to +85	DS2167N	
*	28-Pin PLCC	0 to +70	DS2167Q	
	28-Pin PLCC	-40 to +85	DS2167QN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS2167/8	24-Pin DIP	0 to +70	DS2168	
	24-Pin DIP	-40 to +85	DS2168N	
*	28-Pin PLCC	0 to +70	DS2168Q	
	28-Pin PLCC	-40 to +85	DS2168QN	
*DS2175	16-Pin DIP	0 to +70	DS2175	
	16-Pin DIP	-40 to +85	DS2175N	
*	16-Pin SOIC	0 to +70	DS2175S	
	16-Pin SOIC	-40 to +85	DS2175SN	
*DS2176	24-Pin DIP	0 to +70	DS2176	
	24-Pin DIP	-40 to +85	DS2176N	
*	28-Pin PLCC	0 to +70	DS2176Q	
	28-Pin PLCC	-40 to +85	DS2176QN	
*DS2180A	40-Pin DIP	0 to +70	DS2180A	
	40-Pin DIP	-40 to +85	DS2180AN	
*	44-Pin PLCC	0 to +70	DS2180AQ	
	44-Pin PLCC	-40 to +85	DS2180AQN	
*DS2180K	Kit	N/A	DS2180K	
*DS2181	40-Pin DIP	0 to +70	DS2181	
	40-Pin DIP	-40 to +85	DS2181N	
*	44-Pin PLCC	0 to +70	DS2181Q	
	44-Pin PLCC	-40 to +85	DS2181QN	
*DS2182	28-Pin DIP	0 to +70	DS2182	
	28-Pin DIP	-40 to +85	DS2182N	
*	28-Pin PLCC	0 to +70	DS2182Q	
	28-Pin PLCC	-40 to +85	DS2182QN	
*DS2186	20-Pin DIP	0 to +70	DS2186	
	20-Pin DIP	-40 to +85	DS2186N	
*	20-Pin SOIC	0 to +70	DS2186S	
	20-Pin SOIC	-40 to +85	DS2186N	
*DS2187	18-Pin DIP	0 to +70	DS2187	
	18-Pin DIP	-40 to +85	DS2187N	
*	20-Pin SOIC	0 to +70	DS2187S	
	20-Pin SOIC	-40 to +85	DS2187SN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS2188	16-Pin DIP	0 to +70	DS2188	
	16-Pin DIP	-40 to +85	DS2188N	
*	16-Pin SOIC	0 to +70	DS2188S	
	16-Pin SOIC	-40 to +85	DS2188SN	
*DS2190-003		0 to +70	DS2190-003	
* DS2190DK	Kit	N/A	DS2190DK	
*DS2212	STIK	0 to +70	DS2212-120	120ns
	STIK	0 to +70	DS2212- 80	80ns
	STIK	0 to +70	DS2212- 65	65ns
*DS2217	STIK	0 to +70	DS2217	200ns
	STIK	0 to +70	DS2217-150	150ns
	STIK	0 to +70	DS2217-120	120ns
*DS2219	STIK	0 to +70	DS2219-150	150ns
	STIK	0 to +70	DS2219-120	120ns
*DS222X	TO92	0 to +70	DS2223	
	TO92	-40 to +85	DS2223N	
	TO92 SMT	0 to + 70	DS2223S	
	TO92 SMT	-40 to +85	DS2223N	
*	TO92	0 to +70	DS2224	
	TO92	-40 to +85	DS2224N	
	TO92 SMT	0 to +70	DS2224S	
	TO92 SMT	-40 to +85	DS2224SN	
*DS2227	STIK	0 to +70	DS2227-120	120ns
	STIK	0 to +70	DS2227-100	100ns
	STIK	0 to +70	DS2227-70	70ns
	STIK	0 to +70	DS2227-55	55ns
DS2230	STIK	0 to +70	DS2230-32	32K RAM, 120ns
	STIK	0 to +70	DS2230-64	64K RAM, 120ns
	STIK	0 to +70	DS2230T-32	32K RAM, 120ns
*	STIK	0 to +70	DS2230T-64	64K RAM, 120ns
*DS2244T	STIK	0 to +70	DS2244T-24	2400bps
	STIK	0 to +70	DS2244T-12U	1200bps-US only
*DS2245	STIK	0 to +70	DS2245-24	2400bps
	STIK	0 to +70	DS2245-12	1200bps
	STIK	0 to +70	DS2245-12U	1200bps-US only

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS2249	STIK	0 to +70	DS2249	
*DS2249PH	STIK	0 to +70	DS2249PH	
*DS2250	STIK	0 to +70	DS2250 8-8	8K RAM; 8 MHz
	STIK	0 to +70	DS2250 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2250 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2250 32-8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2250 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2250 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2250 64-8	64K RAM; 8 MHz
	STIK	0 to +70	DS2250 64-12	64K RAM; 12 MHz
	STIK	0 to +70	DS2250 64-16	64K RAM; 16 MHz
DS2250T	STIK	0 to +70	DS2250T 8-8	8K RAM; 8 MHz
	STIK	0 to +70	DS2250T 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2250T 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2250T 32-8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2250T 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2250T 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2250T 64-8	64K RAM; 8 MHz
	STIK	0 to +70	DS2250T 64-12	64K RAM; 12 MHz
*	STIK	0 to +70	DS2250T 64-16	64K RAM; 16 MHz
*DS2251	STIK	0 to +70	DS2251 8-8	8K RAM; 8 MHz
	STIK	0 to +70	DS2251 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2251 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2251 32-8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2251 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2251 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2251 64-8	64K RAM; 8 MHz
	STIK	0 to +70	DS2251 64-12	64K RAM; 12 MHz
	STIK	0 to +70	DS2251 64-16	64K RAM; 16 MHz
	STIK	0 to +70	DS2251 128-8	128K RAM; 8 MHz
	STIK	0 to +70	DS2251 128-12	128K RAM; 12 MHz
	STIK	0 to +70	DS2251 128-16	128K RAM; 16 MHz
	STIK	0 to +70	DS2251T 8-8	8K RAM; 8 MHz
	STIK	0 to +70	DS2251T 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2251T 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2251T 32-8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2251T 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2251T 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2251T 64-8	64K RAM; 8 MHz

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS2251	STIK	0 to +70	DS2251T 64-12	64K RAM; 12 MHz
*	STIK	0 to +70	DS2251T 64-16	64K RAM; 16 MHz
	STIK	0 to +70	DS2251T 128- 8	128K RAM; 8 MHz
	STIK	0 to +70	DS2251T 128-12	128K RAM; 12 MHz
*	STIK	0 to +70	DS2251T 128-16	128K RAM; 16 MHz
*DS2252	STIK	0 to +70	DS2252 8- 8	8K RAM; 8 MHz
	STIK	0 to +70	DS2252 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2252 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2252 32- 8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2252 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2252 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2252 64- 8	64K RAM; 8 MHz
	STIK	0 to +70	DS2252 64-12	64K RAM; 12 MHz
	STIK	0 to +70	DS2252 64-16	64K RAM; 16 MHz
	STIK	0 to +70	DS2252 128- 8	128K RAM; 8 MHz
	STIK	0 to +70	DS2252 128-12	128K RAM; 12 MHz
	STIK	0 to +70	DS2252 128-16	128K RAM: 16 MHz
	STIK	0 to +70	DS2252T 8- 8	8K RAM; 8 MHz
	STIK	0 to +70	DS2252T 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2252T 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2252T 32- 8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2252T 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2252T 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2252T 64- 8	64K RAM; 8 MHz
*	STIK	0 to +70	DS2252T 64-12	64K RAM; 12 MHz
	STIK	0 to +70	DS2252T 64-16	64K RAM; 16 MHz
	STIK	0 to +70	DS2252T 128- 8	128K RAM; 8 MHz
	STIK	0 to +70	DS2252T 128-12	128K RAM; 12 MHz
*	STIK	0 to +70	DS2252T 128-16	128K RAM; 16 MHz
DS2255	STIK	0 to +70	DS2255-10	10 Bit Resolution
*	STIK	0 to +70	DS2255-12	12 Bit Resolution
*DS2256	STIK	0 to +70	DS2256 8- 8	8K RAM; 8 MHz
	STIK	0 to +70	DS2256 8-12	8K RAM; 12 MHz
	STIK	0 to +70	DS2256 8-16	8K RAM; 16 MHz
	STIK	0 to +70	DS2256 32- 8	32K RAM; 8 MHz
*	STIK	0 to +70	DS2256 32-12	32K RAM; 12 MHz
	STIK	0 to +70	DS2256 32-16	32K RAM; 16 MHz
	STIK	0 to +70	DS2256 64- 8	64K RAM; 8 MHz
*	STIK	0 to +70	DS2256 64-12	64K RAM; 12 MHz
	STIK	0 to +70	DS2256 64-16	64K RAM; 16 MHz
	STIK	0 to +70	DS2256 128- 8	128K RAM; 8 MHz

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2256	STIK	0 to +70	DS2256 128-12	128K RAM; 12 MHz
*	STIK	0 to +70	DS2256 128-16	128K RAM; 16 MHz
* DS2262	STIK	0 to +70	DS2262- 4	4M x 1
	STIK	0 to +70	DS2262- 8	8M x 1
	STIK	0 to +70	DS2262-16	16M x 1
	STIK	0 to +70	DS2262-32	32M x 1
*DS2264/8	STIK	0 to +70	DS2264	
	STIK	0 to +70	DS2268	
*DS2267	STIK	0 to +50	DS2267	
*DS2270/E	STIK	0 to +70	DS2270	With Memory
	STIK	0 to +70	DS2270E	W/O Memory
*DS2280/1	STIK	0 to +70	DS2280	
	STIK	0 to +70	DS2281-75	75 ohm
	STIK	0 to +70	DS2281-120	120 ohm
*DS2280DK	Kit	N/A	DS2280DK	
DS2282	STIK	0 to +70	DS2282	
DS2283	STIK	0 to + 70	DS2283	
*DS2286	STIK	0 to +70	DS2286- 8	8K x 8
DS2287	STIK	0 to +70	DS2287- 8	8K x 8
*	STIK	0 to +70	DS2287-32	32K x 8
*DS2290	STIK	0 to +70	DS2290	
*DS2291	STIK	0 to +70	DS2291	
DS2301	STIK	0 to +70	DS2301V 8	8K RAM; 1.0 MHz
	STIK	0 to +70	DS2301V 8B	8K RAM; 2.0 MHz
	STIK	0 to +70	DS2301V 32	32K RAM; 1.0 MHz
*	STIK	0 to +70	DS2301V 32B	32K RAM; 2.0 MHz
	STIK	0 to +70	DS2301VT 8	8K RAM; 1.0 MHz
	STIK	0 to +70	DS2301VT 8B	8K RAM; 2.0 MHz
	STIK	0 to +70	DS2301VT 32	32K RAM; 1.0 MHz
*	STIK	0 to +70	DS2301VT 32B	32K RAM; 2.0 MHz
*	STIK	0 to +70	DS2301Y 8	8K RAM; 1.0 MHz

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2301	STIK	0 to +70	DS2301Y 8B	8K RAM; 2.0 MHz
	STIK	0 to +70	DS2301Y 32	32K RAM; 1.0 MHz
	STIK	0 to +70	DS2301Y 32B	32K RAM; 2.0 MHz
	STIK	0 to +70	DS2301Y 64	64K RAM; 1.0 MHz
	STIK	0 to +70	DS2301Y 64B	64K RAM; 2.0 MHz
	STIK	0 to +70	DS2301YT 8	8K RAM; 1.0 MHz
	STIK	0 to +70	DS2301YT 8B	8K RAM; 2.0 MHz
	STIK	0 to +70	DS2301YT 32	32K RAM; 1.0 MHz
*	STIK	0 to +70	DS2301YT 32B	32K RAM; 2.0 MHz
	STIK	0 to +70	DS2301YT 64	64K RAM; 1.0 MHz
*	STIK	0 to +70	DS2301YT 64B	64K RAM; 2.0 MHz
*DS2340	STIK	0 to +70	DS2340 16A	16K RAM; 8 MHz
	STIK	0 to +70	DS2340 16B	16K RAM; 10 MHz
*	STIK	0 to +70	DS2340 64A	64K RAM; 8 MHz
	STIK	0 to +70	DS2340 64B	64K RAM; 10 MHz
	STIK	0 to +70	DS2340 160A	160K RAM; 8 MHz
	STIK	0 to +70	DS2340 160B	160K RAM; 10 MHz
	STIK	0 to +70	DS2340 256A	256K RAM; 8 MHz
	STIK	0 to +70	DS2340 256B	256K RAM; 10 MHz
	STIK	0 to +70	DS2340T 16A	16K RAM; 8 MHz
	STIK	0 to +70	DS2340T 16B	6K RAM; 10 MHz
*	STIK	0 to +70	DS2340T 64B	64K RAM; 10 MHz
	STIK	0 to +70	DS2340T 160A	160K RAM; 8 MHz
	STIK	0 to +70	DS2340T 160B	160K RAM; 10 MHz
	STIK	0 to +70	DS2340T 256A	256K RAM; 8 MHz
*	STIK	0 to +70	DS2340T 256B	256K RAM; 10 MHz
*DS2400	TO92	0 to +70	DS2400	
	TO92	-40 to +85	DS2400N	
	TO92 SMT	0 to +70	DS2400S	
	TO92 SMT	-40 to +85	DS2400SN	
*DS5000		0 to +70	DS5000 8- 8	8K RAM; 8 MHz
		0 to +70	DS5000 8-12	8K RAM; 12 MHz
		0 to +70	DS5000 8-16	8K RAM; 16 MHz
		0 to +70	DS5000 32- 8	32K RAM; 8 MHz
*		0 to +70	DS5000 32-12	32K RAM; 12 MHz
		0 to +70	DS5000 32-16	32K RAM; 16 MHz

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
* DS5000FP	80-Pin FLAT PACK	0 to +70	DS5000FP - 8	8 MHz
*	80-Pin FLAT PACK	0 TO +70	DS5001FP -12	12 mhZ
*	80-Pin FLAT PACK	0 to +70	DS5000FP -16	16 MHz
	80-Pin FLAT PACK	-40 to +85	DS5000FPN - 8	8 MHz
*	80-Pin FLAT PACK	-40 to +85	DS5000FPN -12	12 MHz
	80-Pin FLAT PACK	-40 to +85	DS5000FPN -16	16 MHz
DS5000T		0 to +70	DS5000T 8- 8	8K RAM; 8 MHz
		0 to +70	DS5000T 8-12	8K RAM; 12 MHz
		0 to +70	DS5000T 8-16	8K RAM; 16 MHz
		0 to +70	DS5000T 32- 8	32K RAM; 8 MHz
		0 to +70	DS5000T 32-12	32K RAM; 12 MHz
*		0 to +70	DS5000T 32-16	32K RAM; 16 MHz
* DS5000TK	Kit	N/A	DS5000TK	
*DS5001FP	80-Pin FLAT PACK	0 to +70	DS5001FP - 8	8 MHz
*	80-Pin FLAT PACK	0 to +70	DS5001FP -12	12 MHz
*	80-Pin FLAT PACK	0 TO +70	DS5001FP -16	16 MHz
	80-Pin FLAT PACK	-40 to +85	DS5001FPN - 8	8 MHz
*	80-Pin FLAT PACK	-40 to +85	DS5001FPN -12	12 MHz
	80-Pin FLAT PACK	-40 to +85	DS5001FPN -16	16 MHz
*DS5002FP	80-Pin FLAT PACK	0 to +70	DS5002FP - 8	8 MHz
*	80-Pin FLAT PACK	0 to +70	DS5002FP -12	12 MHz
*	80-Pin FLAT PACK	0 to +70	DS5002FP -16	16 MHz
	80-Pin FLAT PACK	-40 to +85	DS5002FPN - 8	8 MHz
	80-Pin FLAT PACK	-40 to +85	DS5002FPN -12	12 MHz
	80-Pin FLAT PACK	-40 to +85	DS5002FPN -16	16 MHz
*DS5303FP	80-Pin FLAT PACK	0 to +70	DS5303FP	1.0 MHz
	80-Pin FLAT PACK	0 to +70	DS5303FP -A	1.5 MHz
*	80-Pin FLAT PACK	0 to +70	DS5303FP -B	2.0 MHz
	80-Pin FLAT PACK	-40 to +85	DS5303FPN	1.0 MHz
	80-Pin FLAT PACK	-40 to +85	DS5303FPN -A	1.5 MHz
	80-Pin FLAT PACK	-40 to +85	DS5303FPN -B	2.0 MHz
*DS5340FP	80-Pin FLAT PACK	0 to +70	DS5340FP	8 MHz
*	80-Pin FLAT PACK	0 to +70	DS5340FP -A	10 MHz
	80-Pin FLAT PACK	-40 to +85	DS5340FPN	8 MHz
	80-Pin FLAT PACK	-40 to +85	DS5340FPN -A	10 MHz
*DS6010		0 to +70	DS6010	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS606XA		-20 to +50	DS6065A	
*		-20 to +50	DS6066A	
		-20 to +50	DS6067A	
*DS6068A		-20 to +50	DS6068A	
*DS6068AK	Kit	N/A	DS6068AK	
*DS6070K	Kit	N/A	DS6070K	
*DS6071K	Kit	N/A	DS6071K	
*DS620X		0 to +70	DS6201	
*		0 to +70	DS6204U	Generic Code #1
*		0 to +70	DS6204U-2	Generic Code #2
*		0 to +70	DS6204U-3	Generic Code #3
*		0 to +70	DS6204U-4	Generic Code #4
*		0 to +70	DS6204U-5	Generic Code #5
		0 to +70	DS6204U-xxx	xxx = 001 to 999
		0 to +70	DS6205	
*		0 to +70	DS6207	Generic Code #1
*		0 to +70	DS6207-2	Generic Code #2
*		0 to +70	DS6207-3	Generic Code #3
*		0 to +70	DS6207-4	Generic Code #4
*		0 to +70	DS6207-5	Generic Code #5
		0 to +70	DS6207-xxx	xxx = 001 to 999
*DS630X		0 to +70	DS6301	
*		0 to +70	DS6304U	Generic Code #1
*		0 to +70	DS6304U-2	Generic Code #2
*		0 to +70	DS6304U-3	Generic Code #3
*		0 to +70	DS6304U-4	Generic Code #4
		0 to +70	DS6304U-xxx	xxx = 001 to 999
		0 to +70	DS6305	
*		0 to +70	DS6307	Generic Code #1
*		0 to +70	DS6307-2	Generic Code #2
*		0 to +70	DS6307-3	Generic Code #3
*		0 to +70	DS6307-4	Generic Code #4
*		0 to +70	DS6307-5	Generic Code #5
		0 to +70	DS6307-xxx	xxx = 001 to 999
DS6417		0 to +70	DS6417-1	1 Megabit Density
*		0 to +70	DS6417-2	2 Megabit Density
		0 to +70	DS6417-4	4 Megabit Density

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS6450		0 to +70	DS6450	
		0 to + 70	DS6450 DES	
*DS6460		-20 to +50	DS6460A	
*DS9000			DS9000	
*DS9002			DS9002	
*DS9003			DS9003	
*DS9005			DS9005	
*DS9006			DS9006	
*DS9006K	Kit		DS9006K	
*DS9020		0 to +70	DS9020	
*DS907X		.100" Pitch	DS9071 -30V	30 Pos.-Vertical
*		.100" Pitch	DS9071 -30I	30 Pos.-Inclined
*		.100" Pitch	DS9071 -35V	35 Pos.-Vertical
*		.100" Pitch	DS9071 -35I	35 Pos.-Inclined
*		.050" Pitch	DS9072 -40V	40 Pos.-Vertical
*		.050" Pitch	DS9072H -40R	40 Pos.-Right Angle=Hi
*		.050" Pitch	DS9072L -40R	40 Pos.-Right Angle-Low
*		.050" Pitch	DS9072 -68V	68 Pos.-Vertical
*		.050" Pitch	DS9072 -68I	68 Pos.-Inclined
*		.050" Pitch	DS9072H -68R	68 Pos.-Right Angle Hi
*		.050" Pitch	DS9072L -68R	68 Pos.-Right Angle-Low
*		.050" Pitch	DS9072 -72V	72 Pos.-Vertical
*		.050" Pitch	DS9072 -72I	72 Pos.-Inclined
*		.050" Pitch	DS9072H -72R	72 Pos.-Right Angle-Hi
*		.050" Pitch	DS9072L -72R	72 Pos.-Right Angle-Low
*			DS9075 -40V	40 Pos.-Vertiical; 40 Pins
*		.050" Pitch	DS9076 -40	40 Pins; 40 Pos.

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
*DS908x			DS9080V	Cyber Key-Vertical
*			DS9080A	Cyber Key-Angled
*			DS9081V	Cyber Key Recessed-Vertical
*			DS9081A	Cyber Key Recessed-Angled
*			DS9082V	Cyber Card-Vertical
*			DS9082A	Cyber Card-Angled
*			DS9083V	Cyber Card Recessed-Vertical
*			DS9083A	Cyber Card Recessed-Angled
*			DS9084V	Cyber Card EV Recessed-Vertical
*			DS9084A	Cyber Card EV Recessed-Angled
*DS9092			DS9092	
			DS9092G	Finger Grip
*DS9093			DS9093	
*DS9094			DS9094	

N/A = Not Applicable

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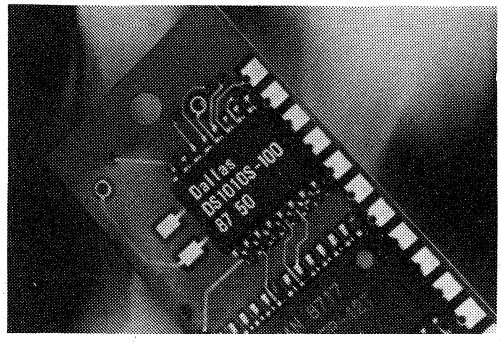
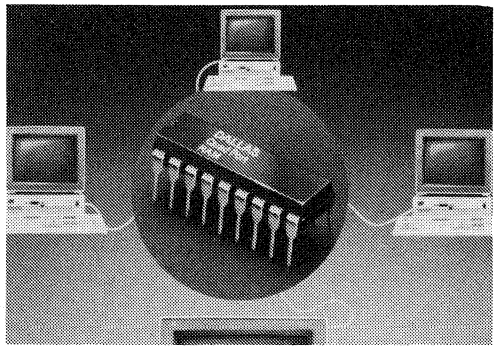
PRODUCT OVERVIEW

Dallas Semiconductor's 14 product families are outlined below.



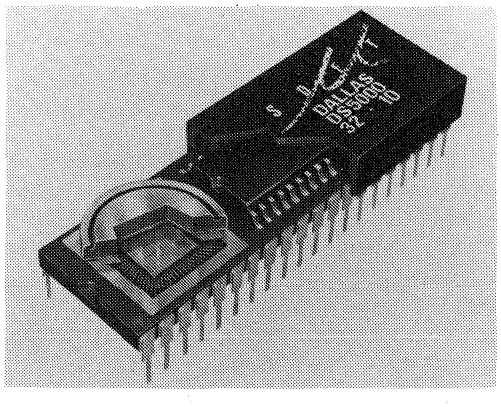
Silicon Timed Circuits

All-silicon time delay lines can withstand the high temperatures associated with surface mounting in small outline packages. They also offer better accuracy than the hybrid approach to delay lines. Laser writing techniques used to customize chips offer maximum flexibility from tailor-made products at off-the-shelf prices.



Multiport Memory

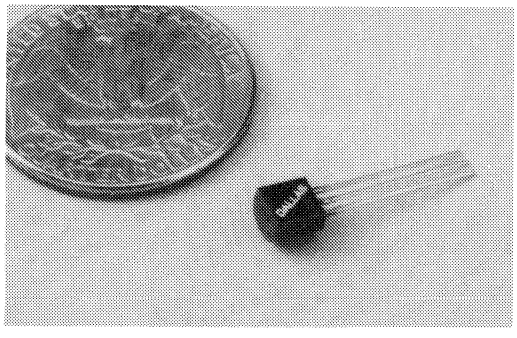
A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out procedures in storing and retrieving data, the products are dual-ported for simultaneous reads and writes.
This product family also includes a four-port memory chip that loosely couples up to four computers at low cost.



Microcontrollers

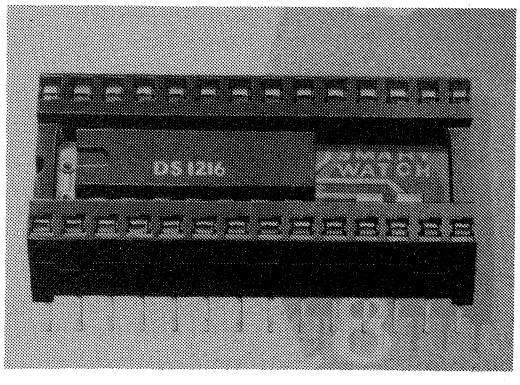
Unlike rigid ROM/EPROM microcontrollers, Dallas Semiconductor microcontroller chips are designed for change: they convert industry-standard bytewide SRAM into high-performance, read/write storage that is nonvolatile for more than ten years. This memory is initially loaded via a serial port and can be dynamically partitioned to fit program and data storage requirements. System performance can be improved based on cumulative knowledge maintained in nonvolatile RAM. On-chip crashproof circuitry and an external lithium cell permit task processing to resume after a power outage.

The DS5000 series Soft Micro Chips incorporate these features along with a complete core CPU which is 100% instruction set-compatible with the industry-standard 8051 microcontroller. An on-chip encryptor protects proprietary application software and confidential data. The DS53xx series Micro Softener Chips provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities for other industry-standard microprocessors, such as the V40. The Micro Stik and Soft Stik products combine the chips with SRAM and a lithium cell to provide a complete microcontroller system in an extremely small form factor. An optional permanently powered clock/calendar allows tasks to be scheduled and events to be logged in nonvolatile storage.



Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for 10 years in the absence of main power. When power goes out of tolerance, the built-in lithium energy source automatically switches on and write protection guards data from garbling during power loss.

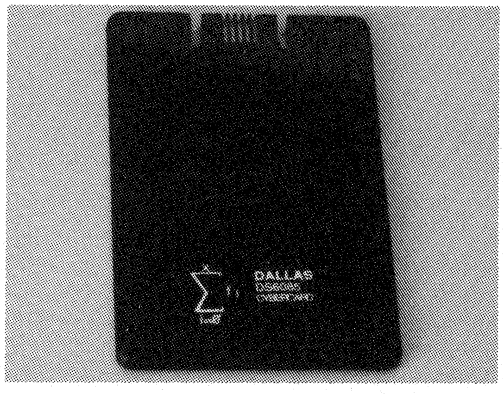


Intelligent Sockets

Intelligent sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.

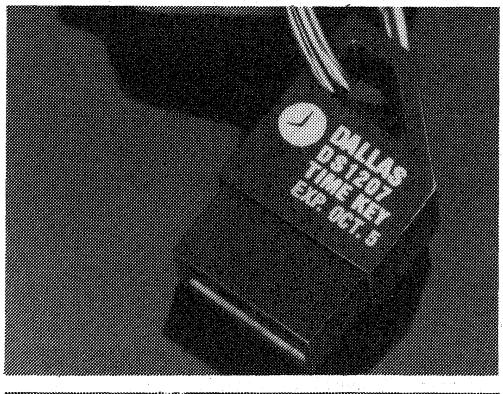
Timekeeping

A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, serial, PC DOS, and bytewide memory.



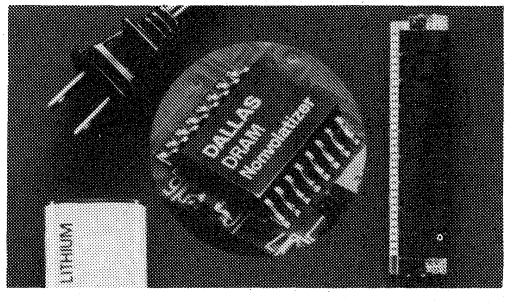
User-Insertable Memory

Nonvolatile memories with densities from 1024 to four million bits are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. Applications for such products include software authorization, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work records.



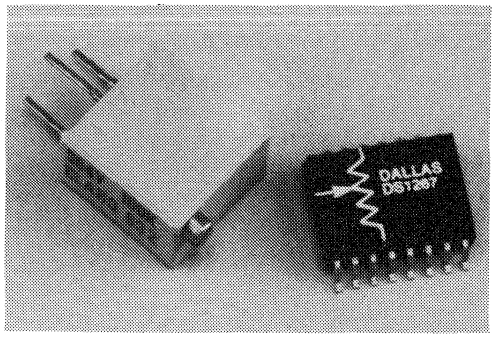
Security Products

These products provide security for intellectual property and data. Devices in this product family control access to software, buildings, and equipment, or let software authors and publishers limit the use of their products to a set period of time.



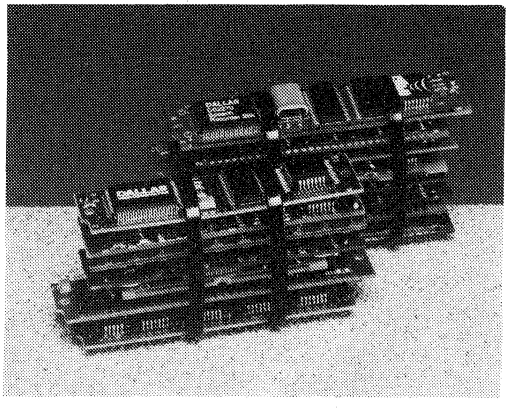
Integrated Battery Backup

This CMOS chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred. Products nonvolatize both static RAM and dynamic RAM.



System Extension

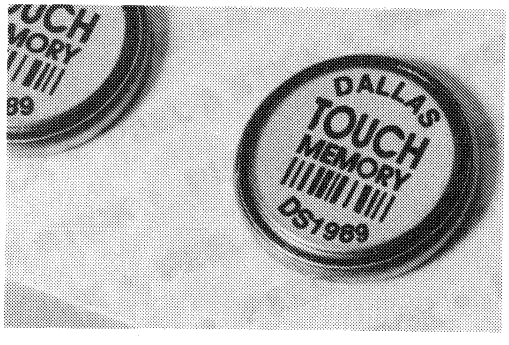
These CMOS products add a variety of special features to systems without encumbering design. For example, the Line Powered Transceiver connects portable systems to personal computers without consuming battery energy. The Micro Manager provides all necessary functions for power supply monitoring, reset control, and memory back-up in microprocessor-based systems. The Digital Potentiometer is an all-silicon variable resistor that can be set under software control and withstands the high temperatures associated with surface mounting.



SIP Stik™ Prefabs

SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.

The Dallas Semiconductor SIP Stik family can provide approximately 80 percent of the circuitry in a typical system. With SIP Stik prototype accessories, a complete system can be mocked up quickly and compactly.

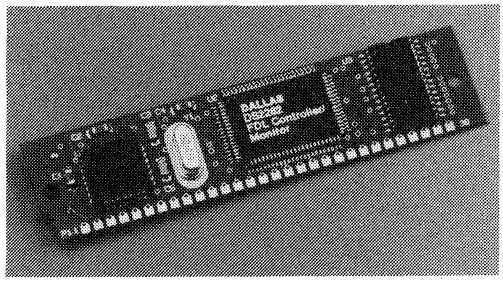


Automatic Identification

Chip-based identifiers read or write data using two methodologies: Proximity and Touch. With our auto ID technology, a chip attached to an object, or carried by a person, identifies and holds relevant information with little or no human intervention. These read/write data carriers can be updated via computer while affixed to an object. Auto ID chips can facilitate automation by tracking a work piece as it travels along an assembly line; people can access secure areas with convenience; and a hand-held terminal can be linked to a host system without burdensome cabling.

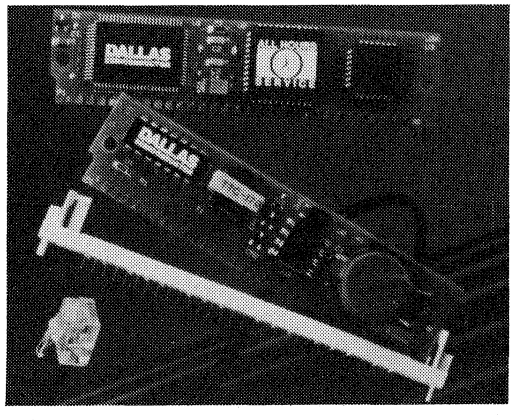
With our Proximity technology, a tagged item or person need only pass within five feet of a base station to establish a bidirectional communication link. A wide range of Proximity devices can be created with the versatile Micro Power Receiver/Interpreter Chip. In addition, Dallas Semiconductor offers ready-to-use proximity devices, optional chips for building high capacity tags, a Wireless Transceiver Stik for handhelds, a UHF Receiver Stik for incorporation into the host computer system, and a starter kit for evaluation.

Using Touch technology, a memory chip can be read or written with the touch of a probe. Each Touch Device is packaged in astainless steel MicroCan™ 16 mm in diameter; individual chips are also available, along with mounting accessories, probes, and an evaluation kit.



Telecommunications

A comprehensive product family addresses the requirements of high-speed digital voice/data transmission and monitoring in T1, CEPT or Primary Rate ISDN networks. ADPCM processors double or quadruple the capacity of voice communication channels through DSP compression techniques.



Teleservicing

Teleservicing products can monitor equipment performance 24 hours a day, release software revisions, perform diagnostics, and make adjustments -- all from a desktop computer over an ordinary telephone line. A growing family of coordinated hardware and software products offers new solutions to service problems at a price well under the cost of an airplane ticket. Components include cartridges for retrofit, modular components for new designs, and a software tool kit.

CORPORATE FACT SHEET

Dallas Semiconductor designs, manufactures, and markets electronic chips and chip-based subsystems called Stiks™. Rather than build products that others have already made, the company concentrates on one-of-a-kind solutions that span many application areas. Through the use of late definition technologies, Soft Silicon™ chips can be tailored after they are made -- even during use.

Founded February 1, 1984, Dallas Semiconductor has a multiproduct strategy to serve the needs of a variety of industries. The company's seven development teams constantly attack unsolved problems and introduce new products to the marketplace.

In its six-year history, Dallas Semiconductor has shipped 97 base products, with over 500 distinct variations, to more than 6,000 customers worldwide. These include Original Equipment Manufacturers (OEMs) in instrumentation, factory automation, personal computers, office equipment, telecommunications, medical equipment, and mainframe computers.

Chips and subsystems are sold through a direct sales force, distributors and manufacturers' representatives worldwide. Sales for 1989 totaled $82 million; the company shipped over $23 million worth of products during the first quarter of 1990. As of March 19, 1990, the company is traded on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions -- dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon™ is made possible by the Late Definition technologies of lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having a similar design. Direct laser writing also allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

The Company occupies 184,000 square feet of facilities in north Dallas. This location includes a six-inch, submicron chip-making plant, one of the most sophisticated wafer production plants in the world. It features Class One cleanliness; automated wafer processing; dry etch using plasma techniques; and 0.15 micron direct step alignment tolerances. Automated modular process technology provides substantial flexibil-

ity in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. As an example, our pick and place machine assembles Stik subassemblies under computer control and can position up to 4,500 chips per hour. All products are shipped from Dallas after final quality assurance and testing.

MARKETING AND SALES

Dallas Semiconductor coordinates its selling activity from its Dallas, Texas headquarters. Twelve area sales managers call on OEM accounts and coordinate the activities of 46 sales representative offices in North America and 34 in Europe and Asia. Dallas Semiconductor also markets its products in North America through national and regional stocking distributors.

QUALITY AND RELIABILITY

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSESS

* *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL-STD-105.

* *In-Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.

* *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.

* *In-Process Sample Tests:* In order to guarantee the accuracy and completeness of in-process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL-STD-105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new products, packages and equipment, as well as processes. A state-of-the-art environmental facility allows all major accelerated stresses to be performed and monitored in-house. In addition, a metallurgical laboratory has been equipped to perform real-time x-ray, x-ray flourescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer-based tracking and retrieval system. Technical support includes, among other things, oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production-ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype, Prequal, and Fully Qualified.

* *Prototype:* Prototype products either have not been characterized to all data sheet limits or do not meet data sheet limits. These products may or may not have any reliability data gathered. All prototype products will be branded PROTO and their data sheets will be labelled PRELIMINARY.

* *Prequal:* Prequal products have been fully characterized to data sheet limits and have their assembly process finalized. These products are in the process of being tested to full qualification requirements. The data sheets of prequal products will be labelled PRELIMINARY.

* *Fully Qualified:* Fully qualified products have been characterized to data sheet limits and pass the full qualification requirements given in the next section.

RELIABILITY TESTS

Table 1 lists the tests which an integrated circuit must pass in order to be classified as fully qualified.

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUITS Table 1

Stress/Test	Condition	Duration	Sample Size/C
Outgoing Elec. Test	Data Sheet	0 Hr	2303/0
Infant Life	125°C, 5.5V	48 Hr	767/0
Long Term Life	125°C, 5.5V	1000 Hr	354/2
Use Condition Prediction	55°C, 5.5V	<3000 Hr <100,000 Hr	<300 FITS <100 FITS
Hi Voltage Life	125°C, 7.0V	1000 Hr	129/1
Hi Temp. Storage	150°C, No Bias	500 Hr 1000 Hr	116/0
Temp. Humidity Bias	85°C / 85% RH, 5.5V	1000 Hr	129/1
Autoclave	121°C, 2 ATM Steam, Unbiased	96 Hr	45/0
Temp. Cycle	-55°C to +125°C	1000 cycle	116/0
X-Ray	Mil-Std 883		11/0
Bond Pull	Mil-Std 883	8 g Pre-mold	153/0 wires
Dimensions	Mil-Std 883 Method 2016		9/0

CAD SYMBOL LIBRARIES

The CAD Utility Company offers schematic symbol libraries containing all ICs in this data book for use with the following Computer Aided Design (CAD) systems:

Personal CAD Systems (PCCAPS)
Data I/O-FutureNet (DASH)
OrCAD (SDT)
AutoCAD

Each symbol is created according to the standards and practices of the respective CAD system. All required information about the IC is included in the symbol, such as pin I/O characteristics and power and ground information. With these libraries, you can spend more time on your design and less time creating symbols for your CAD system. Additional CAD systems may be supported in the future. Contact the CAD Utility Company for more information.

CAD Utility Company
21115 Devonshire Street, Suite 318
Chatsworth, CA 91311

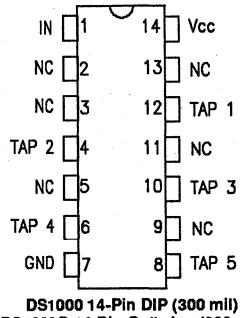
Tel. (805) 527-8630
FAX (805) 526-5093

DALLAS SEMICONDUCTOR

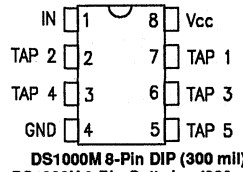
DS1000
5-Tap Silicon Delay Line

FEATURES
- All-silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Delay tolerance +/- 5% or +/-2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

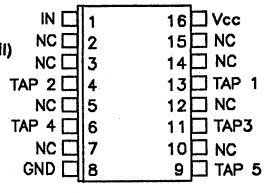
PIN DESCRIPTION



DS1000 14-Pin DIP (300 mil)
DS1000G 14-Pin Gullwing (300 mil)
DS1000K 14-Pin Sheared NC



DS1000M 8-Pin DIP (300 mil)
DS1000H 8-Pin Gullwing (300 mil)



DS1000S 16-Pin SOIC (300 mil)

Also Available in Die Form

PIN NAMES

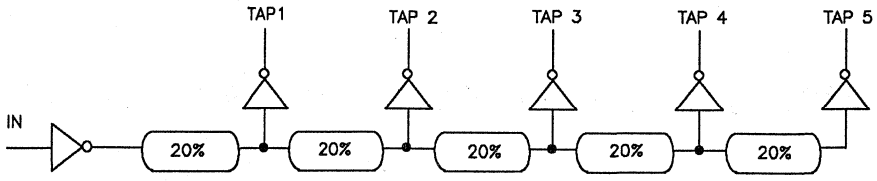
TAP 1-TAP 5	- TAP Output Number
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1000 series delay lines have five equally spaced taps providing delays from 5 ns to 500 ns. These devices are offered in a standard 14-pin DIP that is pin-compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000 series delay lines provide a nominal accuracy of +/-5% or +/- 2 ns, whichever is greater. The DS1000 5-tap silicon delay line reproduces the input logic level at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP2	TAP3	TAP4	TAP5
DS1000-25	5ns	10ns	15ns	20ns	25ns
DS1000-30	6ns	12ns	18ns	24ns	30ns
DS1000-35	7ns	14ns	21ns	28ns	35ns
DS1000-40	8ns	16ns	24ns	32ns	40ns
DS1000-45	9ns	18ns	27ns	36ns	45ns
DS1000-50	10ns	20ns	30ns	40ns	50ns
DS1000-60	12ns	24ns	36ns	48ns	60ns
DS1000-75	15ns	30ns	45ns	60ns	75ns
DS1000-100	20ns	40ns	60ns	80ns	100ns
DS1000-125	25ns	50ns	75ns	100ns	125ns
DS1000-150	30ns	60ns	90ns	120ns	150ns
DS1000-175	35ns	70ns	105ns	140ns	175ns
DS1000-200	40ns	80ns	120ns	160ns	200ns
DS1000-250	50ns	100ns	150ns	200ns	250ns
DS1000-350	70ns	140ns	210ns	280ns	350ns
DS1000-500	100ns	200ns	300ns	400ns	500ns

Custom delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground: -1.0V to + 7.0V
Operating temperature: -40°C to +85°C
Storage temperature: -55°C to + 125°C
Soldering temperature: 260°C for 10 seconds
Short circuit output current: 50mA for 1 second

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V +/- 5%)

PARAMETER	SYM COND.	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V $\leq V_I \leq$ Vcc	-1.0		1.0	uA	
Active Current	I_{CC}	Vcc= Max; Period= Min.		35	75	mA	2,8
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A= 25°C, Vcc=5V+/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of tap 5 t_{PLH}			ns	7
Input to TAP delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6,9
Input to TAP Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6,9
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE

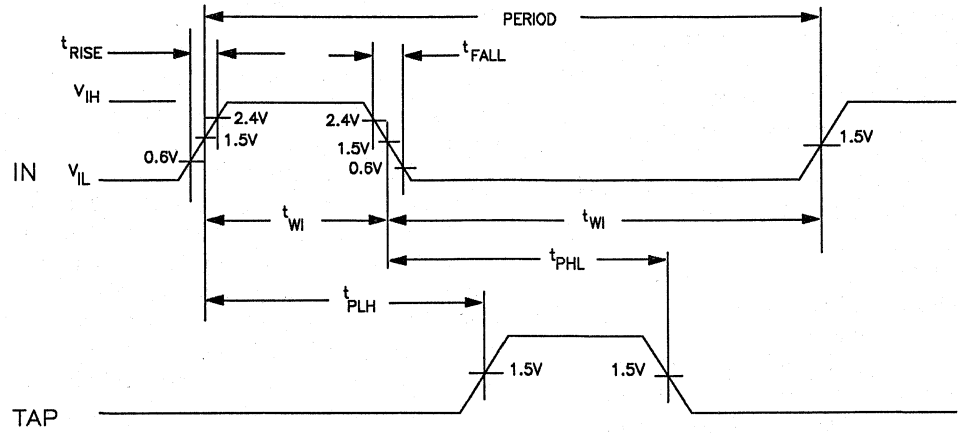
(t_A= 25° C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

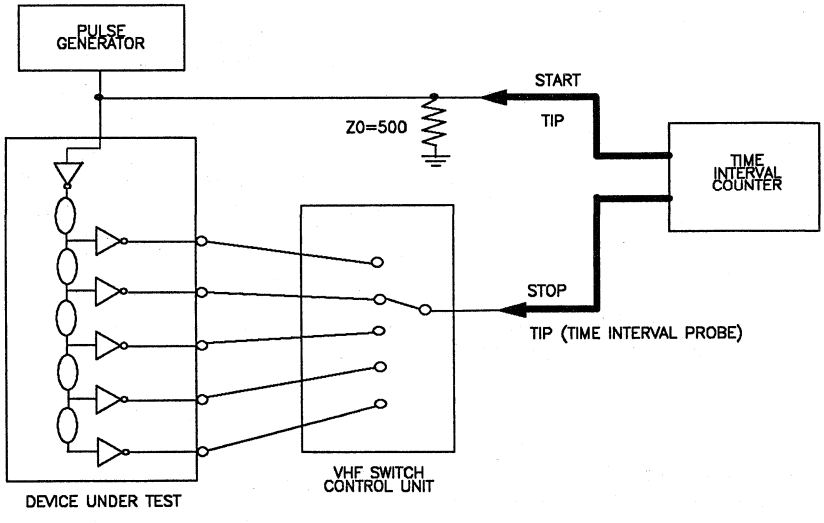
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. V_{CC}= 5V @25°C. Delays accurate on both rising and falling edges within +/- 2 ns or 5%.
4. Temperature variations between 0°C and 70°C will produce an additional delay shift of +/- 1 ns or +/- 3%, whichever is greater.
5. For DS1000-25 through -45, temperature variations between 0°C and 70°C will produce an additional shift of +/- 1 ns or +/- 9%, whichever is greater.
6. All tap delays tend to vary unidirectionally over temperature or voltage range. For example, if tap 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
7. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
8. I_{CC} is a function of frequency and TAP5 delay. Only a -25 operating with a 40 ns period and V_{CC} = 5.25V will have an I_{CC} = 75 mA. For example a -100 will never exceed 30 mA, etc.
9. See "Test Conditions" section at the end of this data sheet.

TIMING DIAGRAM--SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI}(Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS: INPUT

Ambient Temperature:	25°C +/- 3°C
Supply Voltage (V_{CC}):	5.0V +/- 0.1V
Input Pulse:	High = 3.0V +/- 0.1V Low = 0.0V +/- 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0ns Max. (measured between 0.6V and2.4V)
Pulse Width:	500ns (1us for -500)
Period:	1 us (2us for -500)

OUTPUT:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

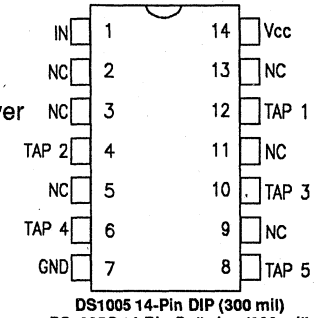
DALLAS SEMICONDUCTOR

DS1005
5-Tap Silicon Delay Line

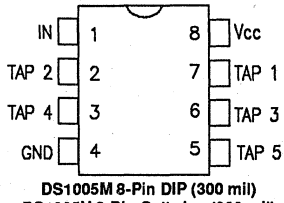
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance +/- 2 ns or +/- 2%, whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin-SOIC
- Low-power CMOS
- TTL /CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

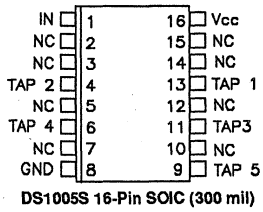
PIN DESCRIPTION



DS1005 14-Pin DIP (300 mil)
DS1005G 14-Pin Gullwing (300 mil)
DS1005K 14-Pin Sheared NC



DS1005M 8-Pin DIP (300 mil)
DS1005H 8-Pin Gullwing (300 mil)



DS1005S 16-Pin SOIC (300 mil)

Also Available in Die Form

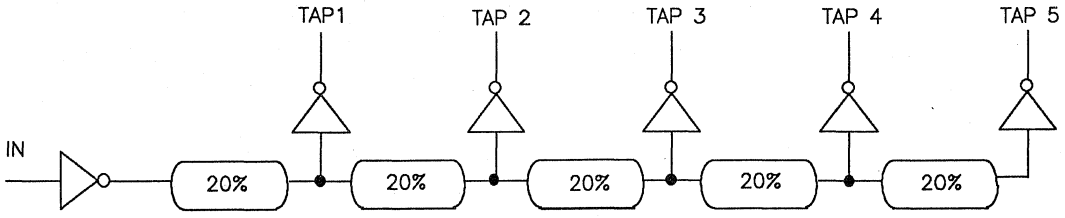
PIN NAMES

TAP 1-TAP 5	- TAP Output Number
Vcc	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of ± 2 ns or ± 2%, whichever is greater. This device is offered in a standard 14-pin DIP making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. The 14-pin DIP and 8-pin DIP are available in a surface mountable gullwing construction. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP2	TAP3	TAP4	TAP5
DS1005-60	12ns	24ns	36ns	48ns	60ns
DS1005-75	15ns	30ns	45ns	60ns	75ns
DS1005-100	20ns	40ns	60ns	80ns	100ns
DS1005-125	25ns	50ns	75ns	100ns	125ns
DS1005-150	30ns	60ns	90ns	120ns	150ns
DS1005-175	35ns	70ns	105ns	140ns	175ns
DS1005-200	40ns	80ns	120ns	160ns	200ns
DS1005-250	50ns	100ns	150ns	200ns	250ns

Custom delays available

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground	-1.0V to + 7.0V
Operating temperature	-40°C to 85°C
Storage temperature	-55°C to + 125°C
Soldering temperature	260°C for 10 seconds
Short circuit output current	50mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

D C ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V +/- 5%)

PARAMETER	SYM.	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5		
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \leq V_I \leq V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

A C ELECTRICAL CHARACTERISTICS

(t_A= 25°C, V_{CC}=5V+/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX.	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of tap 5 t_{PLH}			ns	7
Input to tap delay (leading edge)	t_{PLH}		Table 1		ns	3, 4,5,6
Input to tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4,5,6
Powerup Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES

1.All voltages are referenced to ground.
2.Measured with outputs open.
3.V_{CC}=5V @25°C. Delays accurate on both rising and falling edges within +/- 2 ns or +/- 2%, whichever is greater.
4.See Test Conditions.
5.The combination of temperature variations between 0°C and 70°C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of +/-1.5 ns or +/- 4%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage. For example, if TAP 1 slows down, all other taps will also slowdown; TAP 3 can never be faster than TAP 2.
7. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any TAP output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS-INPUT:

Ambient Temperature	25°C +/- 3°C
Supply Voltage (V_{CC})	5.0V +/- 0.1V
Input Pulse	High = 3.0V +/- 0.1V Low = 0.0V +/- 0.1V
Source Impedance	50 ohm Max.
Rise and Fall Time	3.0 ns Max.
Pulse Width	500 ns
Period	1us

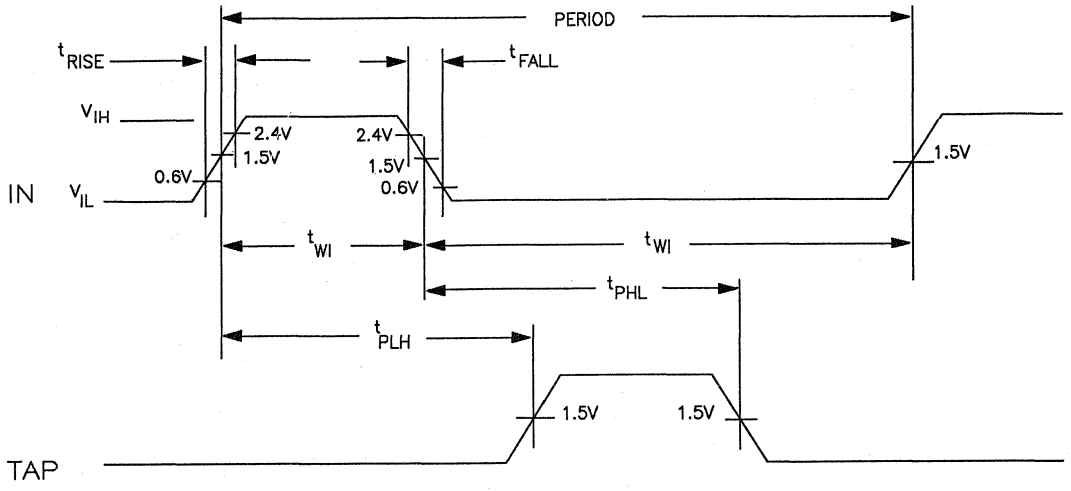
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

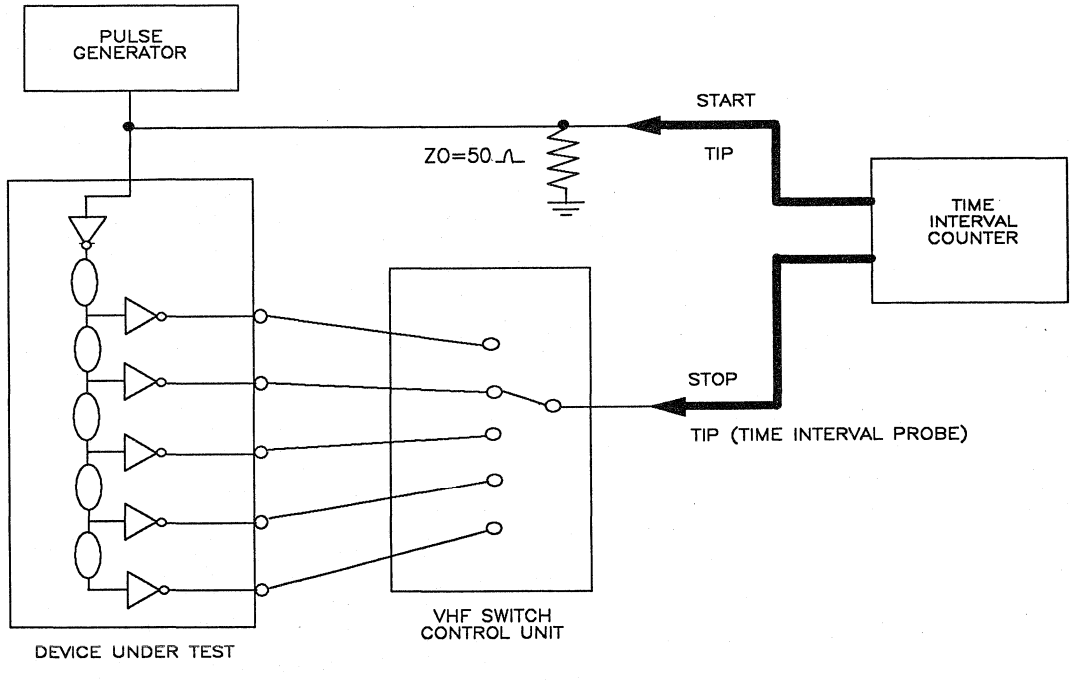
OUTPUT:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



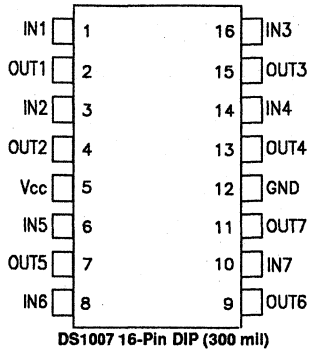
DALLAS SEMICONDUCTOR

DS1007
7- in -1 Silicon Delay Line

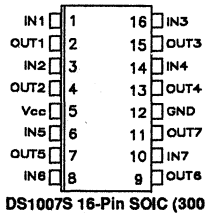
FEATURES

- All-silicon time delay
- 7 independent buffered delays
- Delay tolerance +/- 2 ns
- Four delays can be custom set between 3 ns and 10 ns
- Three delays can be custom set between 9 ns and 40 ns
- Delays are stable and precise
- Economical
- Auto-insertable, low profile
- Surface mount 16-pin SOIC
- Low-power CMOS
- TTL /CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom specifications available
- Quick turn prototypes
- Extended temperature range available

PIN DESCRIPTION



DS1007 16-Pin DIP (300 mil)



DS1007S 16-Pin SOIC (300 mil)

Also Available in Die Form

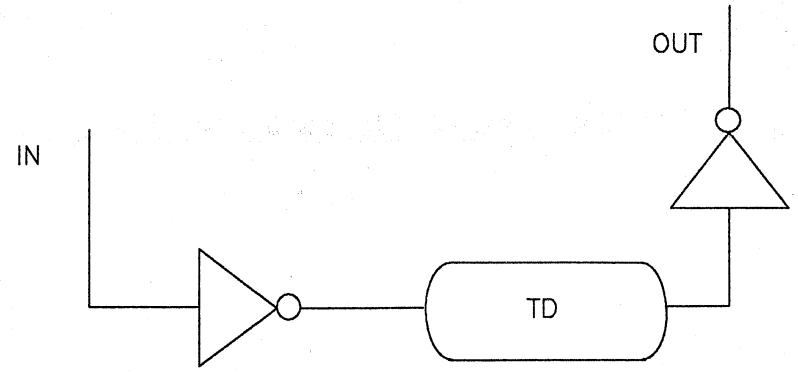
PIN NAMES

IN1 - IN7	- Inputs
Out1- Out7	- Outputs
GND	- Ground
Vcc	- +5 Volts

DESCRIPTION

The DS1007 7-in-1 Silicon Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 40 ns with an accuracy of +/- 2 ns at room temperature. The device is offered in both a 16-pin DIP and a 16-pin SOIC. Since the DS1007 is an all-silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic level at the output after the fixed delay. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



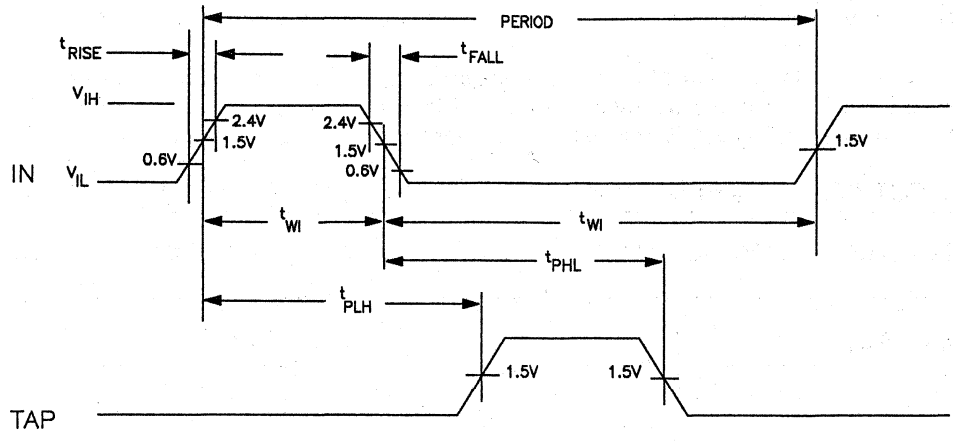
PULSE WIDTH > 100% OF DELAY

PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

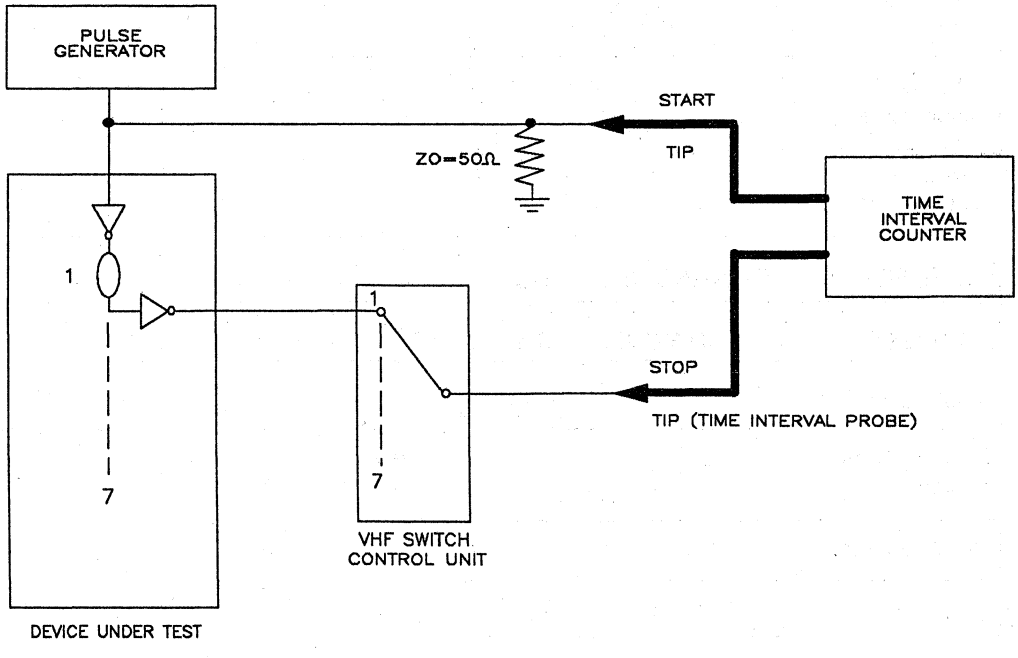
PART #	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
DS1007-1	3ns	4ns	5ns	6ns	9ns	13ns	18ns
DS1007-2	4	6	8	10	12	14	16
DS1007-3	3	3	3	3	10	10	10
DS1007-4	4	4	4	4	12	12	12
DS1007-5	5	5	5	5	15	15	15
DS1007-6	6	6	6	6	20	20	20
DS1007-7	7	7	7	7	25	25	25
DS1007-8	8	8	8	8	30	30	30
DS1007-9	9	9	9	9	35	35	35
DS1007-10	10	10	10	10	40	40	40
DS1007-11	3	4	6	8	10	12	14
DS1007-12	3	4	6	8	10	15	20
DS1007-13	3	4	6	8	12	15	20
DS1007-14	7	7	7	7	9	9	9

Custom delays available. Out 1 through Out 4 can be custom set from 3 to 10ns.
Out 5 through Out 7 can be custom set from 9 to 40ns.

TIMING DIAGRAM SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin to ground:	-1.0V to + 7.0V
Operating temperature:	-40°C° to + 85°C
Storage temperature:	-55°C to + 125°C
Soldering temperature:	260°C for 10 seconds
Short circuit output current:	50mA for 1 second

*This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V+/- 5%)

PARAMETER	SYMBOL COND.	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \leq V_I \leq V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}= Min. V_{OL}= 0.5V	12.0			mA	

A C ELECTRICAL CHARACTERISTICS

(t_A= 25°C, V_{CC}= 5V+/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5
Power-up Time	t_{PU}			100	ms	7
	Period	3 (t_{WI})			ns	6

CAPACITANCE

(t_A= 25° C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:
1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}=5V @25°C. Delays accurate on rising edges within +/- 2 ns.
4. See Test Conditions below.
5. All output delays in the same speed output tend to vary unidirectionally with temperature or voltage range (i.e., if tap 1 slows down, all other taps also slow down.
6. Period specifications may be exceeded; however, accuracy will be application- sensitive (decoupling, layout, etc.).
7. t_{PU} = 0 ms for Out 1 through Out 4.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge, and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C +/- 3°C
Supply Voltage (Vcc):	5.0V +/- 0.1V
Input Pulse:	High = 3.0V +/- 0.1V Low = 0.0V +/- 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 us

OUTPUT:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

NOTE:

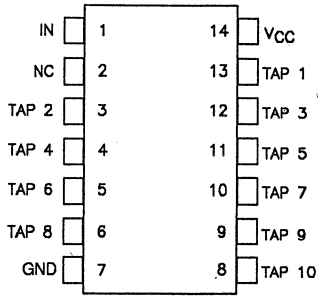
Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising edge.

DALLAS SEMICONDUCTOR

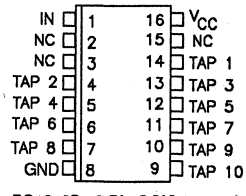
DS1010
10-Tap Silicon Delay Line

FEATURES
- All-silicon time delay
- 10 taps equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Delay tolerance +/- 5% or +/- 2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

PIN DESCRIPTION



DS1010 14-Pin DIP (300 mil)
DS1010G 14-Pin Gullwing (300 mil)



DS1010S 16-Pin SOIC (300 mil)

Also Available in Die Form

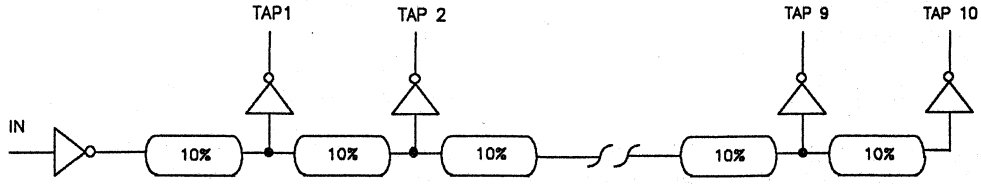
PIN NAMES

TAP1-TAP10	- Tap Output Number
Vcc	- 5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1010 series delay line has ten equally spaced taps providing delays from 5 ns to 500 ns. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternatively, a 16-pin SOIC is available for surface mount technology which reduces P C board area. Since the DS1010 is an all-silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1010 series delay lines provide a nominal accuracy of +/- 5% or +/- 2 ns, whichever is greater. The DS1010 reproduces the input logic level at the TAP 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

CATALOG P/N	TOTAL DELAY	DELAY/TAP (NS)
DS1010-50	50	5
DS1010-60	60	6
DS1010-75	75	7.5
DS1010-100	100	10
DS1010-125	125	12.5
DS1010-150	150	15
DS1010-175	175	17.5
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35
DS1010-400	400	40
DS1010-450	450	45
DS1010-500	500	50

Custom Delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin to Ground:	-1.0V to + 7.0V
Operating Temperature:	-40°C to + 85°C
Storage Temperature:	-55°C to + 125°C
Soldering Temperature:	260°C for 10 seconds
Short Circuit Output Current:	50mA for 1 second

*This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}= 5.0V +/- 5%)

PARAMETER	SYM	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	Vcc		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_L	$0.0V \leq V_I \leq V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}=Max: Period=Min.		40.0	75.0	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A = 25°C, V_{CC}= 5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	30% of TAP 10 t_{PLH}			ns	8
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6, 7
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6, 7
Power-up Time	t_{PU}			100	ms	
	Period	$3(t_{WI})$			ns	

CAPACITANCE

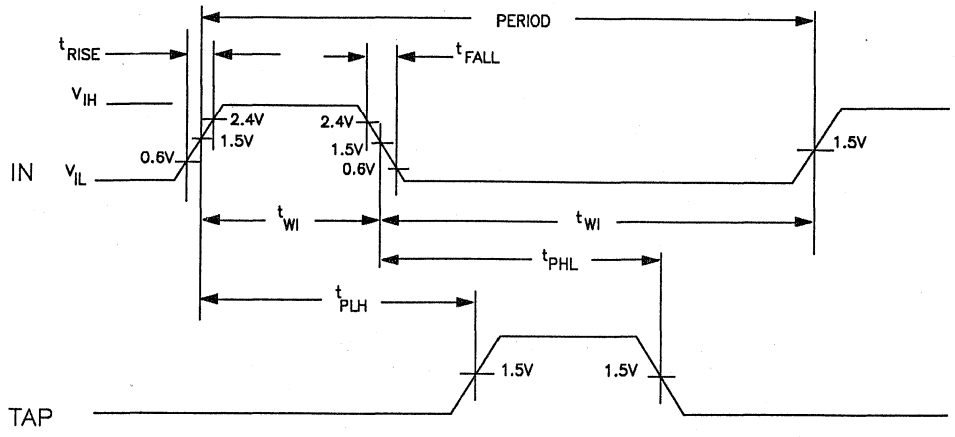
(t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

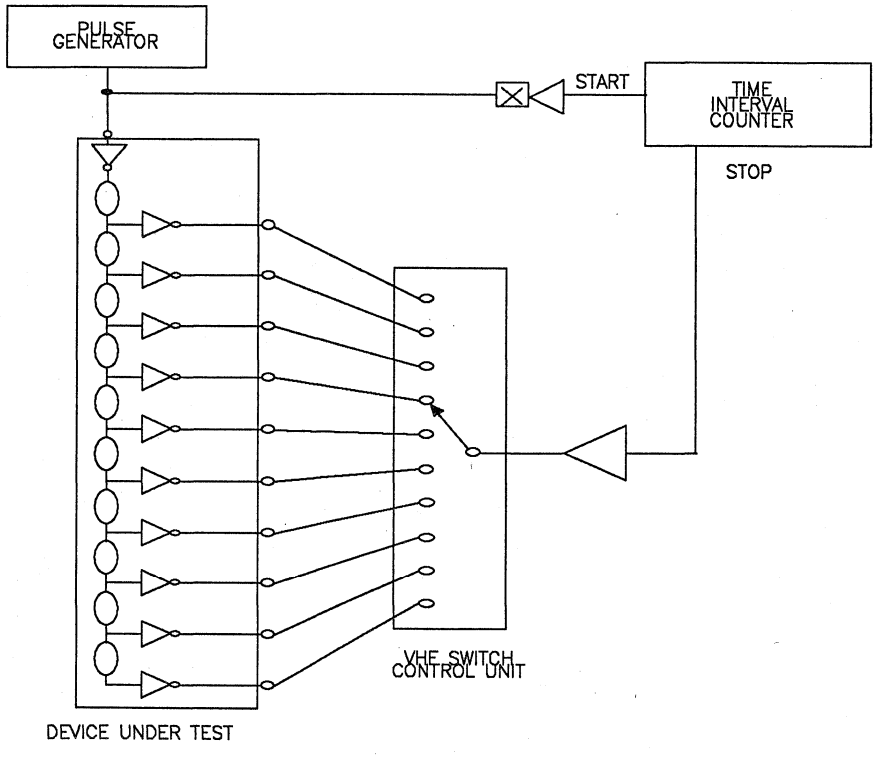
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @25°C. Delays accurate on both rising and falling edges within +/- 2 ns or +/- 5% whichever is greater.
4. See Test Conditions below.
5. Temperature variations between 0°C and 70°C will produce an additional delay shift of +/- 1ns or +/- 3%, whichever is greater.
6. For the DS1010-50, 60, and 75, temperature variations between 0°C and 70°C will produce an additional shift of +/- 1 ns or +/- 9%, whichever is greater.
7. All tap delays vary unidirectionally over temperature or voltage range (i.e., if tap 1 slows down, all other taps also slow down; tap 3 can never be faster than tap 2, etc.).
8. Pulse width and period specifications can be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C +/- 3°
Supply Voltage (V_{CC}):	5.0V +/- 0.1V
Input Pulse:	High=3.0V +/- 0.1V
	Low = 0.0V +/- 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Width:	500 ns (1us for -500)
Period:	1us (2us for -500)

OUTPUT:

Each output is loaded with a 74FO4. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

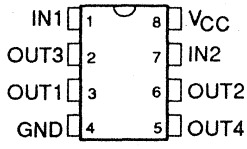
DALLAS SEMICONDUCTOR

DS1012
2- in -1 Sub-Miniature Silicon Delay Line with Logic

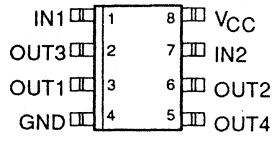
FEATURES

- All-silicon time delay
- 53 uW max. CMOS quiescent mode
- Surface mount 8-pin mini-SOIC and standard 8-pin DIP
- 2 independent buffered delays per input
- Option of complemented output(s)
- Option of timed AND, NAND, OR, NOR, XOR, XNOR, HALF-XOR and HALF-XNOR logic outputs
- Delay tolerance: + 1.5 ns (delays: 3-10 ns), + 2.0 ns (delays: 11-40ns)
- Vapor phase, IR and wave solderability
- Economical
- TTL/CMOS-compatible
- Quick turn prototypes
- Custom delays and logic options available

PIN DESCRIPTION



8-Pin DIP (300 Mil)



8-Pin SOIC (150 Mil)

Also Available in Die Form

PIN NAMES

IN1, IN2	Inputs
OUT1, OUT2	Outputs (delays)
OUT3, OUT4	Outputs (delays, logic)
GND	Ground
V_{CC}	+5 volts

DESCRIPTION

In its most simple configuration, the DS1012 2-in-1 Sub-Miniature Silicon Delay Line Chip provides two inputs, each of which in turn provides independent delays to a pair of outputs. Any of the four outputs can be inverted at the time of manufacture. The DS1012-1 and DS1012-3 are examples of catalog parts having this basic configuration.

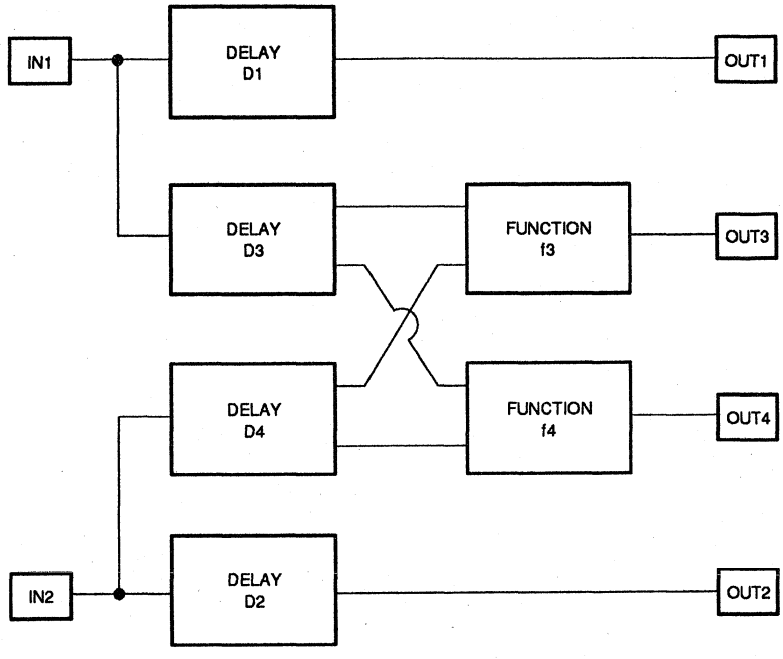
For applications requiring two-input timed logic functions, at the time of manufacture the simple delay on OUT4 can be replaced by one of the following: OR, NOR, XOR, or XNOR. Similarly, a timed AND, NAND, HALF-XOR (D3 and D4\), or NOT HALF-XOR (D3\ OR D4) can be substituted for the simple delay on OUT3. DS1012-2,

DS1012-4, and DS1012-5 are examples of catalog parts configured with logic functions on OUT3 and OUT4. Note that DS1012-2 also utilizes an output inversion on OUT2.

In any configuration, delays D1 (t_{D1}) and D2 (t_{D2}) can be specified within the range of ~3 ns to 10 ns. Delays D3 (t_{D3}) and D4 (t_{D4}) can be specified to have values between ~3 ns and 40 ns. The worst case leading edge delay accuracy at nominal voltage and room temperature is +/- 2 ns. The DS1012 is offered in two packages: an 8-pin DIP and an 8-pin 150 mil wide mini-SOIC.

Dallas Semiconductor offers the DS1012 in a wide variety of custom delay and logic configurations. For special requests and quick turn delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



Function f3 can be one of the following:

D3	D3\
D3 AND D4	D3 NAND D4
D3 HALF-XOR D4	D3 HALF-XNOR D4

Function f4 can be one of the following:

D4	D4\
D3 OR D4	D3 NOR D4
D3 XOR D4	D3 XNOR D4

NOTE:

Any output(s) can be inverted at time of manufacture.

If D1>10 ns, D1=D3.

If D2>10 ns, D2=D4.

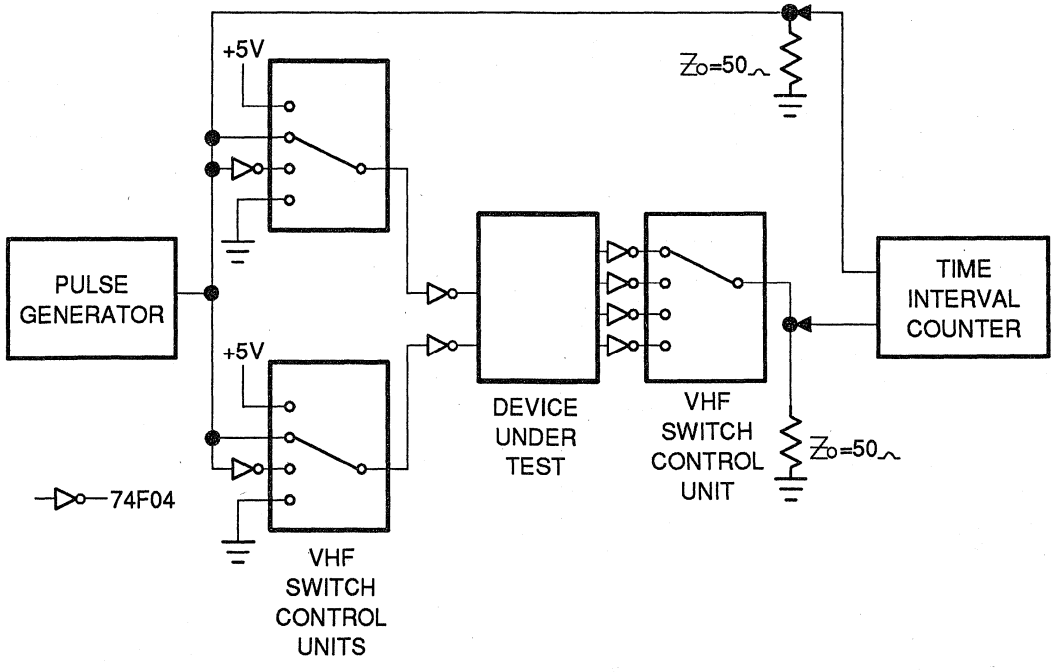
PART NUMBER DELAY AND CONFIGURATION TABLE1

CATALOG P/N	t_{D1} (ns)	t_{D2} (ns)	t_{D3} (ns)	t_{D4} (ns)	OUT1	OUT2	OUT3	OUT4
DS1012-1	5	5	10	10	D1	D2	D3	D4
DS1012-2	5	5	10	10	D1	D2\	D3.D4	D3+D4
DS1012-3	3	7	10	40	D1	D2	D3	D4
DS1012-4	5	5	25	25	D1	D2	D3HXD4	D3XD4
DS1012-5	10	10	5	5	D1	D2	D3.D4	D3+D4

NOTE:
. = AND, + = OR, X = XOR, HX = HALF-XOR.

Contact Dallas Semiconductor for information on custom configurations and timing delays.

TEST CIRCUIT FIGURE2



TEST SETUP DESCRIPTION

The above figure illustrates the hardware configuration used for measuring the timing parameters on thE DS1012. The input waveform is produced by a precision pulse generator under software control connected to the inputs by VHF switch control units. Time delays are measured by a time interval counter (20 ps resolution) connected between the inputs and the outputs. Outputs are connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 4888 bus.

TEST CONDITIONS:

INPUT:

Ambient Temperature:	25°C +/- 3°C
Supply Voltage (V_{CC}):	5.0V +/- 0.1V
Input Pulse:	High = 3.0V +/- 0.1V
	Low = 0.0 V +/- 0.1 V
Source Impedence:	50 Ohms Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1000 ns

OUTPUT:

Each output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V +/- 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V<=VI<=V_{CC}	-1.0		1.0	uA	
Active Current	I_{CCI}	V_{CC} = Max; Period = Min.		40.0	70.0	mA	2
Quiescent Current	I_{CC2}	V_{CC} = Max.			10	uA	5
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min. V_{OL} = 0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A =25°C, V_{CC} = 5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}				ns	6
Input to Output (leading edge)	t_{D1},t_{D2} t_{D3}, t_{D4}				ns	3, 4
Power-up Time	t_{PU}			0	ms	7
	Period	3(t_{WI})			ns	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period. I_{CC1} (max.) for any value of Period can be calculated using the formula:

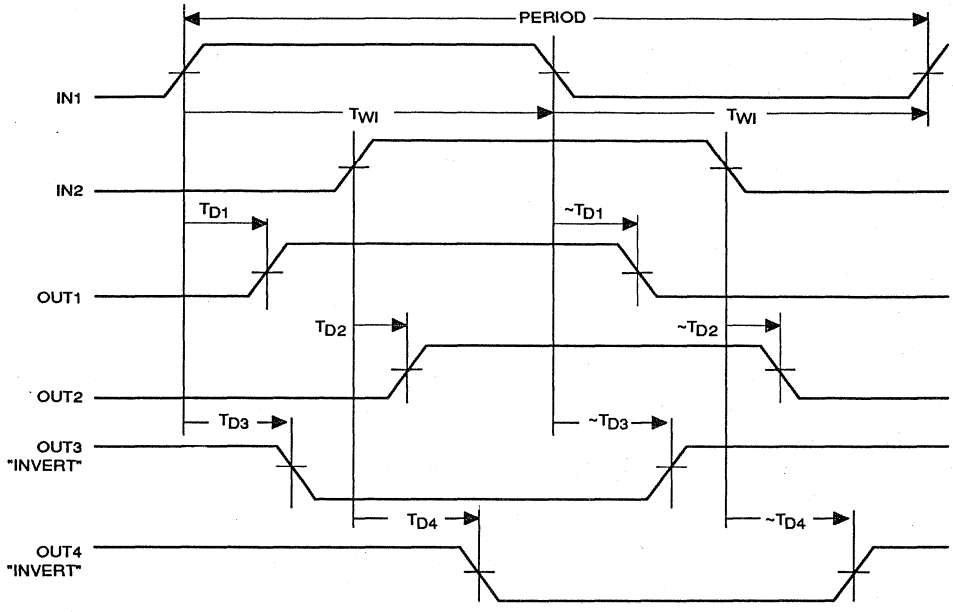
   I_{CC1} (max.) in mA = 840 mA-ns/Period (in ns) + I_{CC2} in mA

   Example: If Period = 50 ns then

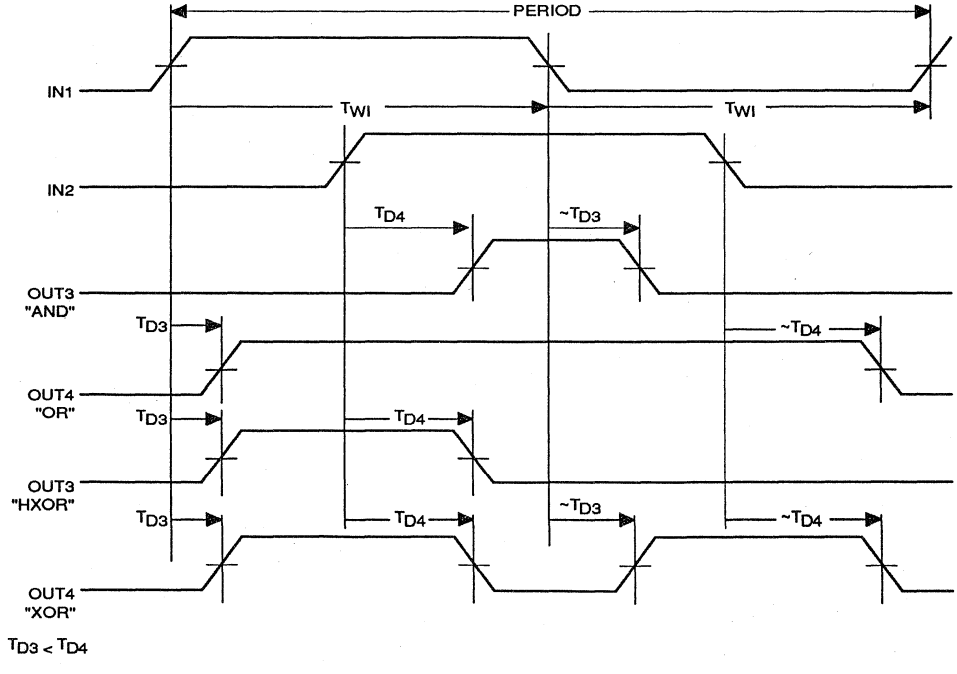
   I_{CC1} (Max) in mA = 840 mA-ns/50 ns + 0.01 mA = 16.81 mA
3. V_{CC} = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within +/- 1.5 ns for values between 3-10 ns and +/- 2 ns for values between 11-40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within +/- 1 ns.
4. See test conditions.
5. For the quiescent mode, both inputs meet the conditions

   $0.3\ V \geq V_i$ or $V_i \geq V_{CC} - 0.3$
6. T_{WI} is the longer of t_{D1} + 2 ns, t_{D2} + 2 ns, t_{D3} + 2 ns, or t_{D4} + 2 ns.
7. On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V_{CC} achieves nominal value.

DELAY FUNCTIONS Figure 3



LOGIC FUNCTIONS Figure 4

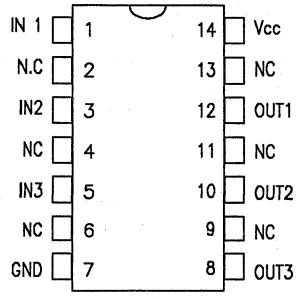


DALLAS SEMICONDUCTOR

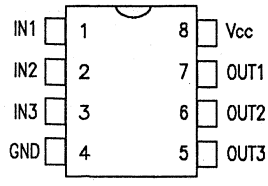
DS1013
3- in -1 Silicon Delay Line

FEATURES
- All-silicon time delay
- 3 independent buffered delays
- Delay tolerance +/- 2ns
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Quick turn prototypes
- Extended temperature ranges available

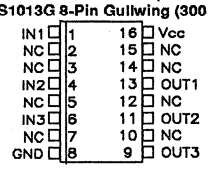
PIN DESCRIPTION



DS1013 14-Pin DIP (300 mil)
DS1013G 14-Pin Gullwing (300 mil)



DS1013M 8-Pin DIP (300 mil)
DS1013G 8-Pin Gullwing (300 mil)



DS1013S 16-Pin SOIC (300 mil)

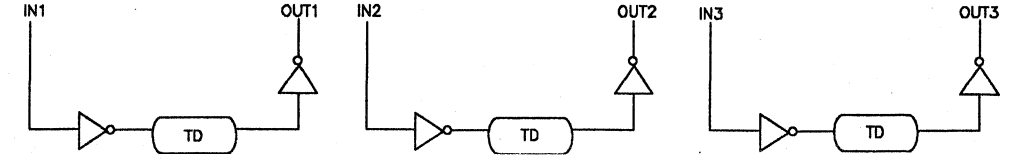
Also Available in Die Form

PIN NAMES

IN1, IN2, IN3	- Inputs
Out1, Out2, Out3	- Outputs
GND	- Ground
V_{CC}	- +5 Volts

DESCRIPTION
The DS1013 series of delay lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternative 8-pin DIP and surface mount packages are available which save PC board area. Since the DS1013 products are an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 series delay lines provide a nominal accuracy of +/- 2ns for delay times ranging from 10 ns to 75 ns, increasing to 5% for delays of 150 ns. The DS1013 delay line reproduces the input logic level at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1

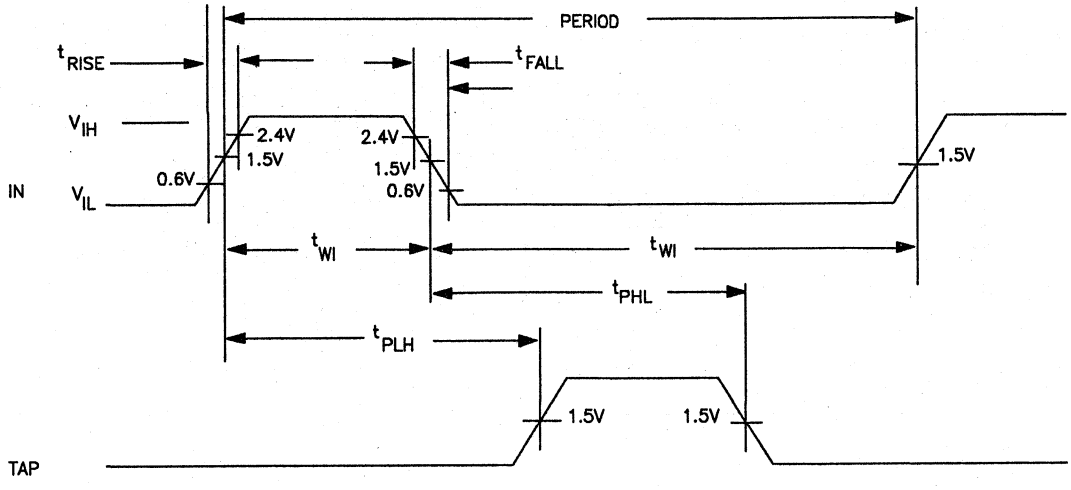


PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH},) Table 1

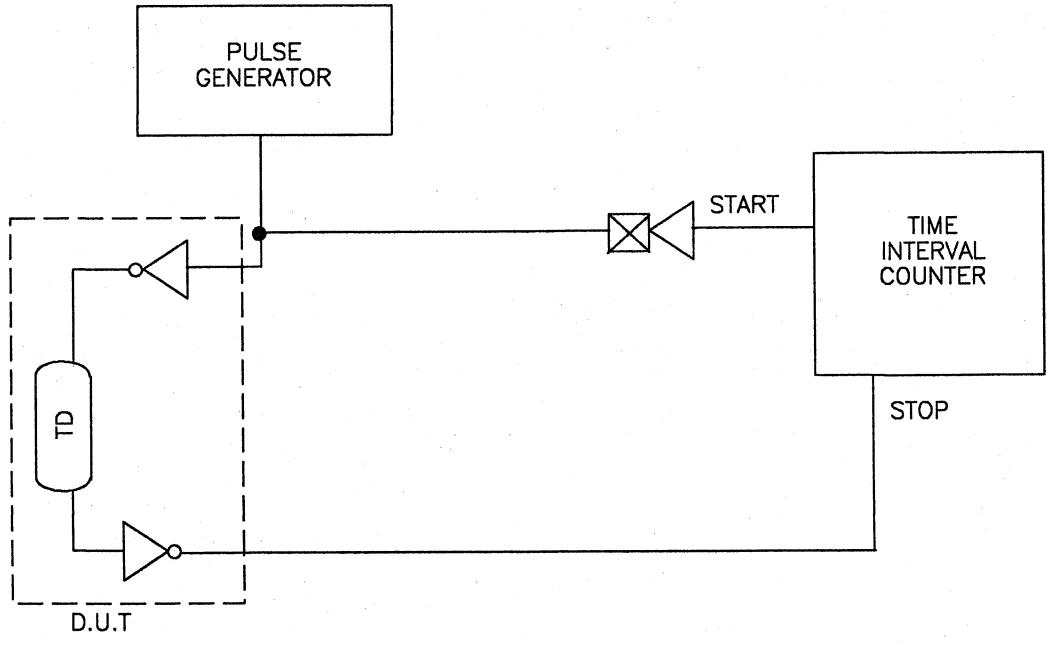
PART NO.	DELAY PER OUTPUT (ns)
DS1013-10*	10/10/10
DS1013-12*	12/12/12
DS1013-15	15/15/15
DS1013-20	20/20/20
DS1013-25	25/25/25
DS1013-30	30/30/30
DS1013-35	35/35/35
DS1013-40	40/40/40
DS1013-45	45/45/45
DS1013-50	50/50/50
DS1013-55	55/55/55
DS1013-60	60/60/60
DS1013-65	65/65/65
DS1013-70	70/70/70
DS1013-75	75/75/75
DS1013-80**	80/80/80
DS1013-90**	90/90/90
DS1013-100**	100/100/10
DS1013-150***	150/150/150

*Consult Dallas Semiconductor for availability.
Custom delays available.
** +/- 3% tolerance.
*** +/- 5% tolerance.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin to Ground: -1.0V to + 7.0V
Operating Temperature: -40°C to + 85°C
Storage Temperature: -55°C to + 125°C
Soldering Temperature: 260°C for 10 seconds
Short Circuit Output Current: 50mA for 1 second

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$, V_{CC}= 5.0V+/- 5%)

PARAMETER	SYMBOL	TEST COND.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		VCC+0.5		
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \leq V_I \leq V_{CC}$	-1.0		1.0	mA	
Active Current	I_{CC}	V_{CC}= Max Period= Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min V_{OL}=0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(t_A= 25°C, V_{CC}=5.0V+/-5%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Output Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	$3(t_{WI})$			ns	7

CAPACITANCE

(t_A= 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @25°C. Delays accurate on both rising and falling edges within ± 2 ns for -10 to -75, ±3% for -80 to -100 and ± 5% for -150.
4. See Test Conditions below.
5. The combination of temperature variations between 0° C and 70° C and voltage variations between 4.75 volts and 5.25 volts produce a worst case delay shift of ± 1.5 ns or ± 3%, whichever is greater.
6. All output delays tend to vary unidirectionally over temperature or voltage ranges (ie., if tap 1 slows down, all other taps also slow down).
7. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C +/- 3°C
Supply Voltage (V_{CC}):	5.0V +/- 0.1V
Input Pulse:	High = 3.0V +/- 0.1V Low = 0.0V +/- 0.1V
Source Impedance:	50 ohms Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1us

OUTPUT:

Each output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

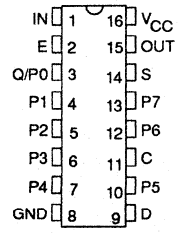
DALLAS SEMICONDUCTOR

DS1020
Programmable 8-Bit Silicon Delay Line

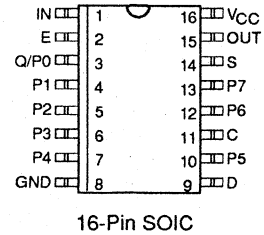
FEATURES

- All-silicon time delay
- Models with 0.25ns, 0.5ns, 1ns, and 2ns steps
- Leading and trailing edge accuracy
- Standard 16-pin DIP or 16-pin SOIC
- Auto-insertable
- Low-power CMOS
- TTL/CMOS-compatible
- Programmable using 3-wire serial port or 8-bit parallel port

PIN DESCRIPTION



16-Pin DIP
(300 Mil)



16-Pin SOIC
(300 Mil)

ALSO AVAILABLE IN DIE FORM

PIN NAMES

IN	-Delay Input
P0-P7	-Parallel Program Pins
GND	-Ground
OUT	-Delay Output
V_{CC}	- +5 volts
S	-Mode Select
E	-Enable
C	-Serial Port Clock
Q	-Serial Data Output
D	-Serial Data Input

DESCRIPTION

The DS1020 Programmable 8-Bit Silicon Delay Line product family consists of 8-bit, user-programmable CMOS silicon integrated circuits. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The fastest model (-025) offers a maximum delay of 73.75ns with an incremental delay of 0.25ns, while the slowest model (-200) has a maximum delay of 520ns with an incremental delay of 2ns. All models have an inherent (step zero) minimum delay of 10ns. After the user-determined delay, the input logic level is reproduced at the output without inversion. The DS1020 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1020 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC.

PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1020 will reproduce the logic level of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. To provide for infrequent modification of the delay value, jumpers should be used to connect the input pins to V_{CC} and ground. For applications requiring frequent timing adjustment, DIP switches can be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. By observing the data setup (T_{DSE}) and data hold (T_{DHE}) requirements, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (T_{EDV} or T_{PDV}) is required before input logic levels are accurately delayed.

Since the DS1020 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1020 will reproduce the logic level of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (T_{DSC}) and data hold (T_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (T_{EDV}) is required before the delay is accurate.

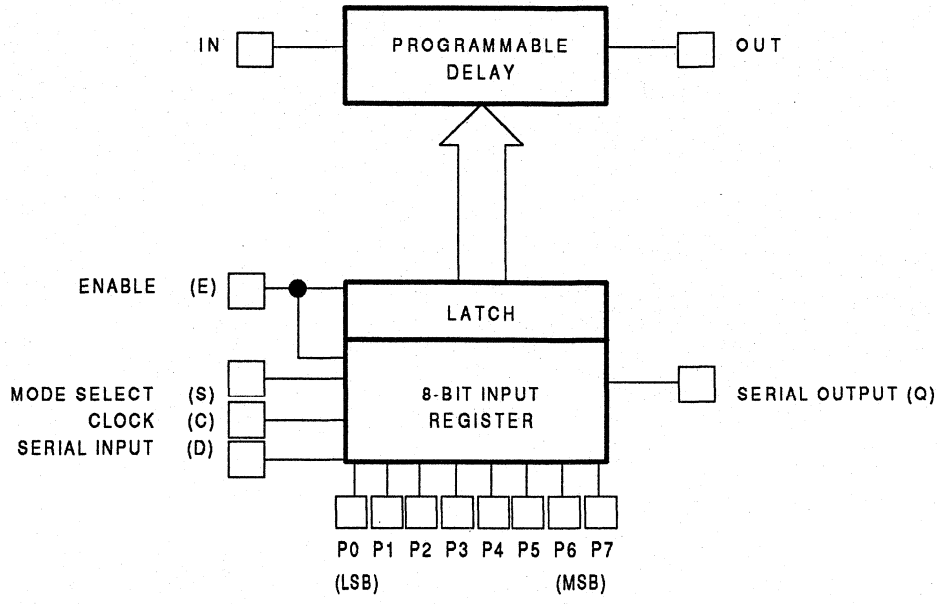
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1020 to the serial input of a second DS1020, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1020 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

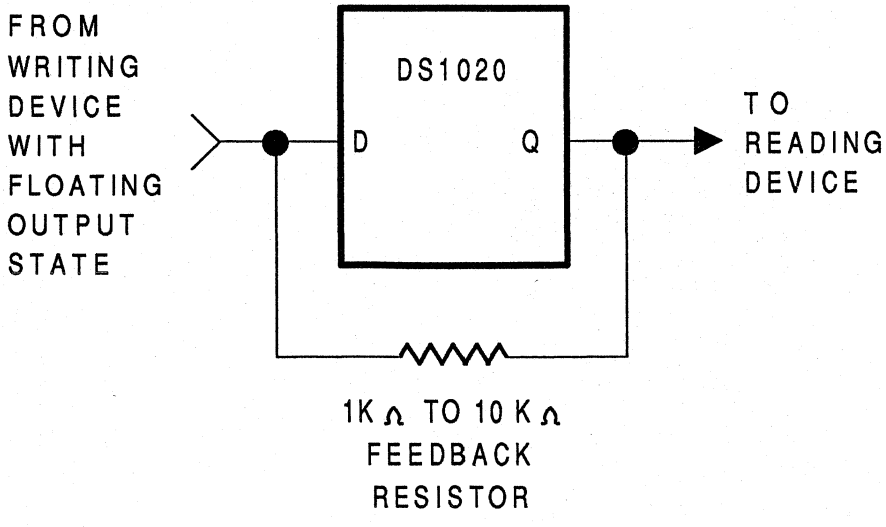
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time (T_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 --> 1) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time T_{CQV}. To restore the input register to its original state, this clocking process must be repeated 8 times. In the case of a daisy-chain, the process must be repeated 8 times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time (T_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1020 is a CMOS design, unused input pins (P1 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

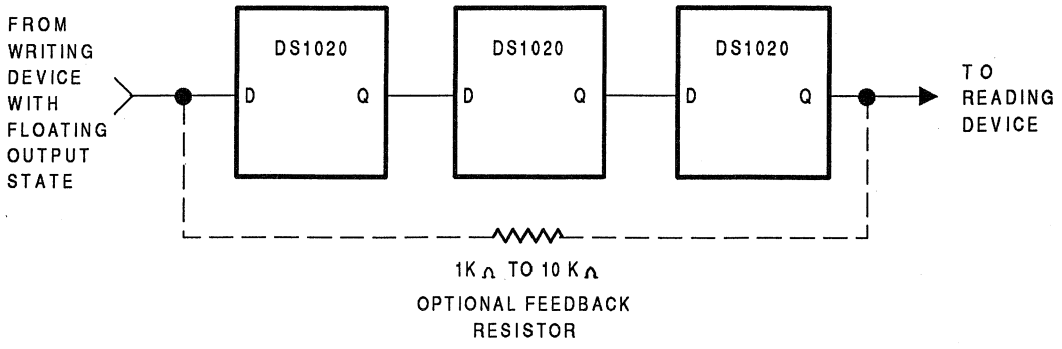
FUNCTIONAL BLOCK DIAGRAM Figure 1



SERIAL READOUT Figure 2



CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



PART NUMBER TABLE Table 1

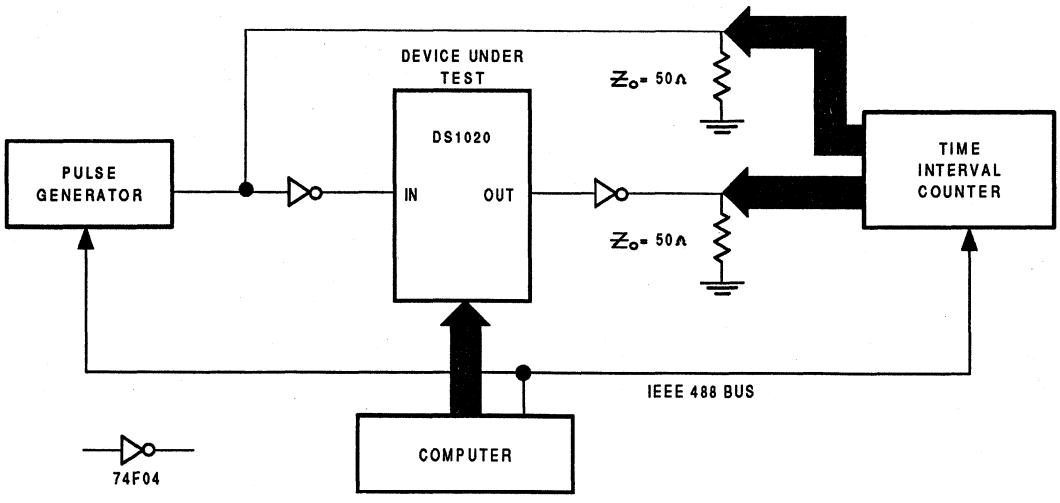
DELAYS AND TOLERANCES (in ns)				
PART NUMBER	**STEP ZERO DELAY TIME**	**MAX DELAY TIME (NOM)**	**DELAY CHANGE PER STEP (NOM)**	**MAX DEVIATION FROM PROGRAMMED DELAY**
DS1020-025	10 ± 2	73.75	0.25	± 4
DS1020-050	10 ± 2	137.5	0.5	± 6
DS1020-100	10 ± 2	265	1	± 8
DS1020-200	10 ± 3	520	2	± 12

DELAY VS. PROGRAMMED VALUE Table 2

	STEP ZERO						MAX DELAY	PAR-ALLEL PORT	SERIAL PORT
BINARY	0	0	0	0	0	0	1	P7	MSB
PROGRAM-	0	0	0	0	0	0	1	P6	
MED VALUE	0	0	0	0	0	0	1	P5	
	0	0	0	0	0	0	1	P4	
	0	0	0	0	0	0	1	P3	
	0	0	0	0	1	1	1	P2	
PART	0	0	1	1	0	0	0	P1	
NUMBER	0	1	0	1	0	1	1	P0	LSB
DS1020-025	10.00	10.25	10.50	10.75	11.00	11.25	73.25	73.50	73.75
DS1020-050	10.0	10.5	11.0	11.5	12.0	12.5	136.5	137.0	137.5
DS1020-100	10	11	12	13	14	15	263	264	265
DS1020-200	10	12	14	16	18	20	516	518	520

All delays in nanoseconds, referenced to input pin.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1020. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1020 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

INPUT:	**TEST CONDITIONS**
Ambient Temperature:	25°C ± 3°C
Supply Voltage (Vcc):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 Ohms Max.
Rise and Fall Time:	3.0 ns Max.
	(measured between 0.6V and 2.4V)
Pulse Width :	500 ns (DS1020-025, -050, -100)
	1000 ns (DS1020-200)
Period :	1 *us* (DS1020-025, -050, -100)
	2 *us* (DS1020-200)

NOTE:
Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground:	-1.0V to +7.0V
Operating Temperature:	-40°C to +85°C
Storage Temperature:	-55°C to +125°C
Soldering Temperature:	250°C for 10 Sec.
Short Circuit Output Current:	50 mA for 1 Sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+ 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0 \leq V_I \leq V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC} = Max. Period = 1us			30.0	mA	
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 2.7V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min. V_{OL} = 0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			10	MHz	
Enable Width	t_{EW}	50			ns	
Clock Width	t_{CW}	50			ns	
Data Setup to Clock	t_{DSC}	30			ns	
Data Hold from Clock	t_{DHC}	10			ns	
Data Setup to Enable	t_{DSE}	30			ns	
Data Hold from Enable	t_{DHE}	10			ns	
Enable to Serial Output Valid	t_{EQV}			50	ns	
Enable to Serial Output High Z	t_{EQZ}	0		50	ns	
Clock to Serial Output Valid	t_{CQV}			50	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	
Enable Setup to Clock	t_{ES}	50			ns	
Enable Hold from Clock	t_{EH}	50			ns	
Parallel Input Valid to Delay Valid	t_{PDV}			50	us	
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Enable to Delay Valid	t_{EDV}			50	us	
Enable to Delay Invalid	t_{EDX}	0			ns	
V_{CC} Valid to Device Functional	t_{PU}			100	us	
Input Pulse Width	t_{WI}	100% of Output Delay			ns	
Input to Output Delay	t_{PLH},t_{PHL}		Table 2		ns	2
Input Period	Period	3(t_{WI})			ns	

CAPACITANCE

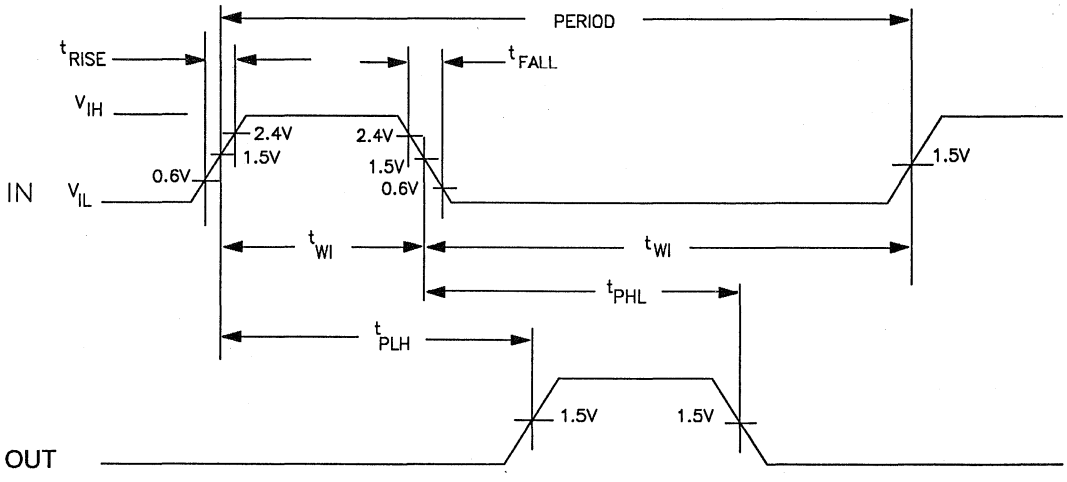
(t_A = 25°C)

PARAMETER	SYMBOL	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}	10	pF	

NOTES

1. All voltages are referenced to ground.
2. @V_{CC}=5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.

TIMING DIAGRAM SILICON DELAY LINE-Figure 5



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

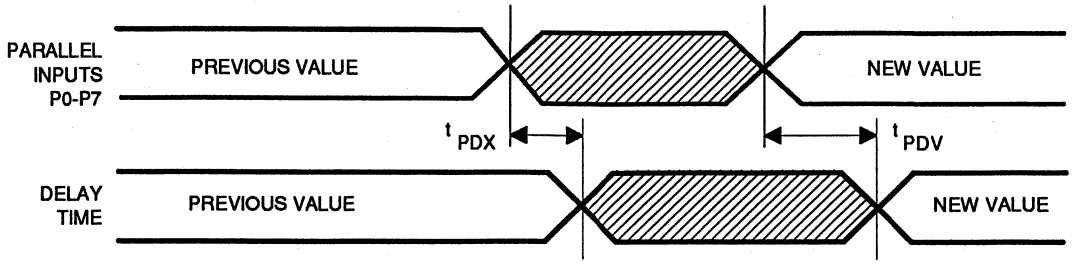
t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

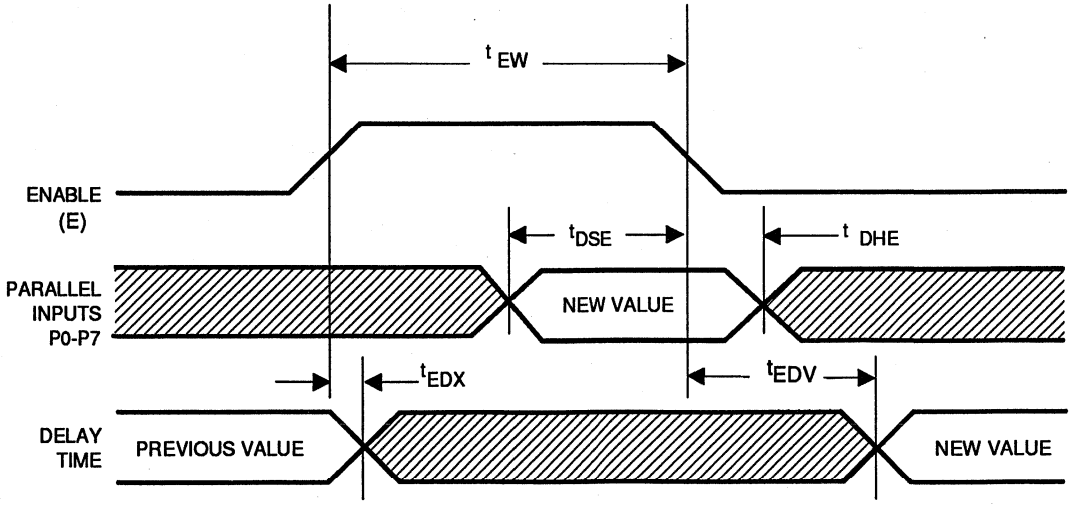
t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

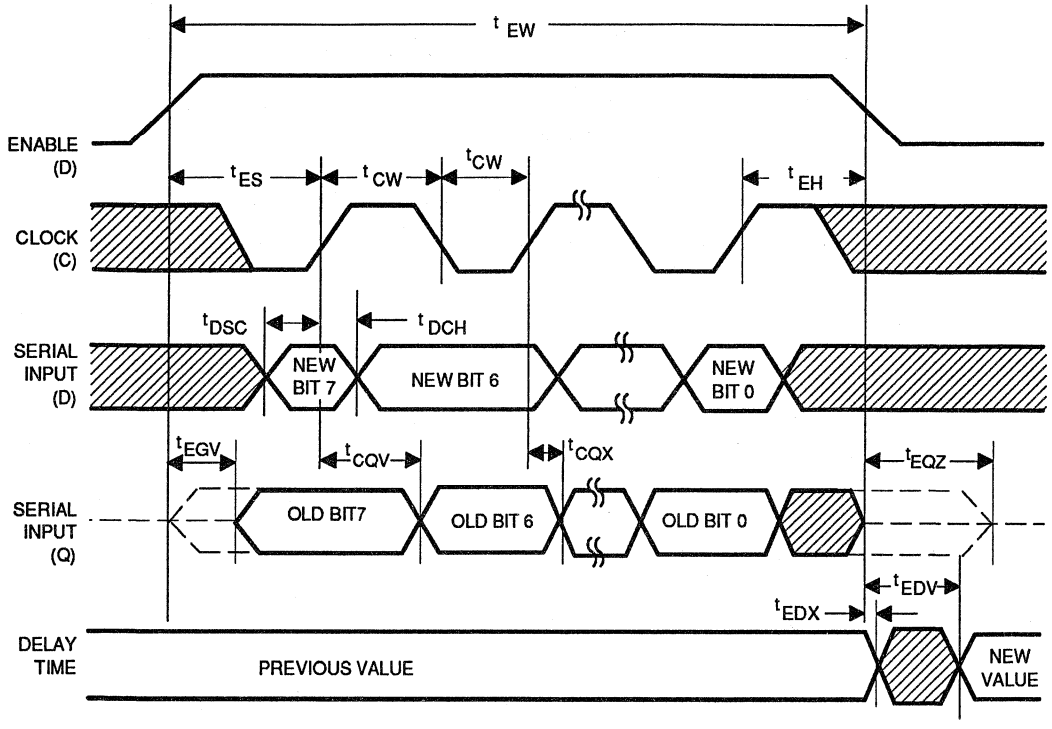
TIMING DIAGRAM NON-LATCHED PARALLEL MODE (S=1, E=1) Figure 6



TIMING DIAGRAM LATCHED PARALLEL MODE (S=1) Figure 7



TIMING DIAGRAM SERIAL MODE (S=0) Figure 8



Multiport Memory

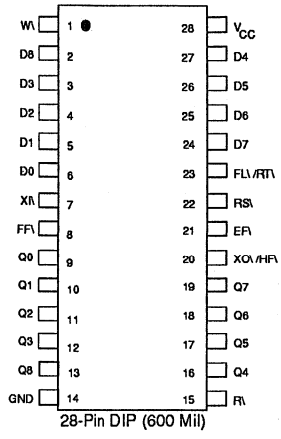
DALLAS SEMICONDUCTOR

DS2009
512 x 9 FIFO Chip

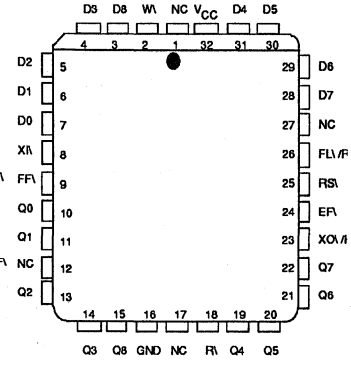
FEATURES

- First-in, first-out memory-based architecture
- Flexible 512 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to + 85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access times

PIN DESCRIPTION



28-Pin DIP (600 Mil)



32-Pin PLCC

PIN NAMES (\ Denotes Condition Low)

W\	- WRITE
R\	- READ
RS\	- RESET
FL\/RT\	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
XI\	- Expansion In
XO\/HF\	- Expansion Out/Half Full
FF\	- Full Flag
EF\	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2009 512 x 9 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2009 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a first-in, first-out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register-based FIFOs, the DS2009 employs a memory-based architecture wherein a byte written into the device does not ripple through. Instead, a byte written into the DS2009 is stored at a specific location where it remains until over-written. The byte can be read and re-read as often as desired.

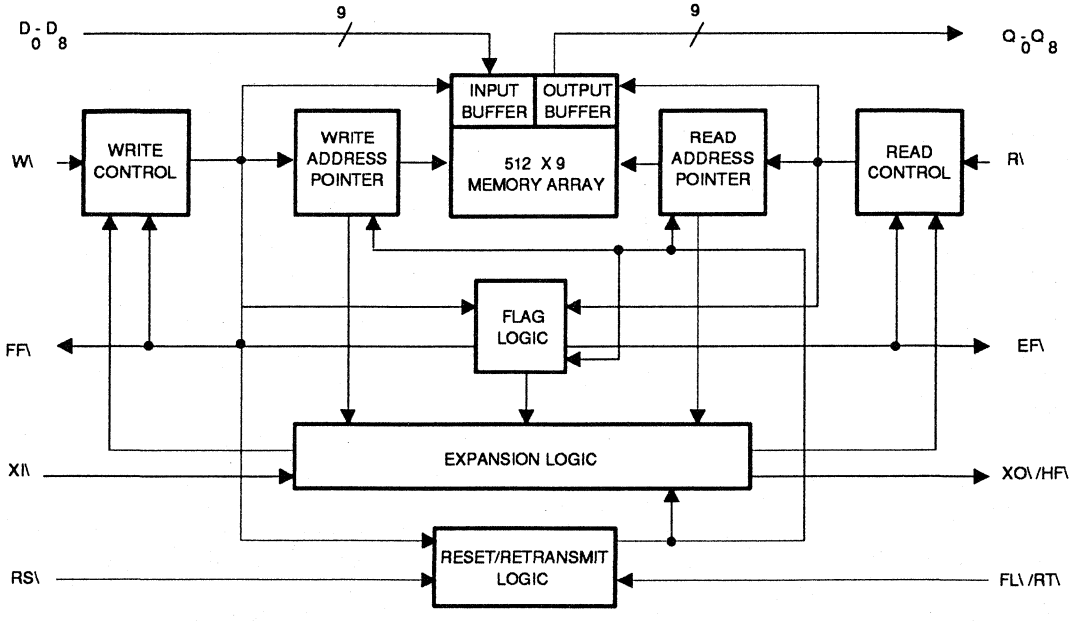
Twin address pointers (ring counters) automatically generate the address required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading unwritten bytes (reading while empty) or over-writing unread bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2009 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2009 can connect the read, write, data in, and data out lines of the DS2009 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion in and expansion out pins as appropriate (see the "Expansion Timing" section for a more complete discussion).

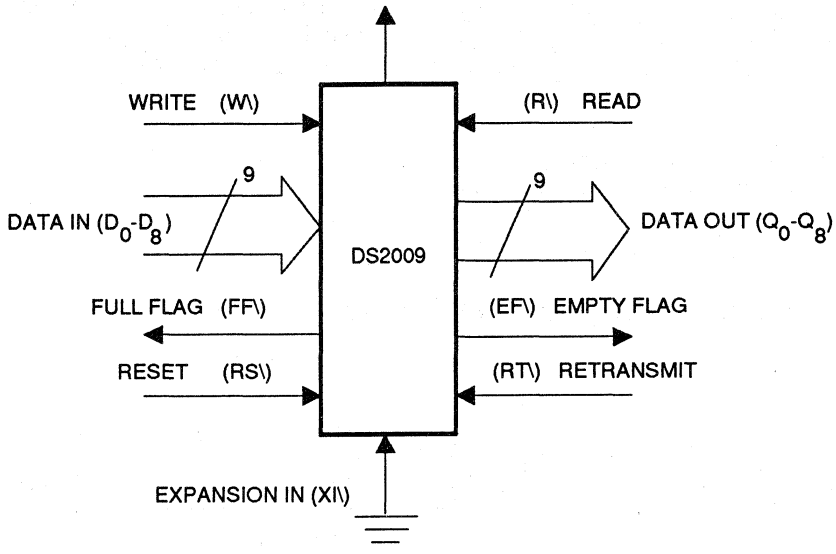
BLOCK DIAGRAM Figure 1



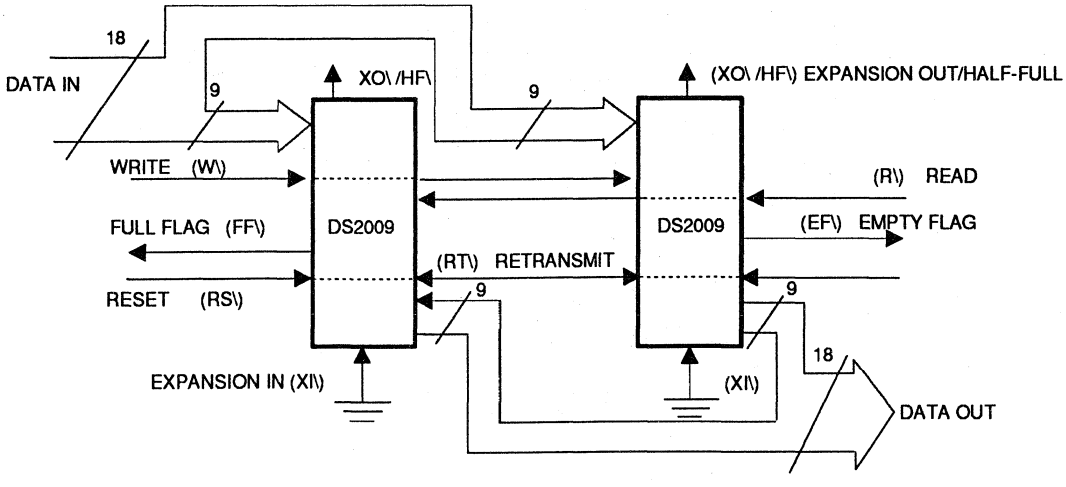
SINGLE DEVICE CONFIGURATION

A single DS2009 can be used when application requirements are for 512 words or less. The DS2009 is placed in single device configuration mode when the chip is reset with the Expansion In pin (XI\) grounded (see Figure 2).

A SINGLE 512 x 9 FIFO CONFIGURATION Figure 2



A 512 x 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:

Flag detection is accomplished by monitoring the FF\, EF\ and HF\ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

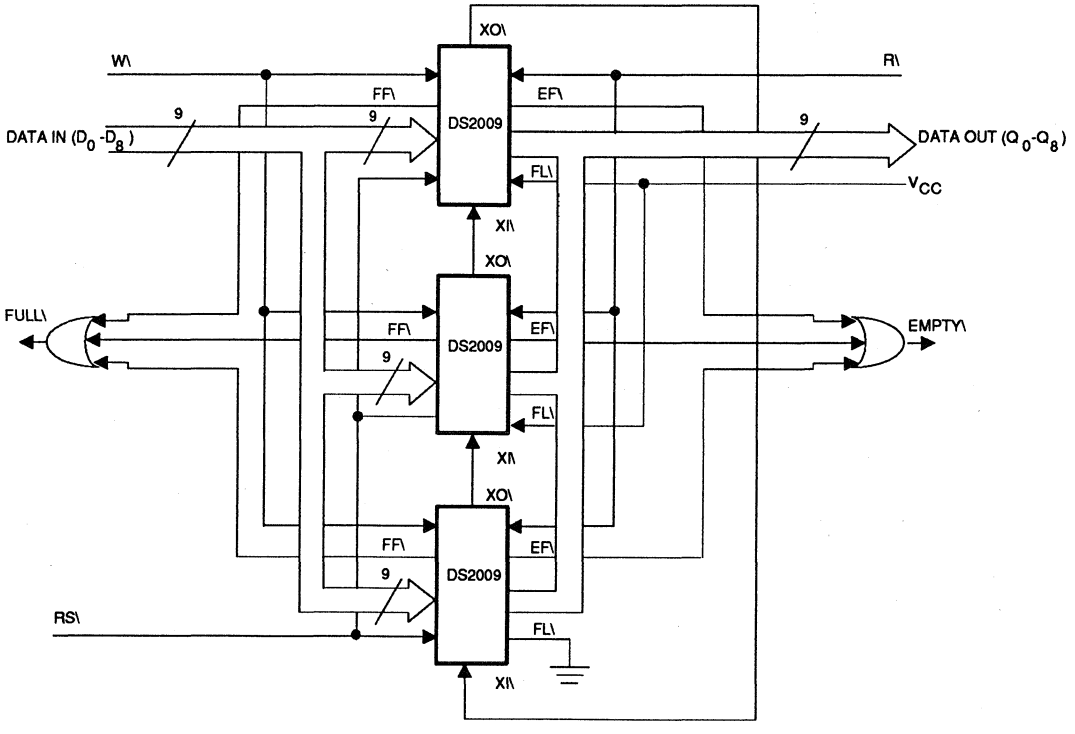
The DS2009 can easily be adapted to applications where more than 512 words are required. Figure 4 demonstrates depth expansion using three DS2009s. Any depth can be attained by adding DS2009s.

External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all EF\s and the ORing of all FF\s (i.e., all must be set to generate the correct composite FF\ or EF\).

The DS2009 operates in the depth expansion configuration after the chip is reset under the following conditions.

1. The first device must be designated by grounding the First Load pin (FL\). The retransmit function is not allowed in the depth expansion mode.
2. All other devices must have FL\ in the high state.
3. The Expansion Out (XO\) pin of each device must be tied to the Expansion In (XI\) pin of the next device. The half-full capability is not allowed in depth expansion.

A 1536 x 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



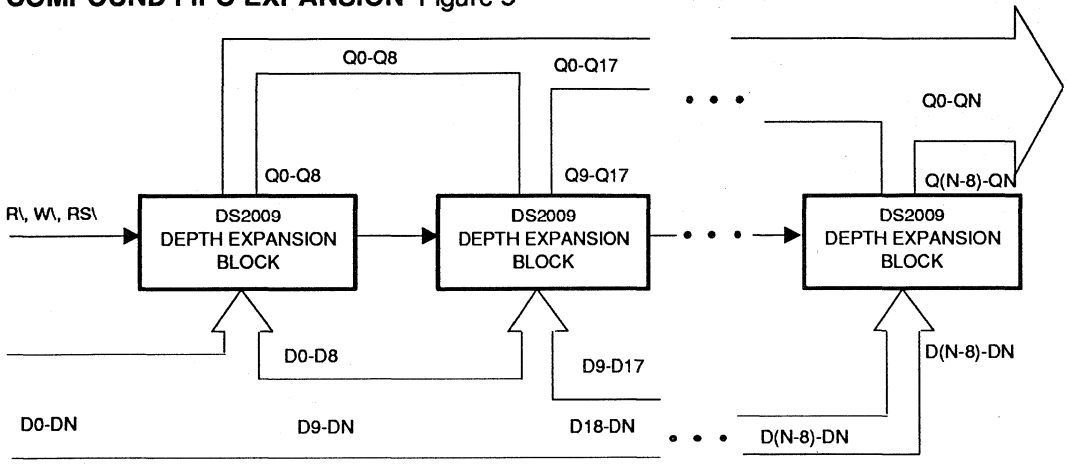
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Bidirectional applications that require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing DS2009s as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., FF\ is monitored on the device where W\ is used; EF\ is monitored on the device where R\ is used). Both depth expansion and width expansion can be used in this mode.

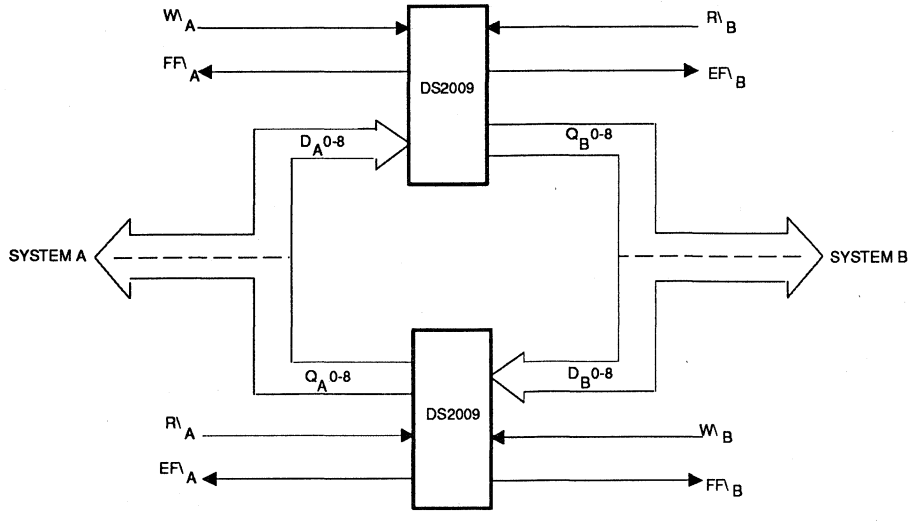
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block diagram see "Depth Expansion" section and Figure 4.
2. For flag operation see "Width Expansion" section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



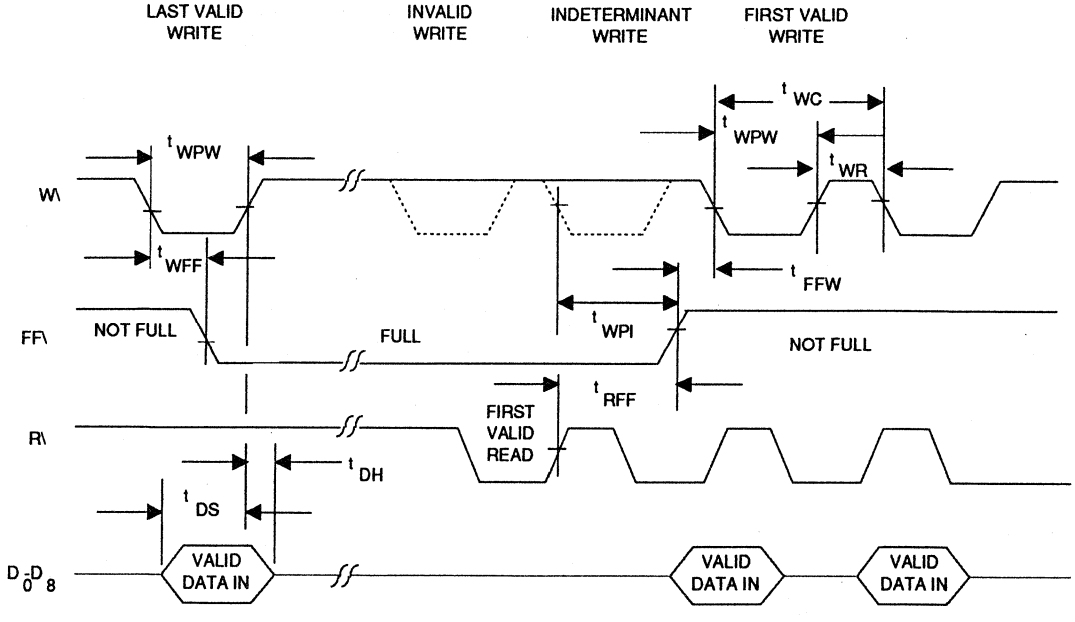
HALF-FULL CAPABILITY

In the single-device and width-expansion modes, the XO\/HF\ output acts as an indication of a half-full memory. (XI\ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag (HF\) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The half-full flag is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2009 initiates a write cycle (see Figure 7) on the falling edge of the write enable control input (W\), provided that the Full Flag (FF\) is not asserted. Data setup and hold time requirements must be satisfied with respect to the rising edge of W\. The data is stored sequentially and independent of any ongoing read operations. FF\ is asserted during the last valid write as the DS2009 becomes full. Write operations begun with FF\ low are inhibited. FF\ will go high t_{RFF} after completion of a valid read operation. Writes beginning after FF\ goes low and more than t_{WPI} before FF\ goes high are invalid (ignored). Writes beginning less than t_{WPI} before FF\ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

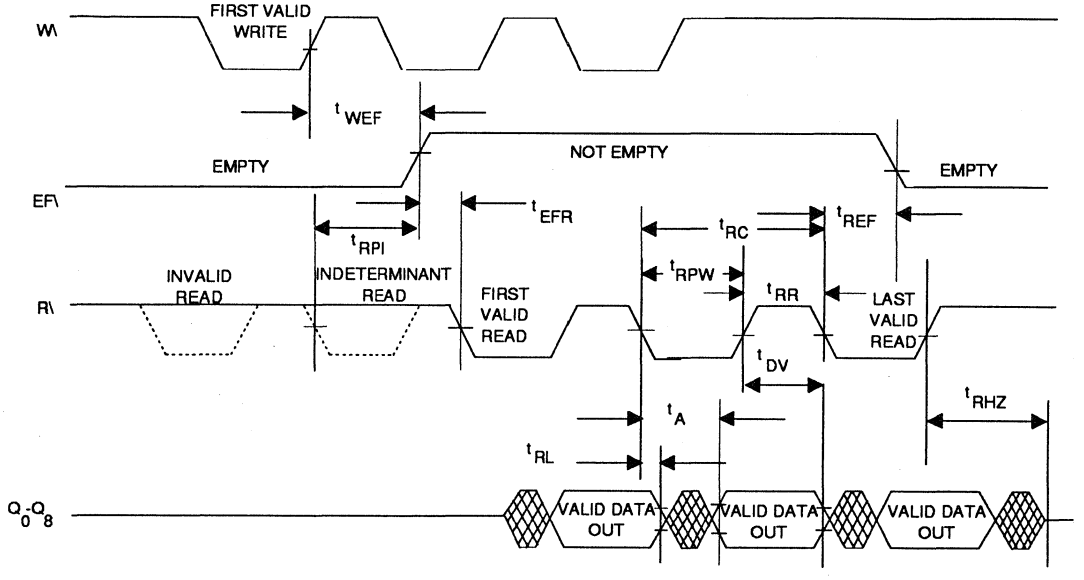
		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Write Cycle Time	t_{WC}	45		65		80		100		140		ns	
Write Pulse Width	t_{WPW}	35		50		65		80		120		ns	1
Write Recovery Time	t_{WR}	10		15		15		20		20		ns	
Data Setup Time	t_{DS}	15		20		25		30		40		ns	
Data Hold Time	t_{DH}	5		5		10		10		10		ns	
W\ Low to FF\ Low	t_{WFF}		30		45		60		70		110	ns	2
FF\ High to Valid Write	t_{FFW}		5		5		10		10		10	ns	2
R\ High to FF\ High	t_{RFF}		30		45		60		70		110	ns	2
Write Protect Indeterminant	t_{WPI}		15		20		25		25		35	ns	2

READ MODE

The DS2009 initiates a read cycle (see Figure 8) on the falling edge of Read Enable control input (R\), provided that the Empty Flag (EF\) is not asserted. In the read mode of operation, the DS2009 provides fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing write operations. After R\ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the EF\ will go low, and further read operations will be inhibited (the data outputs will remain in high impedance). EF\ will go high t_{WEF} after completion of a valid write operation. Reads beginning t_{EFR} after EF\ goes high are valid. Reads begun after EF\ goes low and more than t_{RPI} before EF\ goes high are invalid (ignored). Reads beginning less than t_{RPI} before EF\ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



READ AC ELECTRICAL CHARACTERISTICS

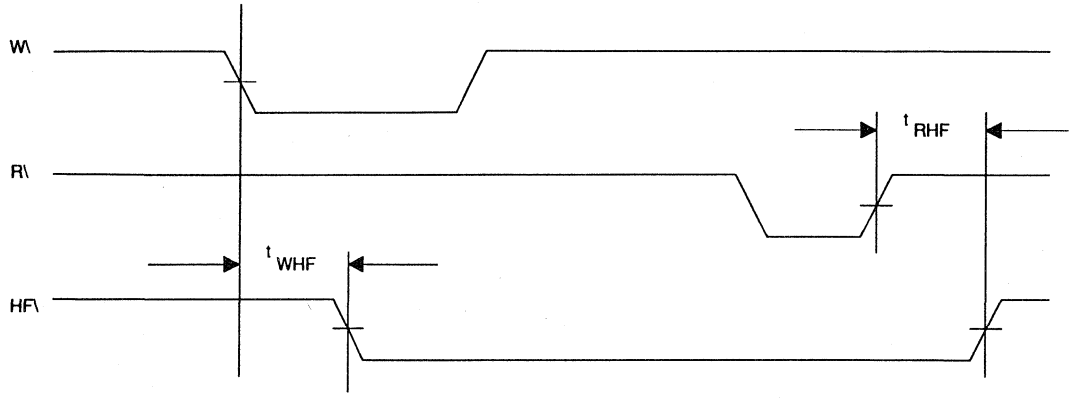
(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Read Cycle Time	t_{RC}	45		65		80		100		140		ns	
Access Time	t_{A}		35		50		65		80		120	ns	1
Read Recovery Time	t_{RR}	10		15		15		20		20		ns	
Read Pulse Width	t_{RPW}	35		50		65		80		120		ns	1
R\ Low to Low Z	t_{RL}	5		10		10		10		20		ns	2
Data Valid from R\ High	t_{DV}	5		5		5		5		5		ns	2
R\ High to High Z	t_{RHZ}		20		25		25		25		35	ns	2
R\ Low to EF\ Low	t_{REF}		30		45		60		70		110	ns	2
EF\ High to Valid Read	t_{EFR}		5		5		10		10		10	ns	2
W\ High to EF\ High	t_{WEF}		30		45		60		70		110	ns	2
Read Protect Indeterminant	t_{RPI}		15		20		25		25		35	ns	2

HALF-FULL MODE

Unlike the full and empty flags, the half-full flag does not prevent device reads and writes. This flag is set by the next falling edge of write when the memory is 256 locations full. The flag will remain set until the memory is less than or equal to 256 locations full. The read operation (rising edge), which results in the memory being 256 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



HALF-FULL FLAG AC CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

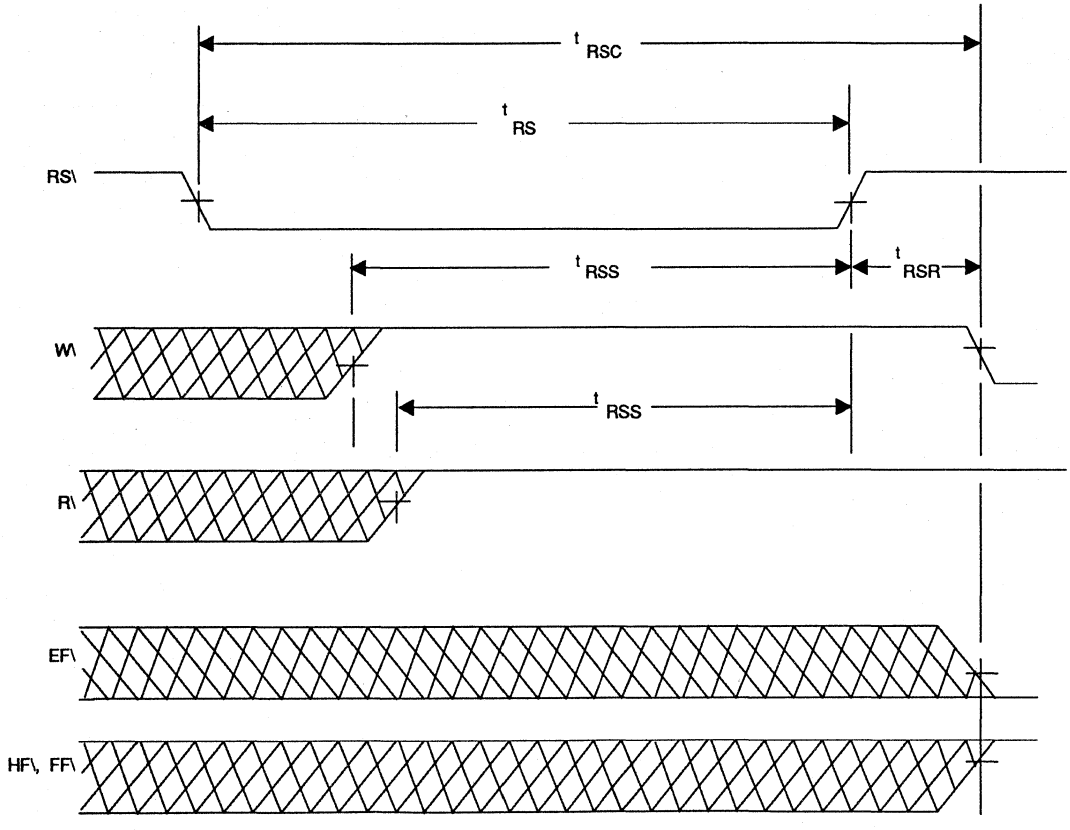
		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120		
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Write Low to Half-Full Flag Low	t_{WHF}		45		65		80		100		140	ns
Read High to Half-Full Flag High	t_{RHF}		45		65		80		100		140	ns

RESET

The DS2009 is reset (see Figure 10) whenever the Reset pin (RS\) is in the low state. During a reset, both the internal read and write pointer are set to the first location. Reset is required after a power-up before a write operation can begin.

Although neither W\ or R\ need be high when RS\ goes low, both W\ are R\ must be high t_{RSS} before RS\ goes high and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of FL\ /RT\ and XI\ during reset.

RESET Figure 10



NOTE:

EF\, FF\ and HF\ may change status during reset, but flags will be valid at t_{RSC}.

RESET AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Reset Cycle Time	t_{RSC}	45		65		80		100		140		ns	
Reset Pulse Width	t_{RS}	35		50		65		80		120		ns	1
Reset Recovery Time	t_{RSR}	10		15		15		20		20		ns	
Reset Setup Time	t_{RSS}	30		40		50		60		100		ns	2

RETRANSMIT

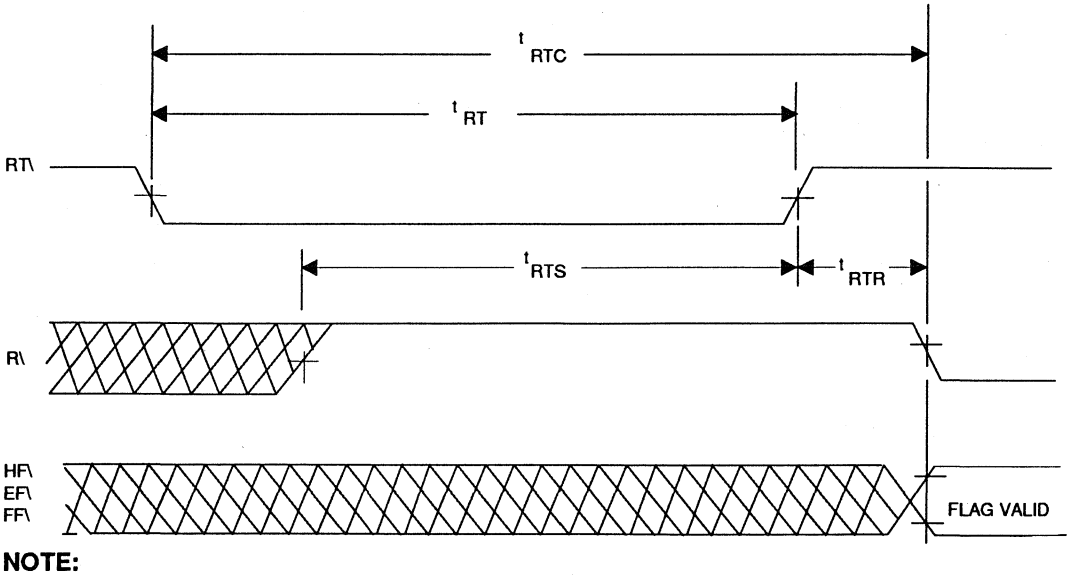
The DS2009 can be made to retransmit (re-read previously read data) after the Retransmit pin (RT\) is pulsed low (see Figure 11).

A retransmit operation sets the internal read pointer to the first physical location in the array but will not affect the position of the write pointer.

R\ must be inactive t_{RTS} before RT\ goes high and must remain high for t_{RTR} afterwards.

The retransmit function is particularly useful when blocks of less than 512 writes are performed between resets. The retransmit feature is not compatible with depth expansion.

RETRANSMIT Figure 11



NOTE:
EF\, FF\ and HF\ may change status during retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Retransmit Cycle Time	t_{RTC}	45		65		80		100		140		ns	
Retransmit Pulse Width	t_{RT}	35		50		65		80		120		ns	1
Retransmit Recovery Time	t_{RTR}	10		15		15		20		20		ns	
Retransmit Setup Time	t_{RTS}	30		40		50		60		100		ns	

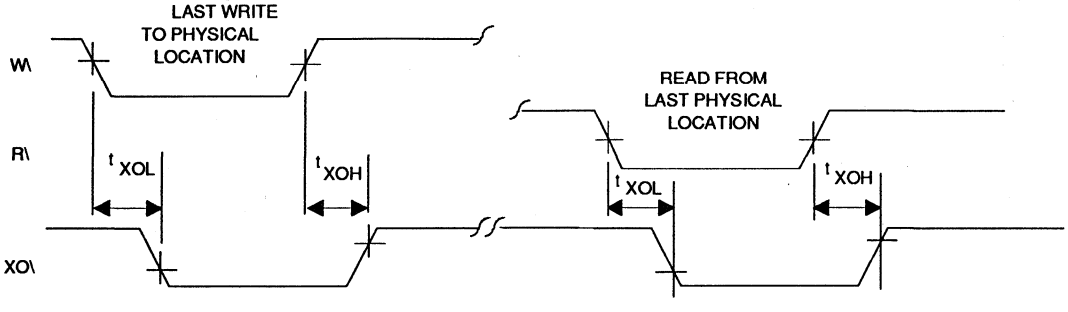
EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the expansion out and expansion in signals. Discussion of expansion out/expansion in timing is provided to clarify how depth expansion works. Inasmuch as expansion out pins are generally connected only to expansion in pins, the user need not be concerned with actual timing in a normal depth expanded application unless extreme propagation delays exist between the XO\ and XI\ pin pairs.

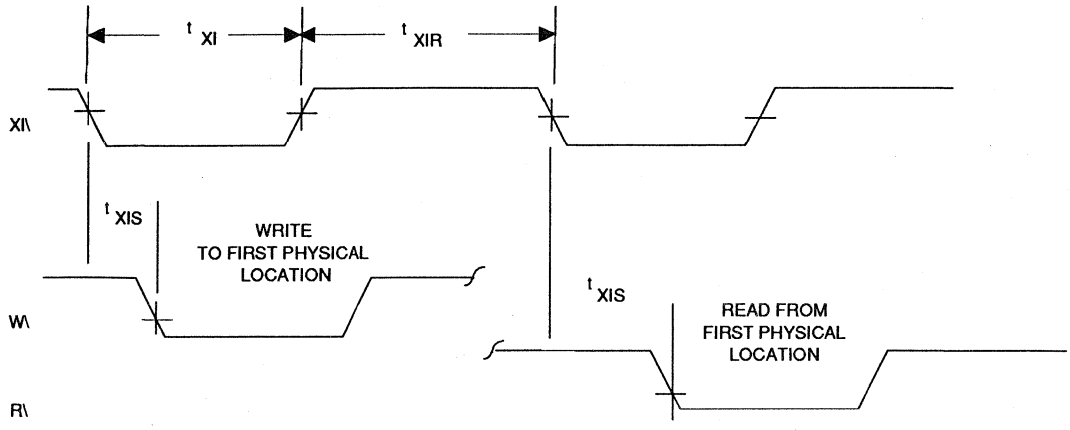
Expansion out pulses are the image of the write and read signals that cause them: delayed in time by t_{XOL} and t_{XOH}. The expansion out signal is propagated when the last physical location in the memory array is written and again when it is read (last read). This is in contrast to when the full and empty flags are activated, which is in response to writing and reading a last available location.

When in depth expansion mode, a given DS2009 will begin writing and reading as soon as valid write and read signals begin, provided FL was grounded at reset time. A DS2009 in depth expansion mode with FL\ high at reset will not begin writing until after an expansion in pulse occurs. It will not begin reading until a second expansion in pulse occurs and the empty flag has gone high. Expansion in pulses must occur t_{XIS} before the write and read signals they are intended to enable. Minimum expansion in pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
AC ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Expansion Out Low	t_{XOL}		30		45		55		70		100	ns	
Expansion Out High	t_{XOH}		30		45		55		70		100	ns	
Expansion In Pulse Width	t_{XI}	35		50		65		80		120		ns	1
Expansion In Recovery Time	t_{XIR}	10		15		15		20		20		ns	
Expansion In Set Up Time	t_{XIS}	15		20		25		30		40		ns	

AC TEST CONDITIONS:

Input Levels.....GND to 3.0V
Transition Times.....5ns
Input Signal Timing Reference Level.....1.5V
Output Signal Timing Reference Level.....0.8V and 2.2V
Ambient Temperature.....0°C to +70°C
V_{CC}.....5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	20 mA

*This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND		0		V	
Logic 1 Voltage All Inputs	V_{IH}	2.0		V_{CC}+0.3	V	3
Logic 0 Inputs	V_{IL}	-0.3		+0.8	V	3,4

DC ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	-1		1	uA	5
Output Leakage Current	I_{OL}	-10		10	uA	6
Output Logic 1 Voltage I_{OUT} =-1mA	V_{OH}	2.4			V	3
Output Logic 0 Voltage I_{OUT}=4 mA	V_{OL}			0.4	V	3
Average V_{CC} Power Supply Current-50ns, 65ns, 80ns, 120ns	I_{CC1}			80	mA	7, 9, 10
Average V_{CC} Power Supply Current -35ns	I_{CC1}			100	mA	7
Average Standby Current (R\=W\= RST\=FL\ /RT\=VIH)	I_{CC2}			8	mA	7
Power Down Current (All Inputs=V_{CC}-0.2V)	I_{CC3}			500	uA	7, 11

CAPACITANCE

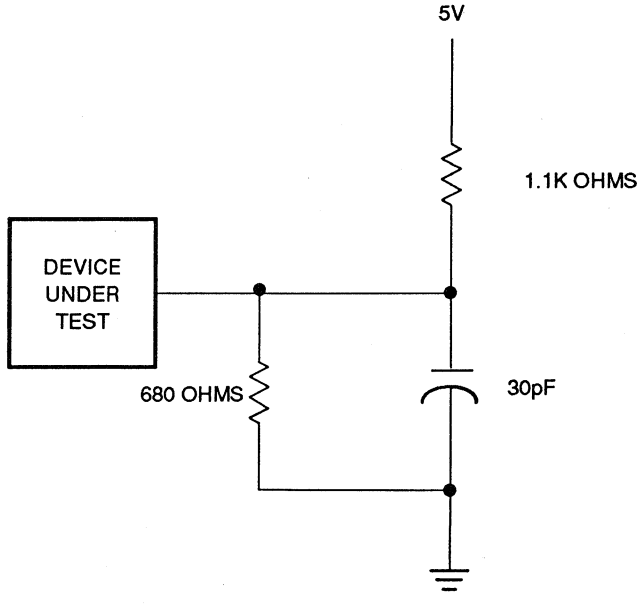
(t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	7	pF	
Capacitance on Output Pins	C_O	12	pF	8

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load diagram.
3. All voltages are referenced to ground.
4. -1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $R \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. DS2010, DS2011, DS2012, and DS2013 have I_{CC}, = 120 mA MAX for 50ns, 65ns, 80ns, and 120ns speed grades.
10. DS2009-N has I_{CC}, = 100mA MAX for 50ns, 65ns, 80ns, and 120ns speed grades.
11. DS2010 has I_{CC3} = 1mA MAX; DS2011, DS2012, DS2013 have I_{CC3} = 2mA MAX.

OUTPUT LOAD Figure 14



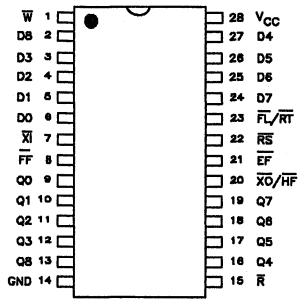
DALLAS SEMICONDUCTOR

DS2010
1024 x 9 FIFO Chip

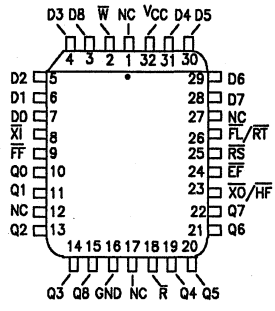
FEATURES

- First-in, first-out memory-based architecture
- Flexible 1024 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access times

PIN CONNECTIONS



DS2010 28-PIN DIP (600 mil)



DS2010R 32-PIN PLCC

PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
FL/RT	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
XI	- Expansion In
$\overline{XO}$/HF	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2010 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2010 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

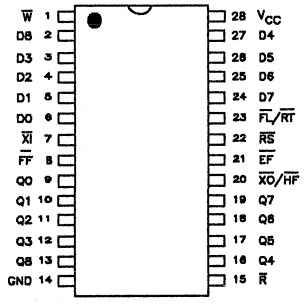
DALLAS SEMICONDUCTOR

DS2011
2048 x 9 FIFO Chip

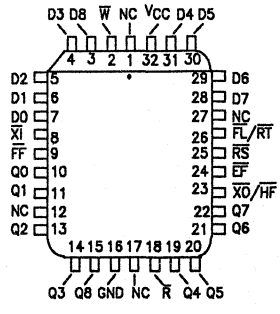
FEATURES

- First-in, first-out memory-based architecture
- Flexible 2048 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50ns, 65ns, 80ns, and 120ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50ns, 65ns, 80ns, and 120ns access times

PIN CONNECTIONS



DS2011 28-PIN DIP (600 mil)



DS2011R 32-PIN PLCC

PIN NAMES(\ Denotes Condition Low)

W\	-WRITE
R\	-READ
RS\	-RESET
FL\ /RT\	-First Load/Retransmit
D_{0-8}	-Data In
Q_{0-8}	-Data Out
XI\	-Expansion In
XO\ /HF\	-Expansion Out/Half Full
FF\	-Full Flag
EF\	-Empty Flag
V_{CC}	-5 Volts
GND	-Ground
NC	-No Connect

DESCRIPTION

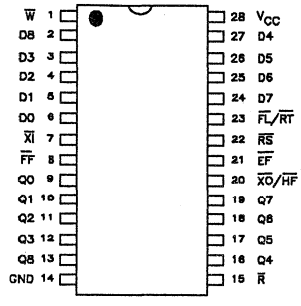
The DS2011 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2011 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

DALLAS SEMICONDUCTOR

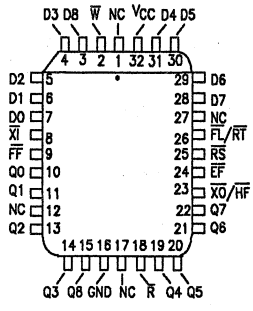
DS2012
4096 x 9 FIFO Chip

FEATURES
- First-in, first-out memory-based architecture
- Flexible 4096 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and120 ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

PIN CONNECTIONS



DS2012 28-PIN DIP (600 mil)



DS2012R 32-PIN PLCC

PIN NAMES (\ Denotes Condition Low)

W\	- WRITE
R\	- READ
RS\	- RESET
FL\ /RT\	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
XI\	- Expansion In
XO\ /HF\	- Expansion Out/Half Full
FF\	- Full Flag
EF\	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

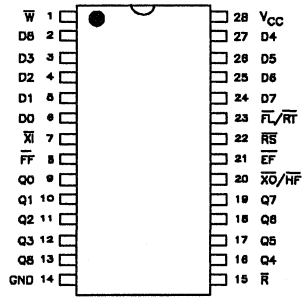
DESCRIPTION
The DS2012 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half full flags, and unlimited expansion capability in both word size and depth. The DS2012 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.

DALLAS SEMICONDUCTOR

DS2013
8192 x 9 FIFO Chip

FEATURES
- First-in, first-out memory-based architecture
- Flexible 8192 x 9 organization
- Low-power HCMOS technology
- Asychronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Industrial temperature range -40°C to +85°C available designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

PIN CONNECTIONS



DS2013 28-PIN DIP (600 mil)

PIN NAMES (\ Denotes Condition Low)

W\	- WRITE
R\	- READ
RS\	- RESET
FL\ /RT\	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
XI\	- Expansion In
XO\ /HF\	- Expansion Out/Half Full
FF\	- Full Flag
EF\	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION
The DS2013 8192 x 9 FIFO Chip implements a first-in, first-out algorithm, featuring asynchronous read/write operations, full, empty, and half-full flags, and unlimited expansion capability in both word size and depth. The DS2013 is functionally and electrically equivalent to the DS2009 512 x 9 FIFO with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to DS2009 512 x 9 FIFO Chip data sheet for detailed device description.

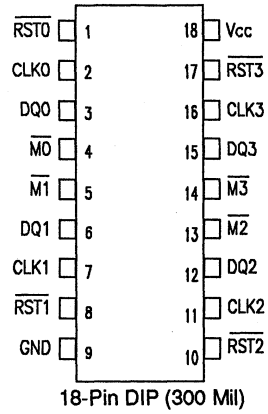
DALLAS SEMICONDUCTOR

DS2015
Quad Port Serial RAM Chip

FEATURES

- Four partitioned easy access ports
- No arbitration required
- Message flag for each port
- Low pin-count serial access
- Simultaneous multiport reads
- Message length of up to eight bytes
- Low-power CMOS
- Space saving 18-pin DIP
- Directly interfaces to the DS1206 Phantom Serial Interface Chip
- Provides a low cost interconnect for up to four microprocessor based systems

PIN CONNECTIONS



18-Pin DIP (300 Mil)

PIN NAMES (\ Denotes Condition Low)

RST0\-RST3\	Port 0 - Port 3 Reset
D/Q0-D/Q3	Port 0 - Port 3 Data I/O
CLK0-CLK3	Port 0 - Port 3 Clock
M0\-M3\	Port 0 - Port 3 Message Ready
GND	Ground
Vcc	+5 Volts

DESCRIPTION

The DS2015 Quad Port Serial RAM Chip is a low-cost device which can loosely couple up to four microprocessors or microcontrollers. Arbitration is handled by protocol and a message center which forces discipline and prevents collisions. Each port has access to all other ports for reading information and can write information only in its own memory area. The memory space for each port is 64 bits. Access to and from each port takes place over a three-wire serial bus. The serial bus keeps pin count low while affording sufficient bandwidth to accommodate loosely coupled system communication. Each port also has a message flag which can be used to warn of message ready conditions.

OPERATION

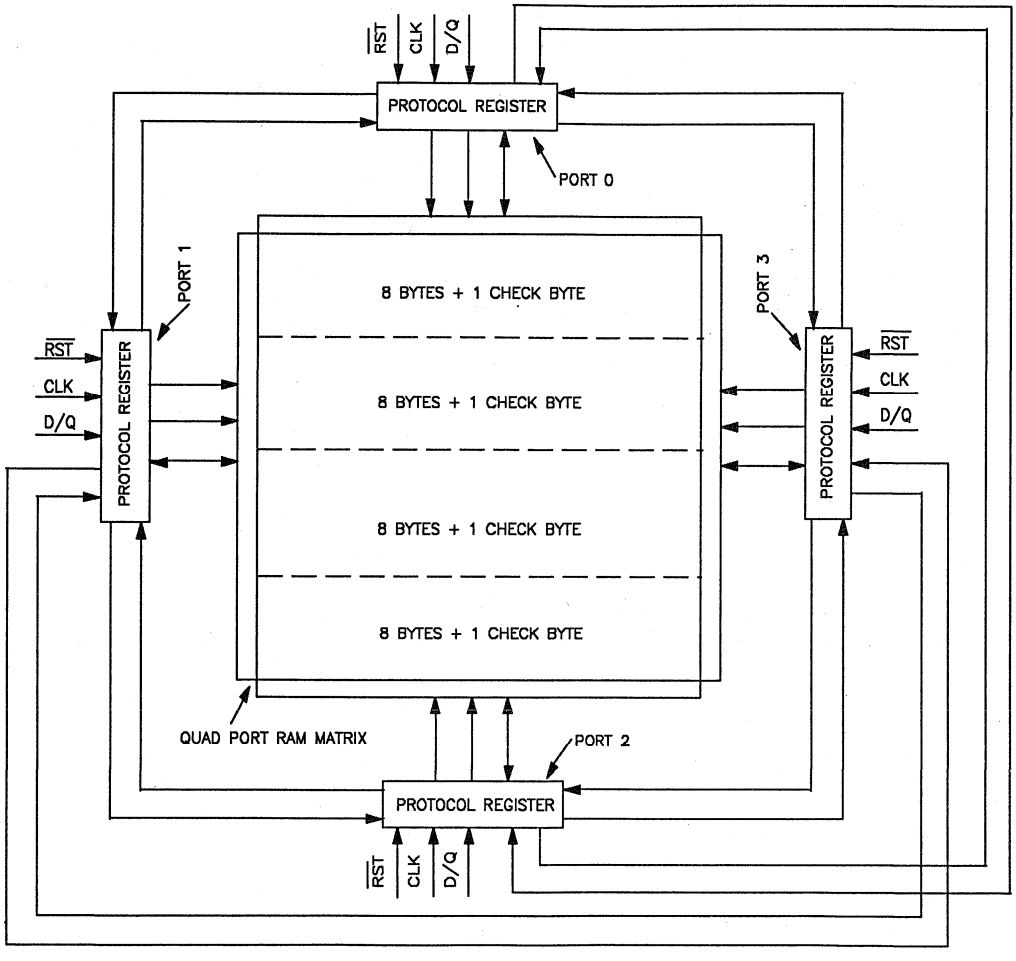
The DS2015 has four separate three-wire serial ports. Each port has direct read and write access to eight message bytes of RAM which are designated as belonging to that particular port. In addition, each port has read only access to three groups of eight message bytes, each of which are designated as belonging to the three other ports. Messages are sent between any port by reading and writing the eight message bytes of the four ports. An optional check byte is provided for each group of eight message bytes to verify data integrity (see Figure 1). All of the cells within the RAM matrix are quad-ported and can be read simultaneously from four different directions. This reduces arbitration to concerns of write operations only.

Each of the four three-wire serial ports contains a three-byte protocol register which defines access to the RAM, and sets the discipline which controls arbitration between the four ports.

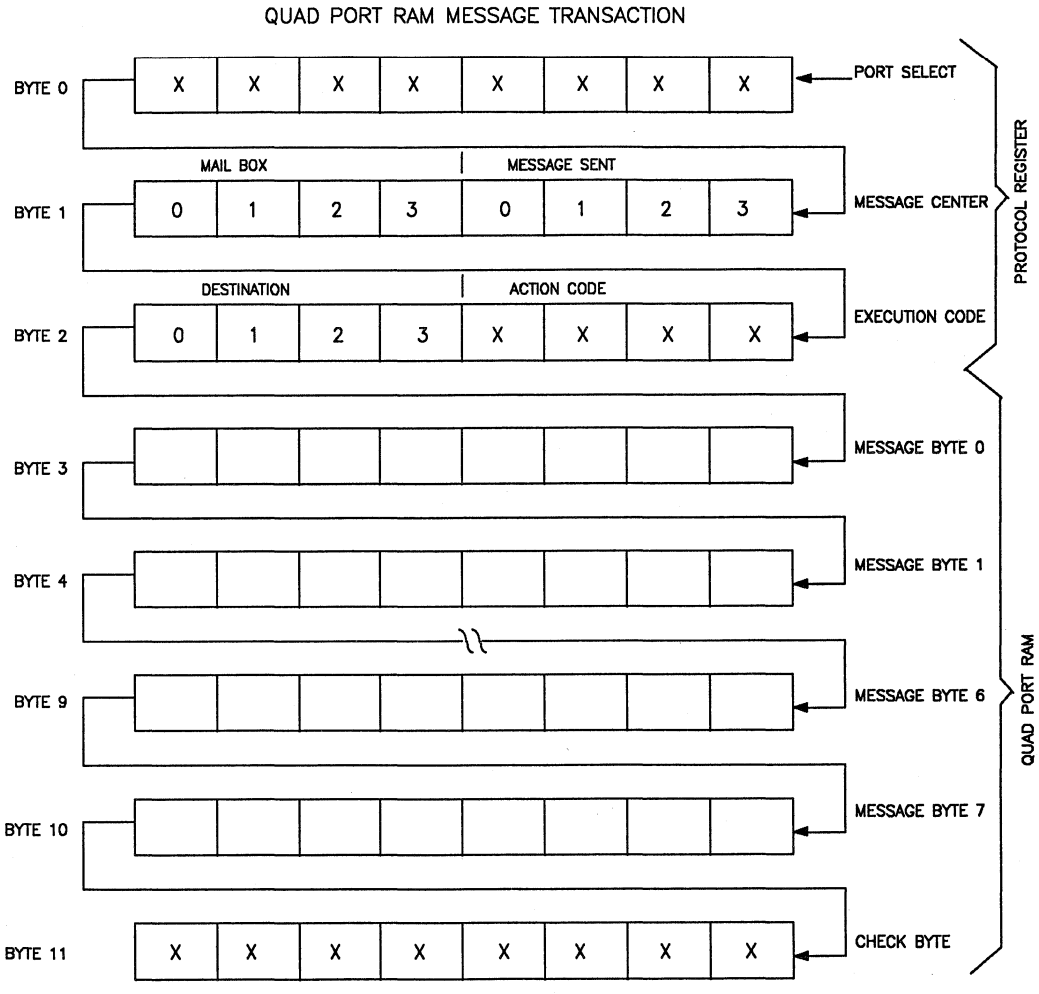
Protocol Register

The first byte of the protocol register is called the port select (see Figure 2). This byte contains an eight-bit pattern which must match the first 8 bits sent on an active port or any further activity will be ignored (Figure 3). A port is active when the reset line is inactive (high) and the CLK input is transitioning. The first eight bits are sent into a port on the D/Q line. The second byte of the protocol register contains eight bits of status information about activity on all four ports. This byte, called the message center, is read only and divided into two nibbles: messages sent and mailbox. The first four bits tell which messages the port has sent to other ports that have not been received. By reading these four bits, the inquiring port knows not to send new messages because all the receiving ports have not read to a previously sent message. Each message sent bit is cleared when the receiving port reads the last bit of its message or the RST\ input of the receiving port is driven low. The next four bits of the message center provide each port with the knowledge of pending messages which are ready for reading and the number of the port or ports which are sending the message(s). These bits are set by the destination bits of each port when a sending port finishes writing the last bit of a message. The mailboxes are read only bits. All message center bits are driven out on the DQ line while RST\ is inactive and the clock is transitioning. The third byte of the protocol register contains the execution code. The execution code byte is also divided into two four bit nibbles: the action code and the destination. This byte is write only and data is input on the D/Q line with RST\ inactive and the CLK input transitioning. The action code bits have only three patterns which will allow subsequent action to take place (Figure 3). An action code of four zeros (0000) calls for a read message action to occur in one of the four sections of the Quad Port RAM as specified by the destination bits. A read message can occur to only one port and, therefore, only one destination bit can be set for an action code of 0000. Once a destination bit is set, a complete message of eight bytes must be read in order to reset the message sent bit in the sending port's protocol register. An action code of a one and three zeros (1000) calls for a write message action to be performed. A write message can only be written in the section of the Quad Port RAM that is identified with the sending port. However, a message which is written by a sending port can be directed to one or more ports by the destination bits. The destination bits will cause the mailbox bits in the protocol register of each port which is to receive the message to be set to logic one as soon as the last bit of the message is written by the sending port. An action code of two ones and two zeros (1100) calls for a write message action to be performed with more data coming. This action code works exactly the same as a standard write message action with one exception. The check byte which follows an eight-byte mes-

QUAD PORT BLOCK DIAGRAM Figure 1

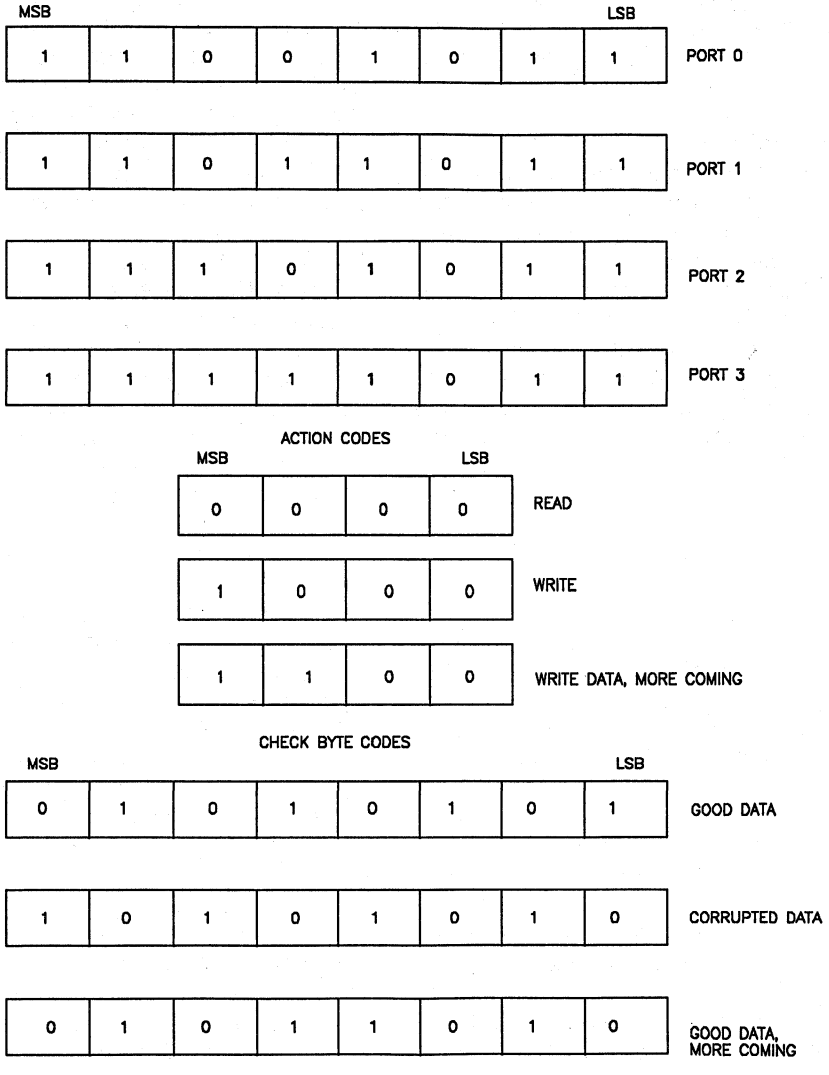


QUAD PORT RAM MESSAGE TRANSACTION Figure 2



NOTE: BITS WHICH ARE SET EQUAL LOGIC ONE.
BITS WHICH ARE CLEAR EQUAL LOGIC ZERO

PORT SELECT CODE Figure 3



sage is driven to a special code which, when read by a receiving port, indicates that more messages will be coming. This information can be used by a receiving port to reduce the overhead of constantly polling for new messages.

Quad Port RAM

As mentioned, each port has direct read and write access to eight message bytes and read access to three groups of eight message bytes. Once the protocol register has been correctly accessed, one of the four sections of the Quad Port will be read or that section of the Quad Port RAM which is dedicated to the transmitting port will be written. When sending a message, all eight message bytes must be written. When receiving a message, all eight of the message bytes should be read. If fewer than all eight bytes are accessed, the message centers may be incorrect and errant communications between ports can result.

Check Byte

A check byte (byte 11) is provided at the end of each of the eight message byte groups. The check byte is read only and provides information to a receiving port. Reading the check byte code is optional and may not be necessary in applications where software discipline is stringent enough to avoid accidental collisions between messages sent and messages received. Three different codes give status to a receiving port about the message which has just been read (Figure 3): good data, corrupted data, and good data with more data coming. When the check byte is read with a good data code, the data which is read by a receiving port is correct and valid. This check byte code assures the receiving port that a sending port is not writing a new message while the receiving port is attempting to read the previous message. When the check byte is read with a corrupted data code, the data which is read by a receiving port is suspect. This check byte warns the receiving port that the sending port is writing a new message while the receiving port is reading an older message. When the check byte is read with a good data and more coming code, the data which is read by a receiving port is correct and valid and additional messages will follow. This check byte code can be used by a receiving port to reduce the overhead of constant polling. If the check byte indicates that a new message will follow, the receiving port is warned to expect a new message.

Polling vs. Message Flags

The DS2015 Quad Port Serial RAM Chip has two methods of warning the sending and receiving ports of impending message status. The software method of polling avoids the complication of additional hardware which is required to connect the message ready pins to a host sending/receiving unit. Polling is accomplished with a receiving unit by satisfying the port select byte of the protocol register and reading the message center. When a port is being polled, care should be taken to avoid entering the execution code portion of the protocol register. When polling a port, communications can be terminated by taking the RST\ input signal low. An alternate method of alerting a host sending/receiving unit of impending message status is to use the message ready signals to interrupt when a message is ready to be read. The message ready pins (M0\-M3\) are driven to an active state (low) when a sending port has written the last bit of the eight message bytes and RST\ of the sending port is set to the inactive state (low), provided the appropriate destination bit is set. When the message ready pin is set to an active state, a receiving unit can execute a software routine to service the interrupt and read the pending message.

RST\ Control

All message transactions are initiated by driving the RST\ port input high. The RST\ input serves two functions. First, it turns on control logic which allows access to the protocol regis-

ter. Second, the RST\ signal provides a method of terminating message transfer. Care must be taken when terminating a message transfer to avoid errant information in the message center. The following rules will avoid all problems.

I. While polling the message center for new messages, always terminate the transaction by driving RST\ low after completing a read of the message center byte and before entering the execution code byte.

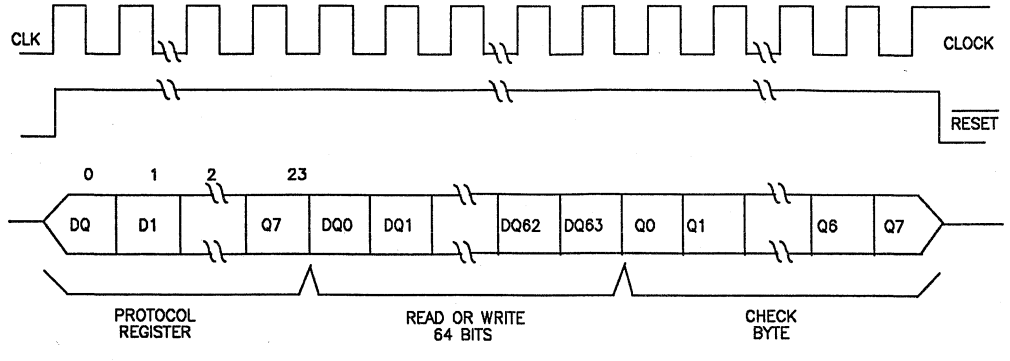
2. When sending a message, all eight messsage bytes must be written. If fewer than eight bytes are written, the mailbox bit of the destination port(s) may not be set and the check byte may indicate corrupted data.

3. When receiving a message, all eight bytes should be read. However, if RESET\ is used to terminate a message which is being read, the message sent bit and the mailbox bit are cleared as RST\ is driven low. When reading a message, the check byte is optional and can be either read or ignored.

Clock Control

A clock cycle is a sequence of a falling edge followed by a rising edge. For message inputs, the data must be valid during the rising edge of the clock cycle. Protocol bits and message bits are input on the rising edge of the clock. Protocol bits and message bits are output on the falling edge of the clock. All message transfer terminates if RST\ is low and the D/Q pins will then go to a high impedance state. When message transfer is terminated using RST\, the transition of RST\ must occur while the clock is at high level to avoid disturbing the last bit of data. Figure 4 illustrates message transfer.

QUAD PORT MESSAGE TRANSFER Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground: -1.0 to + 7.0V
Operating Temperature: 0°C to 70°C
Storage Temperature: -55°C to + 125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Logic 1	V_{IH}	2.0		Vcc+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	Vcc	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, Vcc = 5V+/- 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	uA	
Output Leakage	I_{LO}			1	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(t_A=25°C)

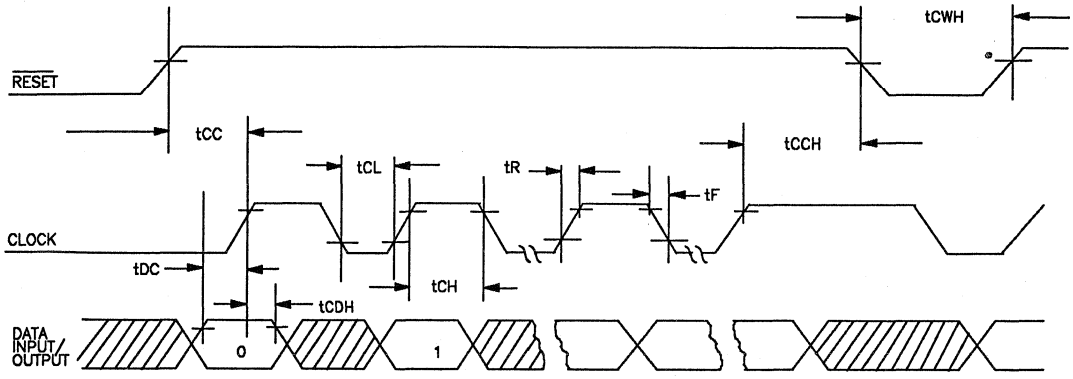
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

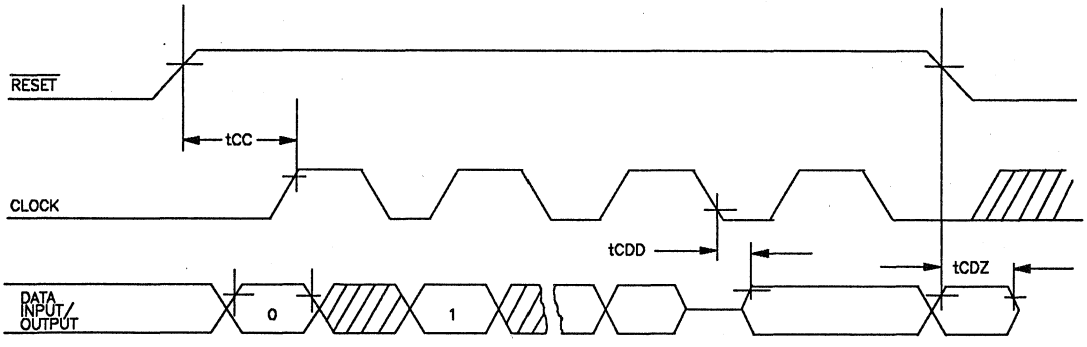
(0°C to 70°C, Vcc = 5V+/- 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	
CLK to Data Hold	t_{CDH}	40			ns	
CLK to Data Delay	t_{CDD}			125	ns	
CLK Low Time	t_{CL}	125			ns	
CLK High Time	t_{CH}	125			ns	
CLK Frequency	f_{CLK}	DC		4.0	MHz	
CLK Rise and Fall	t_R,t_F			500	ns	
RST\ to CLK Setup	t_{CC}	1			us	
CLK to RST\ Hold	t_{CCH}	40			ns	
RST\ Inactive Time	t_{CWH}	125			ns	
RST\ to I/O High Z	t_{CDZ}			50	ns	
RST\ to Message Ready	t_{RF}			100	ns	

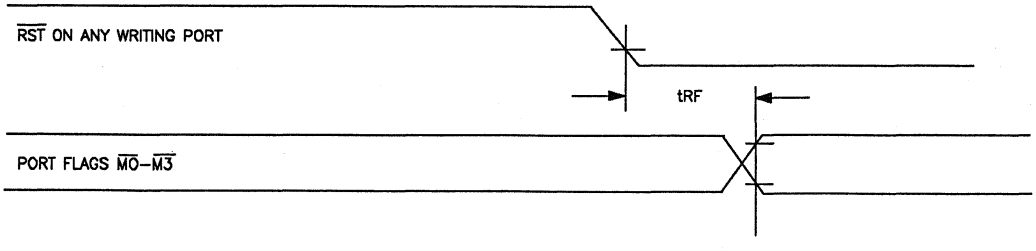
TIMING DIAGRAM-WRITE DATA TRANSFER Figure 5



TIMING DIAGRAM-READ DATA TRANSFER Figure 6



TIMING DIAGRAM-MESSAGE READY Figure 7



NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.

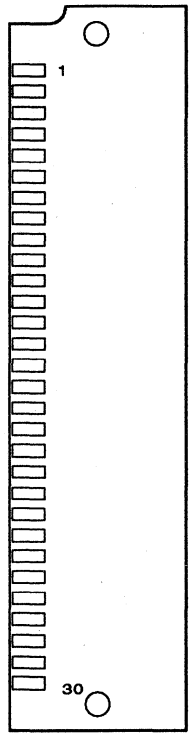
DALLAS SEMICONDUCTOR

DS2212
FIFO Stik

FEATURES

- First-in, first-out memory-based architecture
- Flexible 16384 x 9 organization
- Employs popular JEDEC standard 30-position SIMM connection scheme
- Low-power CMOS technology
- Self-contained logic provides composite full flag and empty flag
- Asynchronous and simultaneous read/write
- Available in 65 ns, 80 ns, and 120 ns access times
- Allows further depth expansion with additional units

PIN CONNECTIONS



30-Pin SIP Stik

DESCRIPTION

The DS2212 depth-expanded FIFO Stik provides a high density, high performance rate buffer for asynchronous data exchange applications. Composite full and empty flags prevent data overflow and underflow. The DS2212 contains 4 DS2012 4K x 9 FIFO circuits to provide a total of 16K x 9 of First-In, First-Out memory. Expansion-Out, Expansion-In, and First Load signals are also provided for further depth expansion.

PIN NUMBER	DESCRIPTION	SIGNAL	I/O
1,30	Power Input Pins	+ 5 Volts	Input
2,29	Power Ground	Ground	
3	Expansion Out	XO\	Output
4	Write Control Pin	W\	Input
13-5	DO-D8 Data In Pins	DO-D8	Input
14	Reset	RS\	Input
15	Empty Flag	EF\	Output
16	Full Flag	FF\	Output
17 - 25	QO - Q8 Data Out Pins	QO - Q8	Output
26	Read Pin	R\	Input
27	Expansion In	XI\	Input
28	First Load	FL\	Input

OPERATION

The DS2212 FIFO Stik employs a memory-based architecture wherein a byte written into the module is stored at a specific location where it remains until overwritten. This architecture is acheived by using four depth-expanded DS2012 4096 x 9 FIFO intergrated circuits. The memory-based architecture allows connection of the read/write, data in, and data out lines of the DS2012 FIFOs in parallel (Figure 1). Please review the DS2012 data sheet for all technical characteristics.

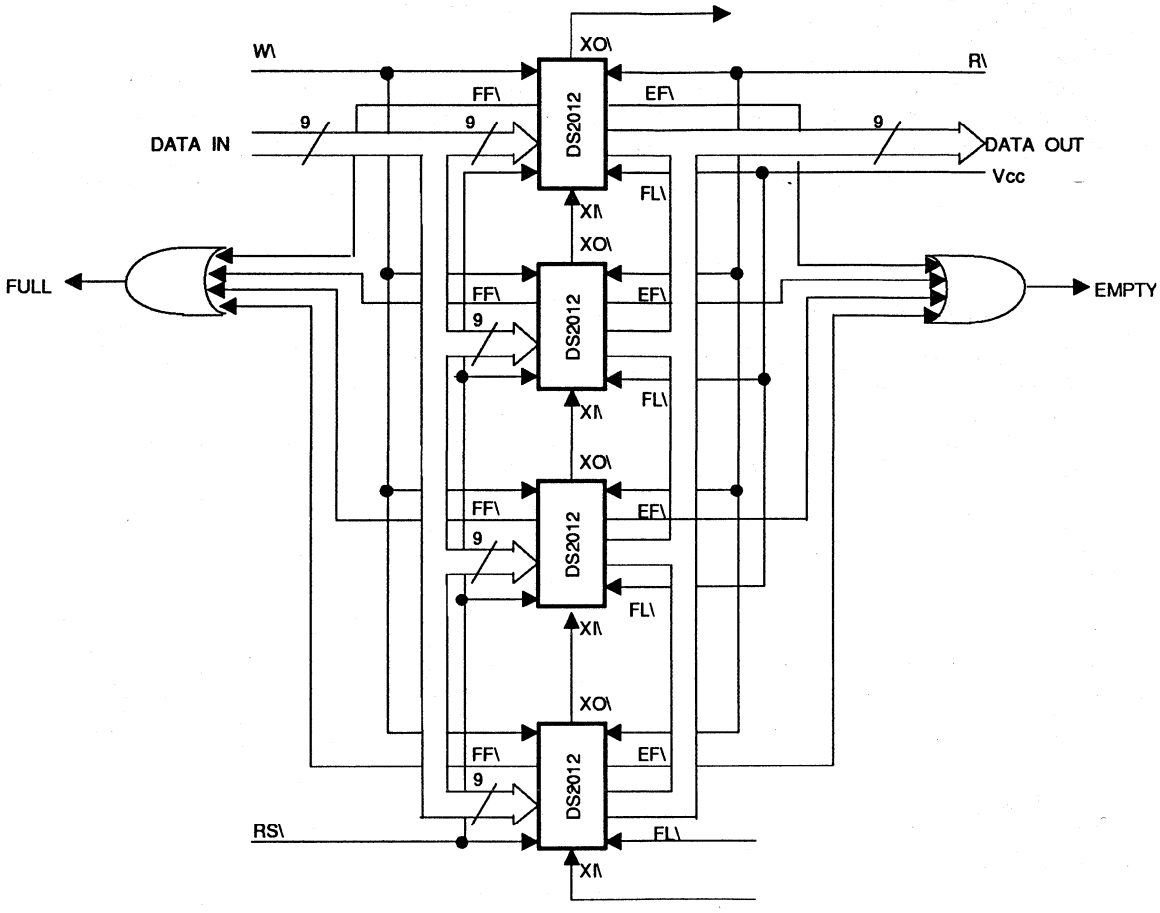
DEPTH EXPANSION

Further depth expansion capability is provided by the DS2212 using the Expansion-Out XO\, Expansion-In XI\, and the First Load FL signals. If two or more Stiks are required for further depth expansion, the XO\ pin of each Stik must be tied to the XI\ pin of the next Stik. The First Load FL\ pin of only one Stik in the array should be tied to ground. All other FL\ pins on other Stiks should be tied to V_{CC}. If only one Stik is required, the XI\ and XO\ pins should be tied together, and the FL\ pin should be grounded.

EMPTY AND FULL FLAGS

Composite empty flag FL\ and full flag FF\ signals are provided to prevent illogical operations. These status flags are composite in that they are created by ORing the EF\ and FF\ of each DS2012 4K x 9 FIFO on the Stik. This feature prevents reading of unwritten bytes (reading while empty) or overwriting unread bytes (writing while full). If two or more DS2212 FIFO Stiks are required for further depth expansion, the EF\ and FF\ outputs from the Stiks must be ORed by the user for proper operation. **NOTE:** EF\ and FF\ output signals will be pushed out by 10 ns maximum due to the propogation delay through the composite OR gates.

Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	0.5V to + 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Output Current per Pin	20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Ground	GND		0		V	
Logic 1 Voltage All inputs	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Voltage	V_{IH}	-0.3		+0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0° C to 70°C) (V_{CC}=5.0 volts +/-10%)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-4	4	uA	3
Output Leakage Current	I_{OL}	-40	40	uA	4
Output Logic1 Voltage I_{OUT}=-1mA	V_{OH}	2.4		V	1
Output Logic 0 Voltage I_{OUT}+4 mA	V_{OL}		0.4	V	1
Average V_{CC} Power Supply Current	I_{CC1}		150	mA	5
Average Standby Current (R\=W\=RS\=FL\ /RT=V_{IH})	I_{CC2}		50	mA	5
Power Down Current (All Inputs = V_{CC} -0.2V)	I_{CC3}		10	mA	5

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	30	pF	
Capacitance on Output Pins	C_O	50	pF	6

NOTES

1. All voltages are referenced to ground.
2. -1.5 volt undershoots are allowed for 10ns once per cycle.
3. Measured with $0.4 < V_{IN} < V_{CC}$.
4. $R > V_{IH}$, $0.4 > V_{OUT} < V_{CC}$.
5. I_{CC} measurements are made with outputs open.
6. With output buffer deselected.

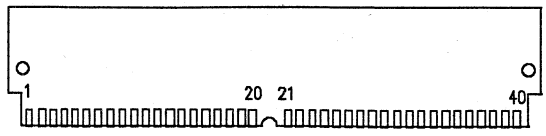
Microcontrollers

DALLAS SEMICONDUCTOR

DS2250
Soft Micro Stik

FEATURES
- Nonvolatile SRAM for program and/or data
- Capable of modifying its own program and/or data memory
- Program downloading via an on-chip, full-duplex serial port
- Adjustable partition between program and data memory
- Completely crashproof: program/data RAM and all data registers are maintained in absence of power
- All 32 port pins available for I/O
- Automatic restart on detection of errant software execution
- Orderly shutdown and automatic restart on power-up/down
- Program and data memory secure, with a tamper-proof, on-chip encryptor
- Compatible with industry standard 8051 instruction set
- DS2250T: Permanently powered clock/calendar
- 40-position SIMM connection scheme

PACKAGE OUTLINE



40-Pin SIMM

ORDERING INFORMATION

DS2250 XX – XX Soft Micro Stik
DS2250T XX – XX Time Micro Stik

Speed Grade

8	8 MHz
12	12 MHz
16	16 MHz

PROGRAM/DATA RAM

8	8 Kbytes
32	32 Kbytes
64	64 Kbytes

DESCRIPTION
The DS2250 Soft Micro Stik and DS2250T Time Micro Stik are the functional equivalents of the DS5000 Soft Microcontroller and DS5000T Time Microcontroller, respectively, with the exception that both devices are available with 64 Kbytes of nonvolatile memory. The pinout and instruction set of both products match the industry standard 8051 microcontroller. The DS2250 and DS2250T each plug into a SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles. For complete information, refer to the DS5000 Soft Microcontroller User's Guide.

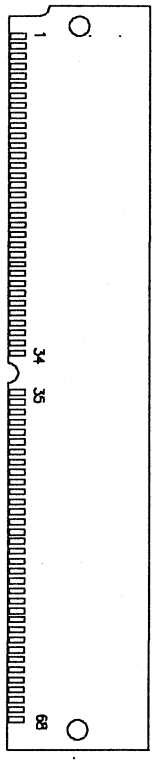
DALLAS SEMICONDUCTOR

DS2251
128K Micro Stik

FEATURES

- Up to 128K of nonvolatile SRAM onboard for program and data memory
- Bytewide address and data bus leaves port pins available
- Three peripheral enables memory map external devices onto the bytewide bus
- Reprogrammable peripheral controller (RPC mode) emulates 8042 for PC bus applications
- Optional DS1283 Watchdog TimeKeeper Chip allows wakeup from Stop mode (DS2251T)
- Flexible program loading from serial port or RPC mode peripheral bus
- Based on the DS5001FP Micro Chip
- 100% compatible with 8051 instruction set
- 68-pin SIMM connection scheme

PIN DESCRIPTION



68-Pin SIP Stik

DESCRIPTION

The DS2251 128K Micro Stik is a complete 8051-compatible microcontroller system, based on the enhanced DS5001FP 128K Micro Chip, in an extremely small form factor. The DS2251 supports all of the improved features that the DS5001FP offers over its DS5000 Soft Microcontroller predecessor, including expanded memory and I/O.

The DS2251 incorporates up to 128K bytes of nonvolatile RAM onboard, accessed by the DS5001FP's embedded address and data bus. The embedded bus is pinned out on the SIP edge connector as well as the four 8051-compatible ports. Additional I/O circuits can also be memory mapped onto the embedded bus by using the three peripheral enable signals. Four 8-bit ports remain available for other applications.

The Reprogrammable Peripheral Controller mode (RPC) brings the benefits of up to 128K nonvolatile RAM to the design of intelligent and flexible peripheral controllers through hardware emulation of the popular 8042 slave interface.

A permanently powered timekeeping feature that is the functional equivalent of the DS1286 Watchdog Timekeeper is incorporated into the DS2251T. This real time clock is driven by an internal quartz crystal and keeps time to a hundredth of a second. In addition, the date is automatically adjusted at the end of the month, including those months with less than 31 days. Leap year compensation is also performed automatically. Access to the timekeeping function is performed entirely on the DS5001FP's embedded address and data bus. As a result, none of the valuable I/O port resources are consumed in the interface. The timekeeper allows the processor to be reset at a pre-determined time via a user-programmable alarm. In this way, the processor can remain in an ultra-low power state until the wakeup time. A second interrupt which occurs at a user-defined periodic interval of up to 99 seconds is also available.

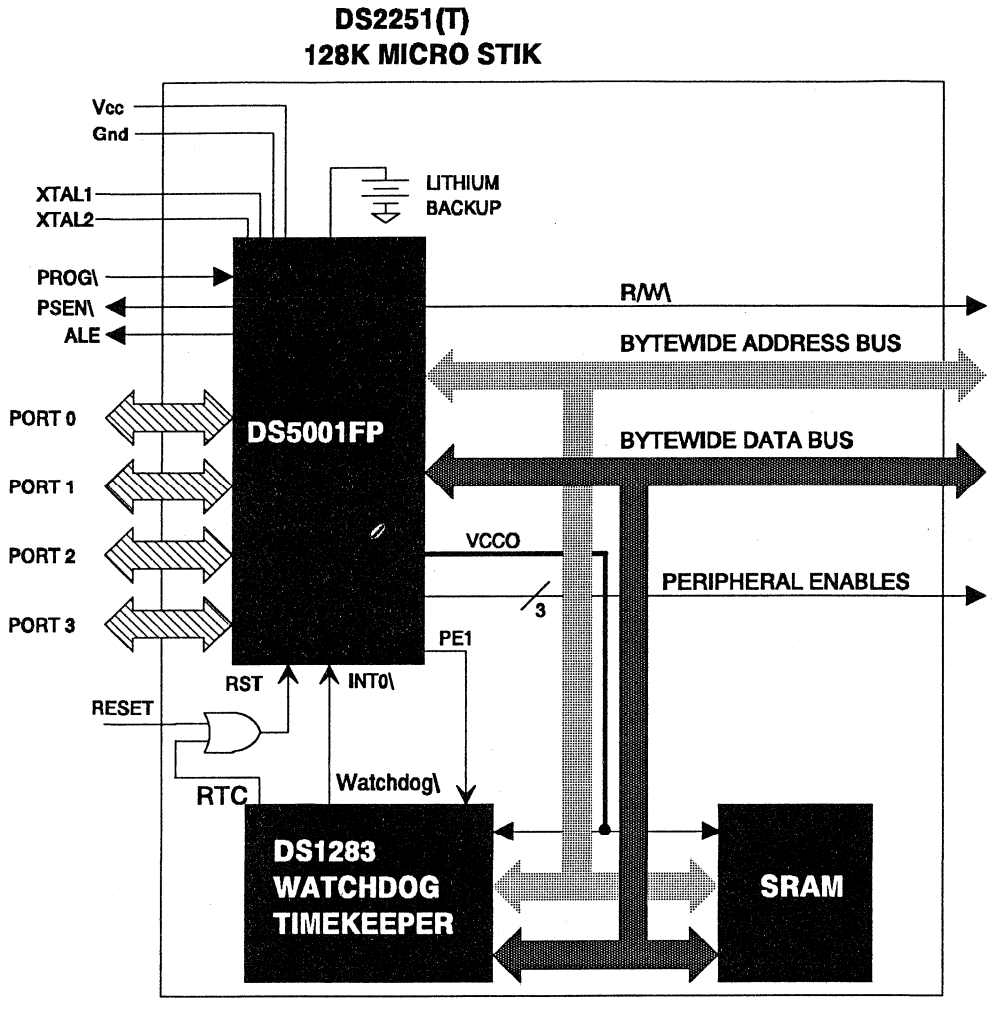
The DS2251 is designed to provide 10 years of timekeeping and data retention in its NV RAM, in the absence of V_{CC}. In addition, a user-programmable freshness seal is available to shut down lithium backup when it is not required.

ORDERING INFORMATION

Standard Configurations		
DS2251 08-08	128K Micro Stik	8K RAM 8 MHz
DS2251 32-12	128K Micro Stik	32K RAM 12 MHz
DS2251T 32-12	128K Micro Stik	32K RAM 12 MHz with Real Time Clock
DS2251T 64-12	128K Micro Stik	64K RAM 12 MHz with Real Time Clock
DS2251T 128-16	128K Micro Stik	128K RAM 16 MHz with Real Time Clock

Other versions are available by special order.

BLOCK DIAGRAM Figure 1



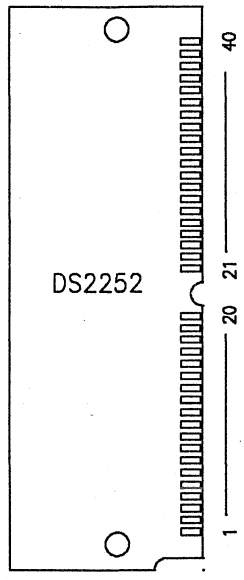
DALLAS SEMICONDUCTOR

DS2252
Secure Micro Stik

FEATURES

- Secure Micro Stik provides up to 128K bytes of lithium-backed NV SRAM for program/data storage
- Enhanced security features (over DS5000 Soft Microcontroller):
  - Stronger address/data encryptor
  - 64-bit encryption key word
  - Automatic true random key generation
  - SDI (Self-Destruct Input)
  - Top coating defeats microprobe attack
  - Customer-specific encryption versions available
- Reprogrammable Peripheral Controller (RPC) mode emulates 8042 for PC bus applications
- Optional DS1283 Watchdog Timekeeper Chip allows wakeup from Stop mode (DS2252T)
- 100% compatible with 8051 instruction set
- 40-pin SIMM connection scheme

PACKAGE OUTLINE



40-Pin SIP Stik

DESCRIPTION

The DS2252 Secure Micro Stik is a complete microcontroller subsystem based on the DS5002FP Secure Micro Chip and packaged in an extremely small form factor. The DS2252 incorporates the DS5002FP and, as a result, offers the most sophisticated security features available in any microcontroller.

The DS2252 incorporates up to 128K bytes of lithium-backed nonvolatile RAM onboard. This RAM is accessed by the DS5002FP's byte-wide bus and is used to store both program and data memory. The 128K byte NV SRAM can be initially loaded by the DS5002's on-chip bootstrap loader via the serial port and can be dynamically partitioned to fit changing program

and data storage requirements of a particular task.

The DS2252 offers all of the security features implemented within the DS5002FP. The entire 128K byte NV SRAM is stored and accessed in encrypted form, using the DS5002FP's advanced encryption algorithm. Customer-specific versions of the DS2252 are also available which incorporate one-of-a-kind encryption algorithms. An input to the DS5002FP's Self-Destruct Input pin is provided so that external detection circuitry can be used to trigger the erasure of the security lock in the event that an attempt is made to tamper with the system. When implemented as a part of a secure system design, the DS2252 can typically provide a level of security which requires more time and resources to defeat than it is worth to unauthorized individuals who have reason to try.

The DS2252 also incorporates the DS5002's Reprogrammable Peripheral Controller (RPC) mode which allows the DS2252 to perform peripheral tasks as a slave processor with a high-speed interface to a host system such as a PC bus. The RPC mode brings the benefits of up to 128K nonvolatile RAM to the design of intelligent and flexible peripheral controllers through hardware emulation of the popular 8042 slave interface.

A permanently powered timekeeping feature, which is the functional equivalent of the DS1286 Watchdog Timekeeper, is available as an option (DS2252T). This real time clock is driven by an internal quartz crystal and keeps time to a hundredth of a second. In addition, the date is automatically adjusted at the end of the month, including those months with fewer than 31 days. Compensation is also performed automatically for a leap year. Access to the timekeeping is performed entirely on the DS5002FP's bytewide bus. As a result, none of the valuable I/O port resources are consumed in the interface. The timekeeper allows the processor to be reset at a pre-determined time via a user programmable alarm. In this way, the processor can remain in an ultra-low power state until the wakeup time. A second interrupt which occurs at a user defined periodic interval (up to 99 seconds) is also available.

The DS2252 is designed to provide 10 years of timekeeping and data retention in its NV RAM, in the absence of V_{CC}. In addition, a user-programmable freshness seal is available to shut down lithium backup when it is not required.

FOR FURTHER INFORMATION

Consult the DS5002FP data sheet for further information on the Secure Micro Chip. Complete data sheets for both the DS2252 and the DS5002FP are available on request to customers who have a signed non-disclosure agreement on file with Dallas Semiconductor.

ORDERING INFORMATION

The following versions of the DS2252 are available as standard products from Dallas Semiconductor.

DS2252 08-08	Secure Micro Stik - 8K RAM 8 MHz
DS2252 32-12	Secure Micro Stik - 32K RAM 12 MHz
DS2252T 32-12	Secure Micro Stik - 32K RAM 12 MHz with Real Time Clock
DS2252T 64-12	Secure Micro Stik - 64K RAM 12 MHz with Real Time Clock
DS2252T 128-16	Secure Micro Stik - 128K RAM 16 MHz with Real Time Clock

Other versions are available by special order. Please contact Dallas Semiconductor for ordering information on customer-specific versions of the DS2252.

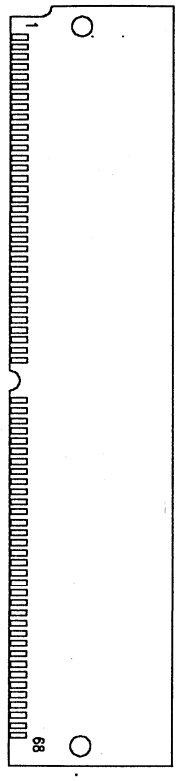
DALLAS SEMICONDUCTOR

DS2255
Instrumentation Stik

FEATURES

- Complete 12-bit A/D with:
  - Built-in high accuracy reference
  - 8-channel input
  - Digitally controlled channel selection
  - 8-bit analog gain and offset adjustment
  - 50 KHz maximum throughput rate
- D/A Features:
  - 8-bit resolution
  - 8 independent analog outputs
  - Each channel has an independent voltage range
- Addressable serial interface for simple software control of all functions
- External A/D clock input provides throughput flexibility
- Based on the DS1267 Dual Digital Potentiometer Chip for low-noise operation
- Interfaces to DS2251 and DS2256 Micro Stiks
  Single +5V supply
- Applications include:
  - Hands-off data acquisition
  - Real-time gain control
  - Software-controlled instrumentation
  - Feedback control
  - Teleservicing

PIN DESCRIPTION



68-Pin SIP Stik

DESCRIPTION

The DS2255 Instrumentation Stik is a complete data acquisition subsystem for microcontroller-based systems. When used in conjunction with a DS2251 128K Micro Stik or DS2256 Power Miser Micro Stik, the benefits of a crashproof nonvolatile system are delivered on an instrumentation platform. Such benefits can include storage of gain settings which calibrate an individual system and a history of sensor readings used for remote troubleshooting.

The DS2255 Instrumentation Stik provides eight

analog inputs with onboard signal conditioning which are digitized to 12 bits. Each channel has an independent, programmable analog gain and offset implemented via the DS1267 Dual Digital Potentiometer Chip. Each gain and offset can be adjusted in real time by an 8-bit potentiometer command word. This signal conditioning technique provides more flexibility than a programmable gain amplifier and substantially improved noise performance compared with other digital potentiometers.

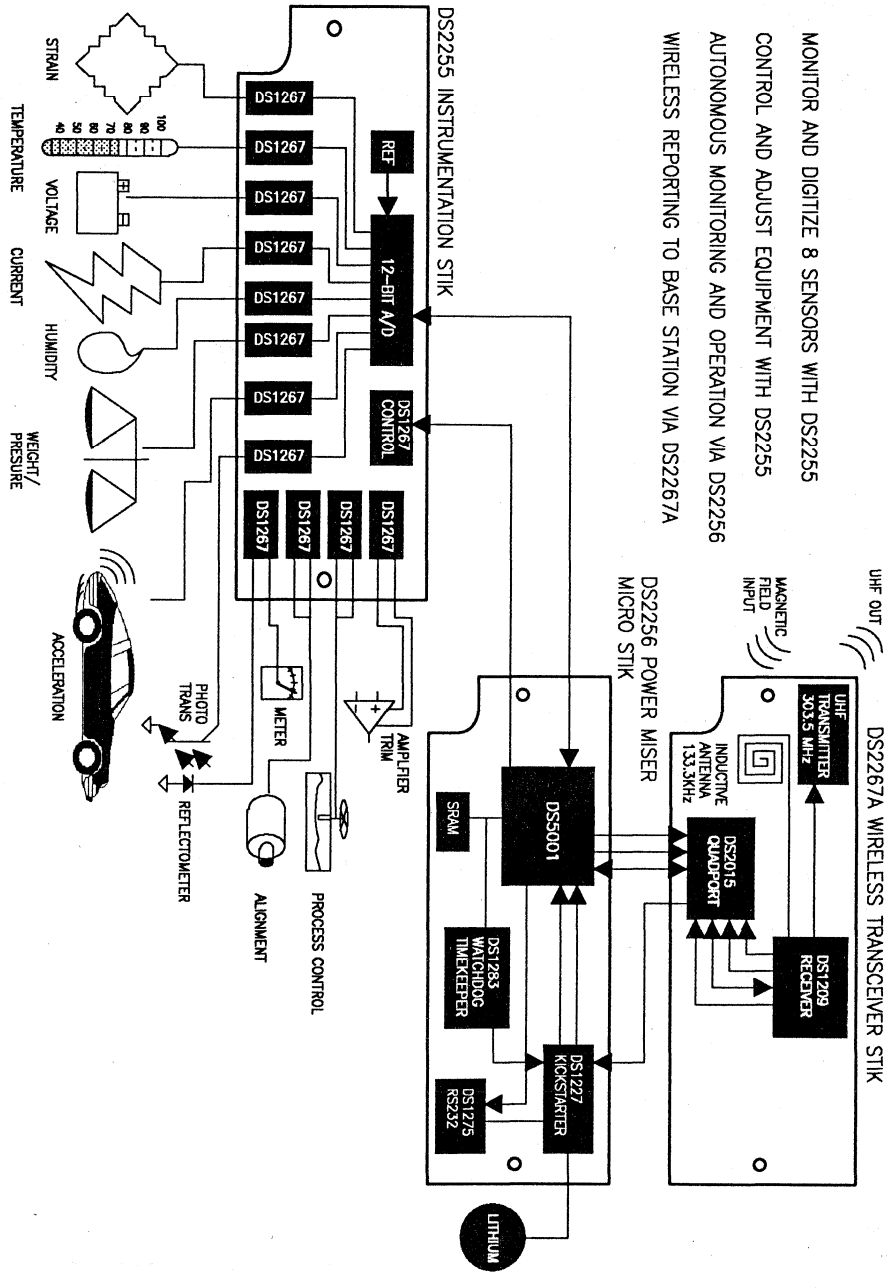
Eight independent analog outputs are available, each with a user-determined voltage range and 8-bit resolution. Since these analog outputs are also implemented via the DS1267, the Instrumentation Stik allows remote adjustment of equipment via a microcontroller and an RS232 link or a modem.

In a typical application, a nonvolatile microcontroller would determine the potentiometer settings for calibrated operation, store them, and then initialize each channel on power-up. Data I/O, gain, and offset command words are communicated by an addressable serial interface for ease of use in a microcontroller application. The entire subsystem can be powered off +5V or +/-5V. An onboard precision reference is included to allow high accuracy 12-bit A/D conversion.

ORDERING INFORMATION

DS2255-12 Instrumentation Stik

TYPICAL APPLICATION: BUTTONLESS INSTRUMENT Figure 2



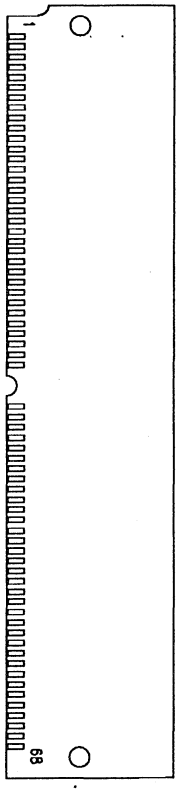
DALLAS SEMICONDUCTOR

DS2256
Power Miser Micro Stik

FEATURES

- Complete system core for remote or handheld instrument applications:
  - Buttonless execution of low-power microcontroller tasks
  - Data recording with time stamp and date
  - Sensor processing with DS2255 Instrumentation Stik
- Based on the DS5001FP 128K Micro Chip
- Includes up to 128K bytes of nonvolatile CMOS SRAM for program/data storage
- Permanently powered timekeeping and periodic interval alarms with the DS1283 Watchdog Timekeeper Chip
- Kickstarts system power in response to external events such as:
  - Sensor trip (e.g., photodiode)
  - Clock/calendar alarm
  - Any low-level logic signal
  - Incoming RS-232 activity
- Power conservation with Microenergy Management of the DS1227 Kickstarter Chip
- Complete +5V regulated power supply accepts +3V input
- Switchable auxiliary power supply output lines for external circuits
- 29 bits of user-definable port I/O
- Bytewide address and data bus for memory-mapped peripheral circuits
- 68-pin SIMM connection scheme

PACKAGE DESCRIPTION



68-Pin SIP Stik

DESCRIPTION

The DS2256 Power Miser Micro Stik provides the lowest power microcontroller solution for remote or handheld instruments. Designed as a complete core which serves all of the basic requirements of such applications, it includes a microcontroller, nonvolatile memory, timekeep-

ing, and I/O functions which are commonly required in an instrument. Power management and kickstarting features allow buttonless operation in remote systems, and maximize the life of a power source when an operator interface is required. A block diagram of the system is shown in Figure 1.

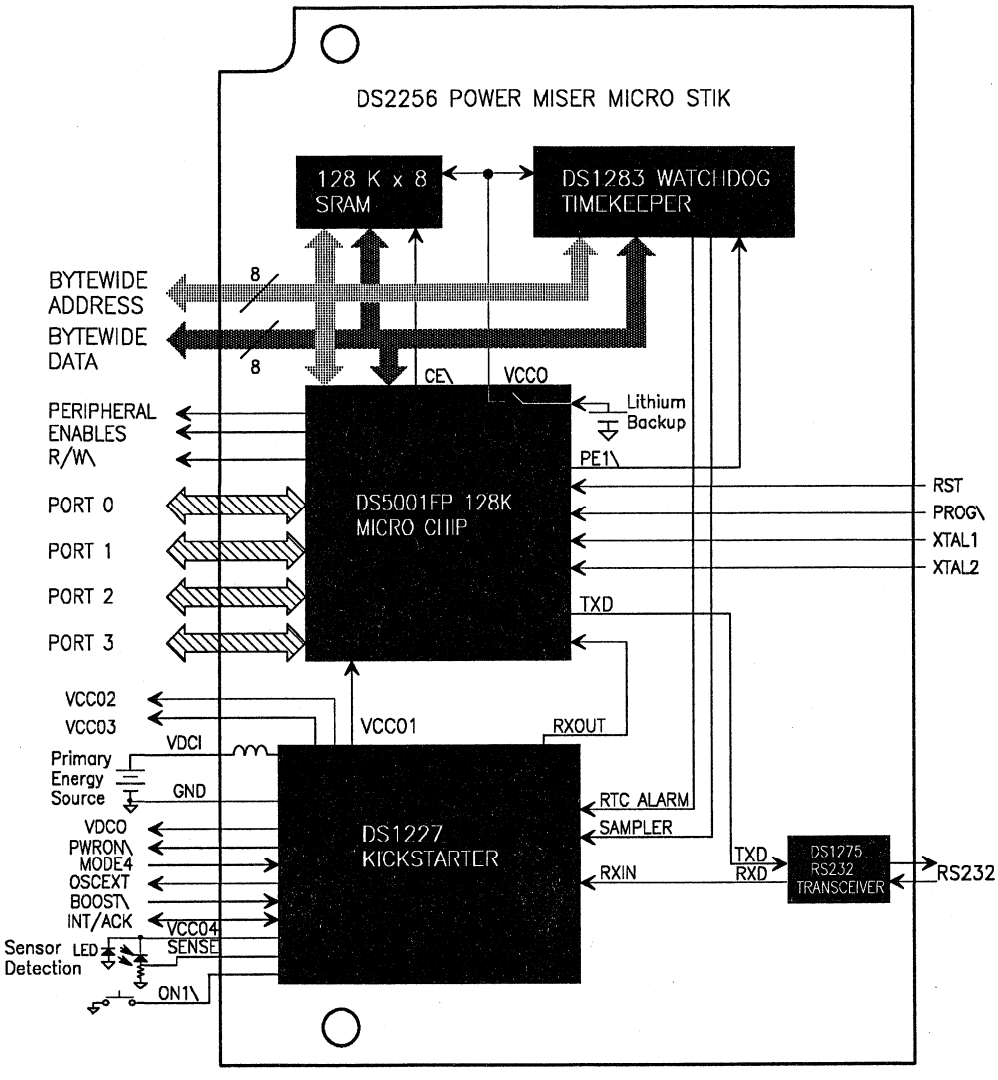
The DS2256 delivers unprecedented end-system flexibility by incorporating the DS5001FP 128K Micro Chip. Unlike rigid ROM or EPROM-based microcontrollers, all of the Micro Chip memory is flexible, read/write, and nonvolatile for more than 10 years. The DS5001FP is equipped with up to 128K bytes of nonvolatile SRAM which can be used for program and data storage requirements. A major benefit resulting from its RAM architecture is that the DS5001FP allows program memory to be changed at any time, even after the device has been installed in the end system. An onboard, line-powered RS232 transceiver allows serial bootstrap loading of the application software, as well as direct communication with a host PC by the instrument.

A permanently powered timekeeping feature, which is the functional equivalent of the DS1286 Watchdog Timekeeper, is incorporated into the DS2256. This real time clock is driven by an internal quartz crystal and keeps time to a hundredth of a second. In addition, the date is automatically adjusted at the end of the month, including those months with fewer than 31 days. Leap year compensation is also performed automatically. Access to the timekeeping is performed entirely on the DS5001FP's bytewide address and data bus. As a result, none of the valuable I/O port resources are consumed in the interface. The timekeeper allows the system to be powered up at a pre-determined time via a user programmable alarm. In this way, the instrument remains in an ultra-low power state until the "wakeup time". A second interrupt which occurs at a user defined periodic interval is also available.

Achieving the lowest power operation requires more sophistication than simply using low-power CMOS circuits. To minimize the operating current profile, the Power Miser Micro Stik incorporates the DS1227 Kickstarter circuit. Using its integral DC-DC converter, the DS1227 provides +5V to the onboard components from a +3 volt external power source. In +5V or +6V supply systems, the DC-DC converter can be bypassed. Most importantly, the DS1227 gives the DS2256 the ability to wake up from an ultra-low power retention state, perform a task, and then go back to sleep until the next task needs to be processed. This wakeup, or kickstarting action, can be performed in response to practically any type of low-level stimulus such as an incoming logic signal, RS232 data, or an alarm from the onboard clock/calendar. The DS5001FP can then instruct the Kickstarter to switch on (and off) two external power lines for user circuitry. When a task is complete, the DS5001FP can power itself down via the Kickstarter. In this manner, power can be selectively applied to different sections of circuitry for only the amount of time that their function is required. By reacting to its environment, the DS2256 facilitates "buttonless" instrument operation free of human intervention, and consequently uses less power. This micro-energy management technique allows the life of a primary power source to be maximized by minimizing the time when operating power is consumed.

Application flexibility is further enhanced by the substantial I/O resources of the DS2256. Twenty-nine port pins are provided for user-definable I/O functions. These are identical in function to those provided by the DS5001FP (or 8051). Although the DS5001FP has 32 port pins, three are committed to onboard functions. In addition, the embedded address and data bus is available for memory mapped control of external peripherals.

DS2256 BLOCK DIAGRAM Figure 1



ORDERING INFORMATION

Standard Configurations

DS2256-08-08	Power Miser Micro Stik	8K RAM 8 MHz
DS2256-32-12	Power Miser Micro Stik	32K RAM 12MHz
DS2256-64-12	Power Miser Micro Stik	64K RAM 12 MHz
DS2256-28-16	Power Miser Micro Stik	128K RAM 16 MHz

Other versions are available by special order.

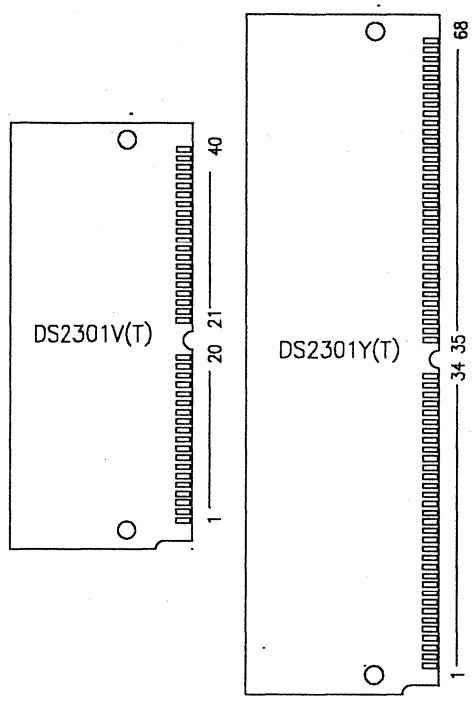
DALLAS SEMICONDUCTOR

DS2301
Soft 6301 Stik

FEATURES

- 630x subsystems adapt to task-at-hand:
  - -Up to 64K bytes of NV SRAM for program/data
  - -Serial bootstrap loading of software
  - -Code can be changed in end use
- Executes standard 6801 instruction set
  - -Incorporates Hitachi HD6303Y
  - -Two timer/counters: 16-bit and 8-bit
  - -Async/sync serial I/O
  - -Low power consumption modes
- Crashproof operation during transient conditions
- Enhanced I/O ports:
  - -DS2301V: 4 ports with 8 interrupt inputs
  - -DS2301Y: 7 ports with 8 interrupt inputs and Dual Port Register File
- Retrofitable SIMM connection scheme:
  - -DS2301V 40-pos. retrofits HD6301V
  - -DS2301Y 68-pos. retrofits HD6301Y
  - -SIMM to DIP adapters available
- DS1283 Watchdog Timekeeper Chip option available

PACKAGE OUTLINE



DESCRIPTION

The DS2301 Soft 6301 Stiks provide the benefits of adaptability, crashproof operation, and retrofit capability with enhanced I/O for the industry-standard 630x microcontroller architecture.

The DS2301V offers a total of four parallel I/O ports, two of which offer extended I/O capabilities that are not available with 630x series components. One of these extended ports allows each pin to serve as an interrupt input. The other extended port can be configured as a true bidirectional port or as a quasi-bidirectional port. The DS2301Y offers three additional I/O ports (for a total of seven). Two of these additional ports can be configured as a high-speed interface to allow the Soft 6301 Stik to act as a peripheral controller in a multiprocessor system.

With minimal software adjustment, the DS2301V and DS2301Y can be used to retrofit

into sockets designed to accept the popular HD6301V0 and HD6301Y0 devices, respectively. SIMM to DIP adapters are available to support this retrofit capability.

The DS2301VT and the DS2301YT provide the additional feature of a permanently powered real time clock/calendar. This feature is provided with the addition of a DS1283 Watchdog Timekeeper circuit. These Soft 6301 Stiks keep track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years. The DS1283 is parallel-accessed by the processor and is powered by the onboard lithium cell for greater than 10 years of timekeeping in the absence of V_{CC}.

Throughout this data sheet, when features are discussed that apply to all versions of the Soft 6301 Stik, the designation DS2301 will be used. When features are discussed which apply to both the time and non-time versions of the DS2301V and DS2301Y, these are referred to as the DS2301V(T) and DS2301Y(T), respectively. Therefore, DS2301V(T) is a generic reference to both the DS2301V and DS2301VT, while DS2301Y(T) refers to both the DS2301Y and DS2301YT.

DS2301 BLOCK DIAGRAM

Figure 1 is a block diagram which is applicable to all versions of the DS2301. All versions incorporate the HD6303Y and the DS5303 6303 Softner Chip.

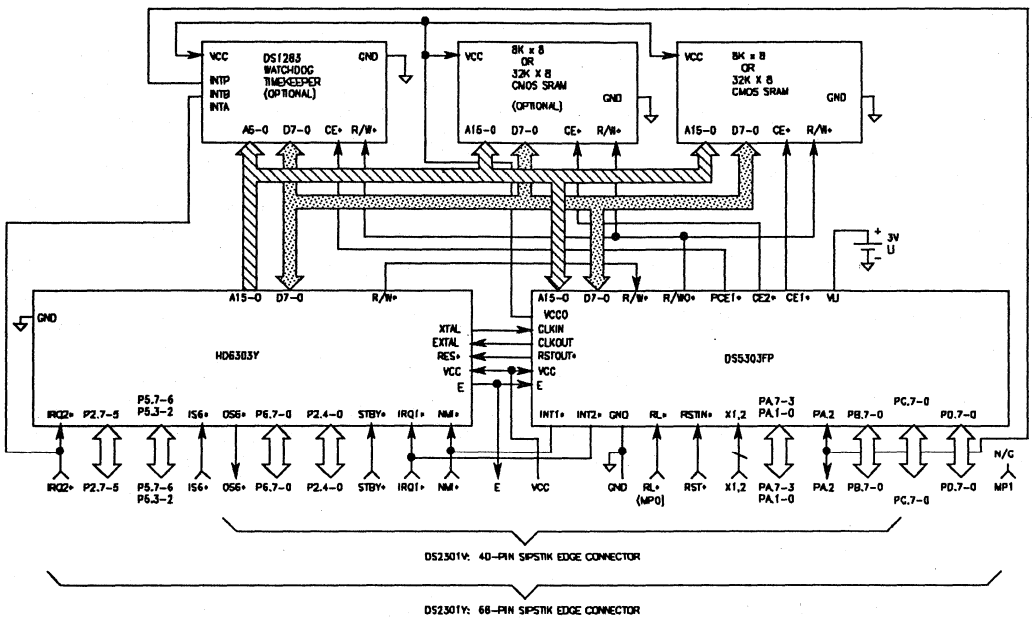
A standard Hitachi HD6303Y is the microprocessor. This component provides the CPU along with basic I/O functions.

The Dallas Semiconductor DS5303 6303 Softener Chip together with an onboard lithium energy source provides crashproof control for up to a full 64K bytes of CMOS SRAM, converting it into nonvolatile storage for program and data. In addition, the Softener Chip provides bootstrap loading and program/data partitioning of the NV SRAM. Finally, it provides a clock oscillator, extended function parallel I/O ports, and a watchdog timer.

The DS1283 is an onboard, permanently powered timekeeper on the DS2301VT and DS2301YT. This device is a self-contained real time clock, alarm, and interval timer in a 28-pin SOIC surface mount package. It is parallel-accessed by the HD6303Y and is permanently powered from the Softener's primary V_{CC} output pin.

Both the DS2301V(T) and the DS2301Y(T) support only the single chip operating modes of the HD6301V0 and HD6301Y0, respectively.

BLOCK DIAGRAM Figure 1



MICROPROCESSOR

The HD6303Y is a low-power CMOS microprocessor that is incorporated on both the DS2301V(T) and DS2301Y(T). It is instruction set-compatible with the industry standard 6801. In addition to the CPU functions, this device provides parallel I/O, serial I/O, and timer/counters. The Hitachi data sheet for this device should be consulted for full operational details.

DS5303 6303 SOFTENER CHIP

The DS5303 Softener makes possible the NV SRAM management, serial bootstrap loading, crashproof operation, and watchdog timer features of the DS2301V(T) and DS2301Y(T) Soft 6301 Stiks. For operational information on this device, the user should consult the DS53xx Micro Softener Chips and the DS5303 data sheets. Its features and how they apply to the DS2301 are described in the following sections.

MEMORY MAP

The DS5303's CE1\ and CE2\ signals each access either 8K or 32K bytes of memory space, for a total possible memory space of 8K, 16K, 32K, or 64K bytes. The selection between the two possible memory ranges is made under the control of the bootstrap loader and retains as nonvolatile information sustained from the external lithium cell in the absence of V_{CC}. The range selection operation is described in the DS5303 data sheet.

8K, 32K, and 64K bytes of NV SRAM are available as memory size options for the DS2301. For the 8K version, the DS5303's range bit should be cleared to 0 via the serial bootstrap loader. This configuration selects the 8K x 8 RAM on CE2\. Since CE1\ is not connected on this version, and the HD6303Y's address and data busses are not available to the user, the 8K

space selected by CE1\ as well as the undecoded areas below $C000 are not accessible by the user. The memory map for the 8K version of the DS2301 with the Range = 0 is shown at the left in Figure 2.

For the 32K byte and the 64K byte version, the range bit should be set to a 1. This configuration selects a 32K byte memory space on both CE1\ and CE2\. CE2\ is always connected to a 32K byte SRAM for both the 32K byte and 64K byte version. On the 32K byte version, CE1\ is left unconnected, and so the corresponding 32K byte space is not accessible by the user. The memory map for the 32K or 64K version of the DS2301 with the Range = 1 is shown in Figure 2.

PCE2\ is not connected on the DS2301. Therefore, the PCE2 bit should be left disabled in the DS5303.

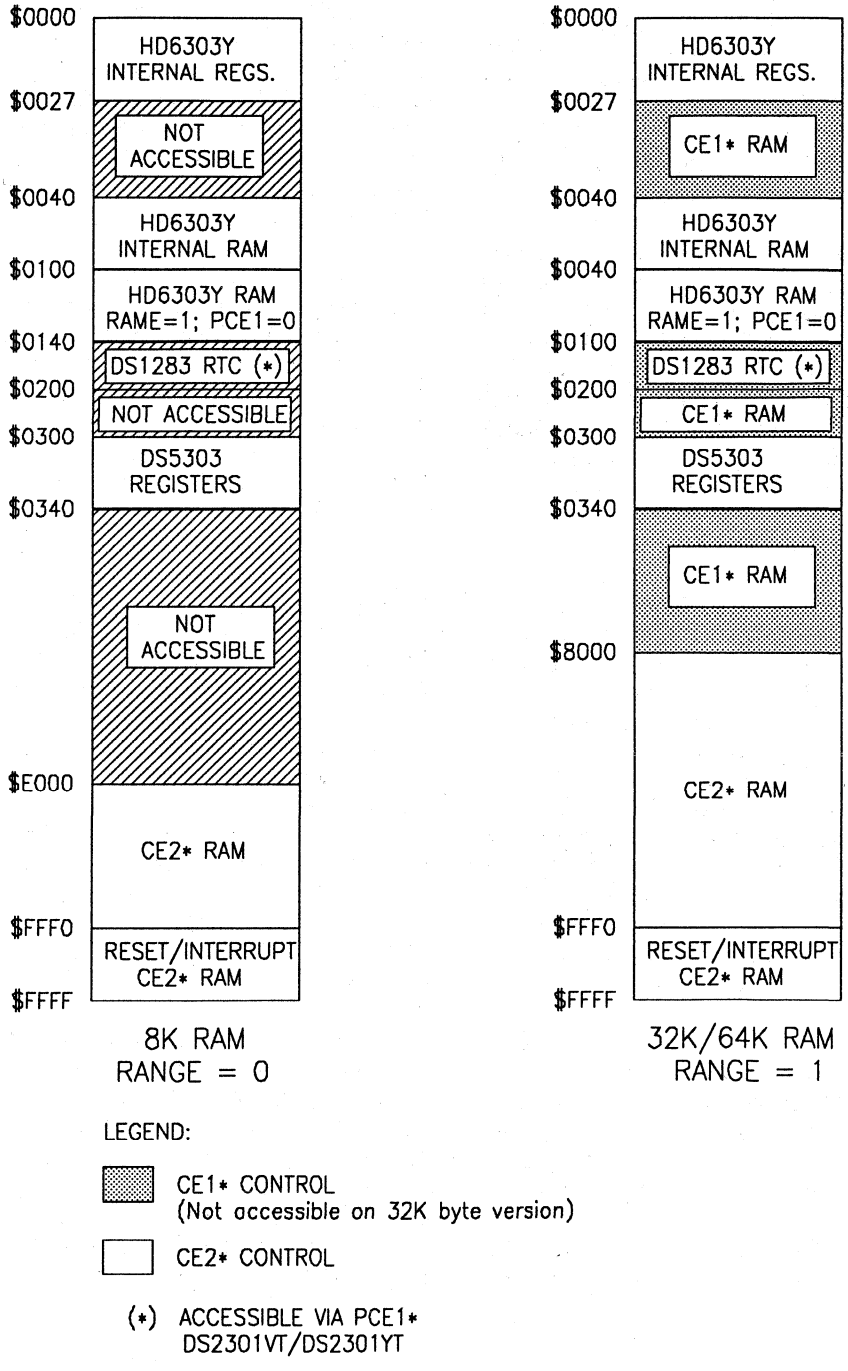
PCE1\ is connected to the onboard DS1283 Watchdog Timekeeper if it is installed as an option. Because of its additional I/O capabilities, the HD6303Y was chosen as the processor for the DS2301. However, there is a potential conflict in the memory map between the HD6303Y's internal RAM and the DS1283 accessed via PCE1\. The HD6303Y's incorporates 256 bytes of on-chip internal RAM which is located in the range of $0040 - $013F. This RAM can be enabled or disabled under the control of the RAME bit within the HD6303Y. The DS5303, which was originally designed for the HD6303X, enables its PCE1\ signal (which enables the DS1283) for any access in the range between $0100 - $01FF when the DS5303's PCE1 bit is enabled. When a read access is performed with the RAME and PCE1 bits both enabled in the conflicting region of $0100 - $013F, the HD6303Y will read data from the internal RAM. The problem occurs during a write access in this region. When both RAME and PCE1 are enabled during a write access between $0100 - $013F, the HD6303Y will simultaneously write an internal RAM location and drive its R/W\ line low. Consequently, both the internal RAM and the timekeeper will be written. Data will therefore be corrupted in the timekeeper. A solution to this problem is to make sure that the PCE1 bit is disabled when accesses to the RAM are performed in the conflicting range and to make sure that RAME is disabled when accesses are performed to the timekeeper. This can be summarized as follows:

Internal RAM access: RAME = 1, PCE1 = 0
Timekeeper access: RAME = 0, PCE1 = 1

As an added precaution, PCE1 should only be enabled just prior to code which accesses the timekeeper and disabled immediately following its execution.

If the timekeeper is not present, the PCE1 bit should be left disabled.

DS2301V(T) AND DS2301Y(T) MEMORY MAPS Figure 3



DS2301V(T) PIN FUNCTIONS

The 40 signals provided on the DS2301V(T)'s edge connector map one-for-one with the popular HD63701V0 40-pin DIP configured for operation in the single chip mode with one exception: The input strobe pin provided on the HD63701V0 is replaced with the Reload pin (RL\). This pin is used to externally activate the Softener's on-chip serial bootstrap loader for initialization of the program/data RAM.

As shown in Figure 1, the NMI\, STBY\, IRQ1\, and E control signals are taken directly from the HD6303Y processor and are brought out to the edge connector of the DS2301V(T). These pins are identical in function to the counterpart signals implemented on the HD6301V. The multiple function port pins P2.4-0 of the HD6303Y are also brought directly out to the edge connector. These pins also have identical counterparts in the HD6301V0.

In place of Port 3 on the HD6301V0, Port 6 on the HD6303Y is pinned out on the edge connector along with its associated output strobe signal, OS6\. These pins are identical in function to those on the HD6301V0. However, all of the port 6 control registers, including the control bits for the output strobe, are addressed at different locations within the HD6303Y. Therefore, for applications in which the DS2301V is to retrofit into a socket designed to accept a HD6301V0, the application software must be modified to address the control registers at the new locations. Consult the Hitachi technical literature for these devices for the exact location of these registers.

The HD6303Y provides some additional internal I/O functions which are not available on the HD6301V0. These include a programmable 8-bit timer and an asynchronous/synchronous serial port. Again, consult the Hitachi literature for programming details on these features.

X1 and X2 of the DS5303 are brought out in place of the XTAL and EXTAL on the HD6301V0. This is done so that the Softener can detect the execution of the processor's low power standby mode and place itself in such a low power state. The X1 and X2 are functionally identical to the X1 and X2 pins of the HD6303V0. The external RST\ line is monitored by the DS5303's RSTIN\ pin, and the HD6303Y's RST\ input is controlled by the DS5303's RSTOUT\ pin. This is done so that the Softener can monitor the external RST\ line to signal the termination of the low power standby condition.

In place of Ports 1 and 4 of the HD6301V0, Ports A and D of the DS5303 are brought out on the edge connector. These pins are functionally compatible with their counterparts. In fact, they can be programmed to serve the additional functions described above.

Ports B and C on the DS5303 are not pinned out on the DS2301V(T). As a result, the Dual Port Register File is not available on this Soft Stik.

DS2301Y(T) PIN FUNCTIONS

The 68-position DS2301Y(T) Soft 6303 Stik provides all of the functions of the HD63701Y0 64-pin DIP operating in the single chip mode.

As described above for the HD6301V, the NMI\, STBY\, IRQ1\, and E control signals as well as the multiple function port pins P2.4-0 are taken directly from the HD6303Y processor and are brought out to the edge connector of the DS2301V(T). In addition, the HD63701Y0-identical signals IRQ2\, P2.7-5, P6.7-0, IS6\, OS6\, P5.7-6, and P5.3-2 are present on the edge connector.

As for the DS2301V(T), the X1 and X2 signals are brought out as functional equivalents for XTAL and EXTAL, respectively, on the HD6303Y. The external RST\ line is actually tied to the DS5303's RSTIN\, also as described above. The Reload pin (RL\) is brought out in place of the signal MP0. During normal operation, this pin should be tied high, as it should be on the HD63701Y0 to enable single chip operation.

In place of P1.7-0, P3.7-0, P4.7-0, and P7.4-0 on the HD63701Y0, PA.7-0, PB.7-0, PC.7-0, and PD.4-0 are pinned out from the DS5303. All of these pins are capable of serving the corresponding function in addition to the special functions described above.

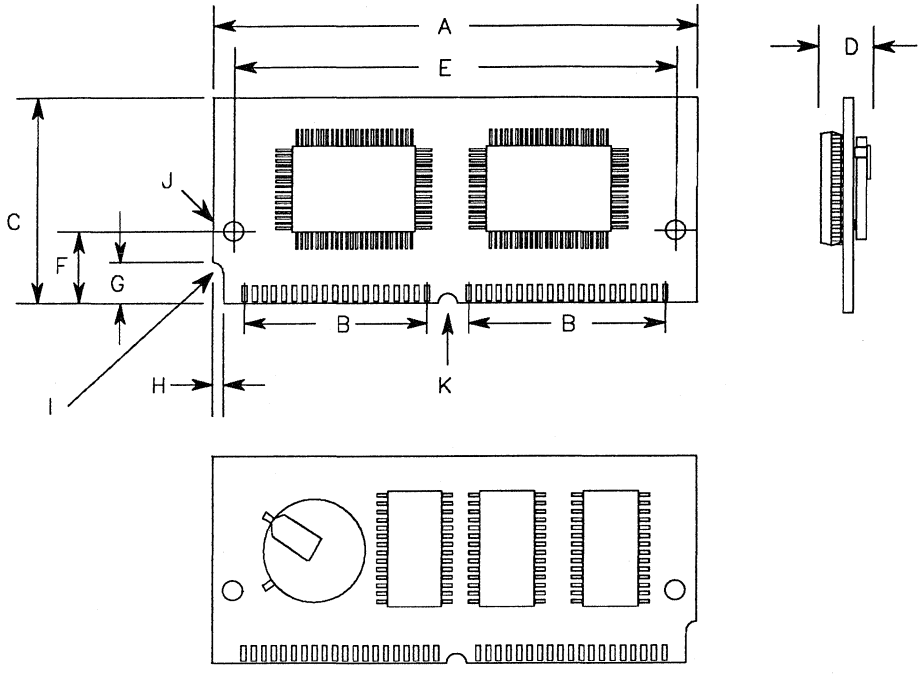
ORDERING INFORMATION

The following versions of the DS2301 are available as standard products from Dallas Semiconductor:

PART #	TIME-KEEPER	RAM	CLOCK
DS2301V 08	No	8K x 8	1.0 MHz
DS2301V 32-B	No	32K x 8	1.0 MHz
DS2301VT 32-B	Yes	32K x 8	2.0 MHz
DS2301Y 08	No	8K x 8	1.0 MHz
DS2301YT 32-B	Yes	32K x 8	1.0 MHz
DS2301YT 64-B	Yes	64K x 8	2.0 MHz

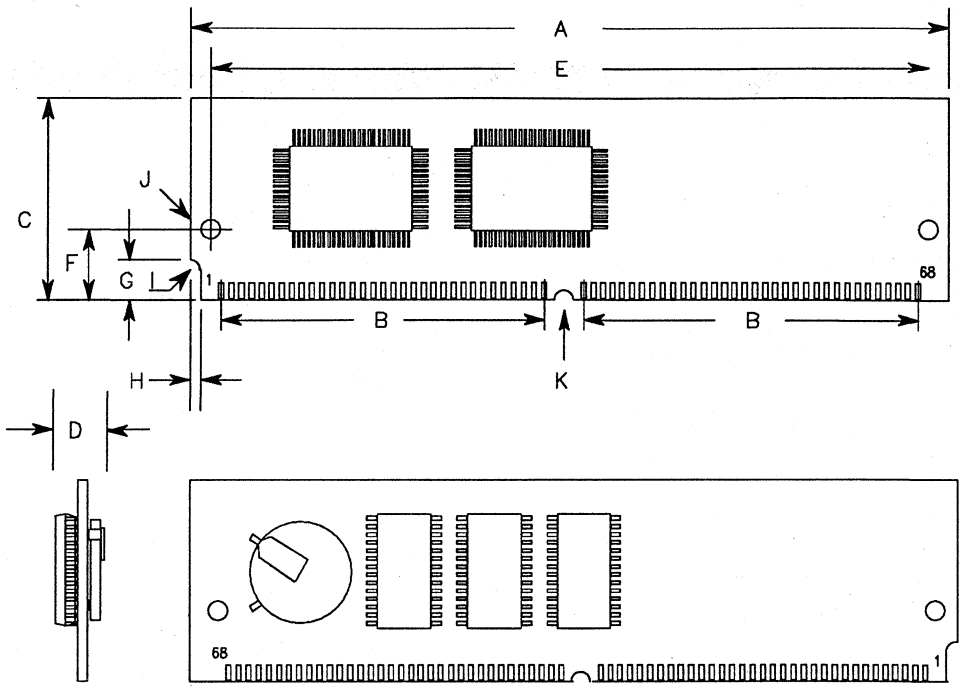
Please contact Dallas Semiconductor for ordering information on other configurations of the DS2301.

DS2301V
SOFT 6301 STIK



DIM.	INCHES	MM
A	2.650	67.31
B	0.950	24.13
C	1.250	31.75
D	0.350	8.89
E	2.384	60.55
F	0.400	10.16
G	0.250	6.35
H	0.080	2.03
I	R .062	R 1.57
J	D 0.125	D 3.18
K	R .062	R 1.57

DS2301Y(T)
SOFT 6301 STIK



DIM.	INCHES	MM
A	4.050	102.87
B	1.650	41.91
C	1.250	31.75
D	0.350	8.89
E	3.784	96.11
F	0.400	10.16
G	0.250	6.35
H	0.080	2.03
I	R .062	R 1.57
J	D 0.125	D 3.18
K	R .062	R 1.57

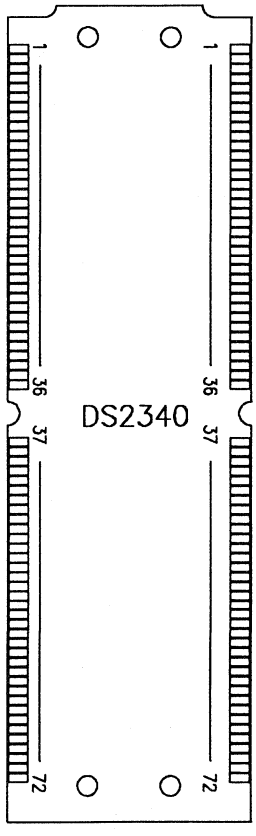
DALLAS SEMICONDUCTOR

DS2340
Soft V40 Flip Stik

FEATURES

- V40-based embedded control system adapts to task-at-hand:
  - -Up to 256K bytes of lithium-backed NV SRAM for program/data storage
  - -Serial bootstrap loading of software
  - -Code can be changed in end use
- Incorporates V40 family processor:
  - -Executes industry-standard 8086 instruction set
  - -On-chip timers, serial I/O, DMA, and interrupt control
  - -Allows code development in native instruction set of IBM PC
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports
- DS2340T provides DS1283 Watchdog Timekeeper Chip
- Dual 72-pin SIMM connection scheme supports single-board or expanded operation

PACKAGE OUTLINE



72-Pin SIMM Double-edge Connector

DESCRIPTION

The DS2340 and DS2340T Soft V40 Flip Stiks are complete, 8086-compatible microcontroller systems that provide the benefits of adaptability, crashproof operation, and powerful I/O capabilities for embedded control applications in an extremely small form factor. These unique features are made possible by the incorporation of the DS5340 V40 Softener Chip. In addition, the DS2340 and DS2340T execute the native instruction set of the IBM PC, so that the PC can serve as a development platform for the Soft V40 Flip Stiks. As a result, a wide variety of high-level language compilers, assemblers, and debugging tools are available to support system designs based on the DS2340.

The DS2340 offers two SIMM card-edges to support single-board and expanded operations. This scheme allows the Flip Stik to be installed into a 72-pin SIMM connector in one of two ways to support the selected operation. Connector A supports single-board operation. This card edge provides a total of three 8-bit parallel I/O ports. One of these ports allows each pin to serve as an interrupt input. The other two ports can be configured as a high-speed interface to allow the DS2340 to act as a peripheral controller to a host microprocessor system. For expanded operation, connector B supports all of the address lines as well as DMA handshake and bus control lines.

The DS2340T incorporates a DS1283 Watchdog Timekeeper Chip as a permanently-powered clock/calendar function that keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years. The clock is parallel-accessed by the V40 processor and is powered by the onboard lithium cell for greater than 10 years of timekeeping in the absence of V_{CC}.

NOTE: Throughout this data sheet, when features are discussed that are generic to both the time and non-time versions of the DS2340, the device is referred to as the DS2340(T).

PIN DESCRIPTION

Tables 1 and 2 document the pin assignments for sides A and B, respectively, for the DS2340(T). Table 3 is a summary of the pin functions that are common for both sides A and B. Finally, Tables 4 and 5 summarize pin functions unique to sides A and B, respectively.

DS2340(T) SIDE A PIN ASSIGNMENT Table 1

1 - AD0	25 - PB.3	49 - TOUT2
2 - AD1	26 - PB.4	50 - TCLT2
3 - AD2	27 - PB.5	51 - TCLK
4 - AD3	28 - PB.6	52 - A16
5 - AD4	29 - PB.7	53 - A15
6 - AD5	30 - IBR\	54 - A14
7 - AD6	31 - PCE2\	55 - A13
8 - AD7	32 - CE4\	56 - A12
9 - INTP1	33 - CE3\	57 - A11
10 - INTP2	34 - CE2\	58 - A10
11 - INTP3	35 - V_{CC}	59 - A9
12 - INTP4	36 - GND	60 - A8
13 - INTP6	37 - GND	61 - INTAK\/TOUT1/SRDY\
14 - TXD	38 - V_{CC}	62 - ASTB
15 - RXD	39 - X1	63 - PA.7
16 - IOWR\	40 - X2	64 - PA.6
17 - MWR\	41 - PC.7	65 - PA.5
18 - IORD\	42 - PC.6	66 - PA.4
19 - MRD\	43 - PC.5	67 - PA.3
20 - RST\	44 - PC.4	68 - PA.2
21 - INTP\	45 - PC.3	69 - PA.1
22 - PB.0	46 - PC.2	70 - PA.0
23 - PB.1	47 - PC.1	71 - RL\
24 - PB.2	48 - PC.0	72 - NMI

(\Denotes Condition Low)

DS2340(T) SIDE B PIN ASSIGNMENT Table 2

1 - AD0	25 - BUFR/W\	49 - A19
2 - AD1	26 - REFRQ\	50 - A18
3 - AD2	27 - DMARQ0	51 - A17
4 - AD3	28 - DMAAK0\	52 - A16
5 - AD4	29 - DMARQ1	53 - A15
6 - AD5	30 - DMAAK1	54 - A14
7 - AD6	31 - PCE2\	55 - A13
8 - AD7	32 - CE4\	56 - A12
9 - INTP1	33 - CE3\	57 - A11
10 - INTP2	34 - CE2\	58 - A10
11 - INTP3	35 - V_{cc}	59 - A9
12 - INTP4	36 - GND	60 - A8
13 - INTP6	37 - GND	61 - A7
14 - TXD	38 - V_{cc}	62 - A6
15 - RXD	39 - X1	63 - A5
16 - IOWR\	40 - X2	64 - A4
17 - MWR\	41 - END/TC\	65 - A3
18 - IORD\	42 - BUSLOCK\	66 - A2
19 - MRD\	43 - PA.3	67 - A1
20 - RST\	44 - PA.2	68 - A0
21 - INTP\	45 - TOUT2	69 - PA.1
22 - RSTOUT\	46 - TCTL2	70 - PA.0
23 - CLKOUT	47 - TCLK	71 - RL\
24 - BUFEN\	48 - INTAK\/TOUT1/	

DS2340(T) PIN DESCRIPTION - COMMON FOR SIDE A OR B Table 3

NAME	DESCRIPTION	NAME	DESCRIPTION
V_{cc}	+5V Power Supply Input	NMI	Non-Maskable Interrupt
GND	Ground		Input to V40
X1	Crystal Oscillator Input	INTP1	Interrupt Input 1 to V40
X2	Crystal Oscillator Output	INTP2	Interrupt Input 2 to V40
A16-A8	V40 Address Bus Outputs	INTP3	Interrupt Input 3 to V40
AD7-AD0	V40 Mux. Address/Data	INTP4	Interrupt Input 4 to V40
	Bus; Bidirectional	INTP6	Interrupt Input 6 to V40
MRD\	V40 Memory Read Output	PA.3-0	DS5340 Port A Bits 1 and 0;
MWR\	V40 Memory Write Output		Bidirectional
IOR\	V40 I/O Read Output	RL\	DS5340 Reload Input
IOWR\	V40 I/O Write Output	INTP\	DS1283 INTP\ Output;
CE2\-CE4\	DS5340 Chip Enable Outputs		Open-Drain
PCE2\	DS5340 Peripheral Chip	TCLK	V40 Timer Clock Input
	Enable Output	TCTL2	V40 Timer/Counter 2
RST\	System Reset Input		Control Input
TXD	V40 Transmit Data Output	TOUT2	V40 Timer/Counter 2 Output
RXD	V40 Receive Data Input	INTAK\	V40 Interrupt Acknowledge
		/ TOUT1	/ Timer 1 Output
		/ SRDY\	/ Serial Ready

DS2340(T) PIN DESCRIPTION - UNIQUE TO SIDE A Table 4

NAME	DESCRIPTION
ASTB	V40 Address Strobe
PA7-PA4	DS5340 Port A bits 7-2; Bidirectional
PB7-PB0	DS5340 Port B; Bidirectional
PC7-PC0	DS5340 Port C; Bidirectional
IBR\	Interrupt Buffer Ready status output

DS2340(T) PIN DESCRIPTION - UNIQUE TO SIDE B Table 5

NAME	DESCRIPTION
A19-A17	Demultiplexed V40 AddressOutput Lines
A7-A0	Demultiplexed V40 Address Output Lines
RSTOUT\	V40 Reset Output
CLKOUT	V40 Clock Output
BUFEN\	V40 Buffer Enable Output
BUFR\W	V40 Buffer Read/Write Output
REFRQ\	V40 Refresh Request Output
DMARQ0,1	V40 DMA Request Inputs
DMAAK0,1	V40 DMA Acknowledge Outputs
END\TC\	V40 End Input/Terminal Count Output
BUSLOCK\	V40 Bus Lock Output

BLOCK DIAGRAM

Figure 1 depicts the DS2340(T). A standard NEC V40 is used as the microprocessor. This component provides the 8086-compatible CPU along with basic I/O functions. The Dallas Semiconductor DS5340 V40 Softener Chip provides nonvolatile control, bootstrap loading capability, and program/data partitioning for the Stik's SRAM. In addition, it provides a clock oscillator, extended function parallel I/O ports, and a watchdog timer.

The DS1283 Watchdog Timekeeper Chip is a self-contained clock/calendar, alarm, and interval timer in a 28-pin SOIC surface mount package. This device is parallel accessed from the V40 and is powered from the V40 Softener's primary V_{cco} output pin.

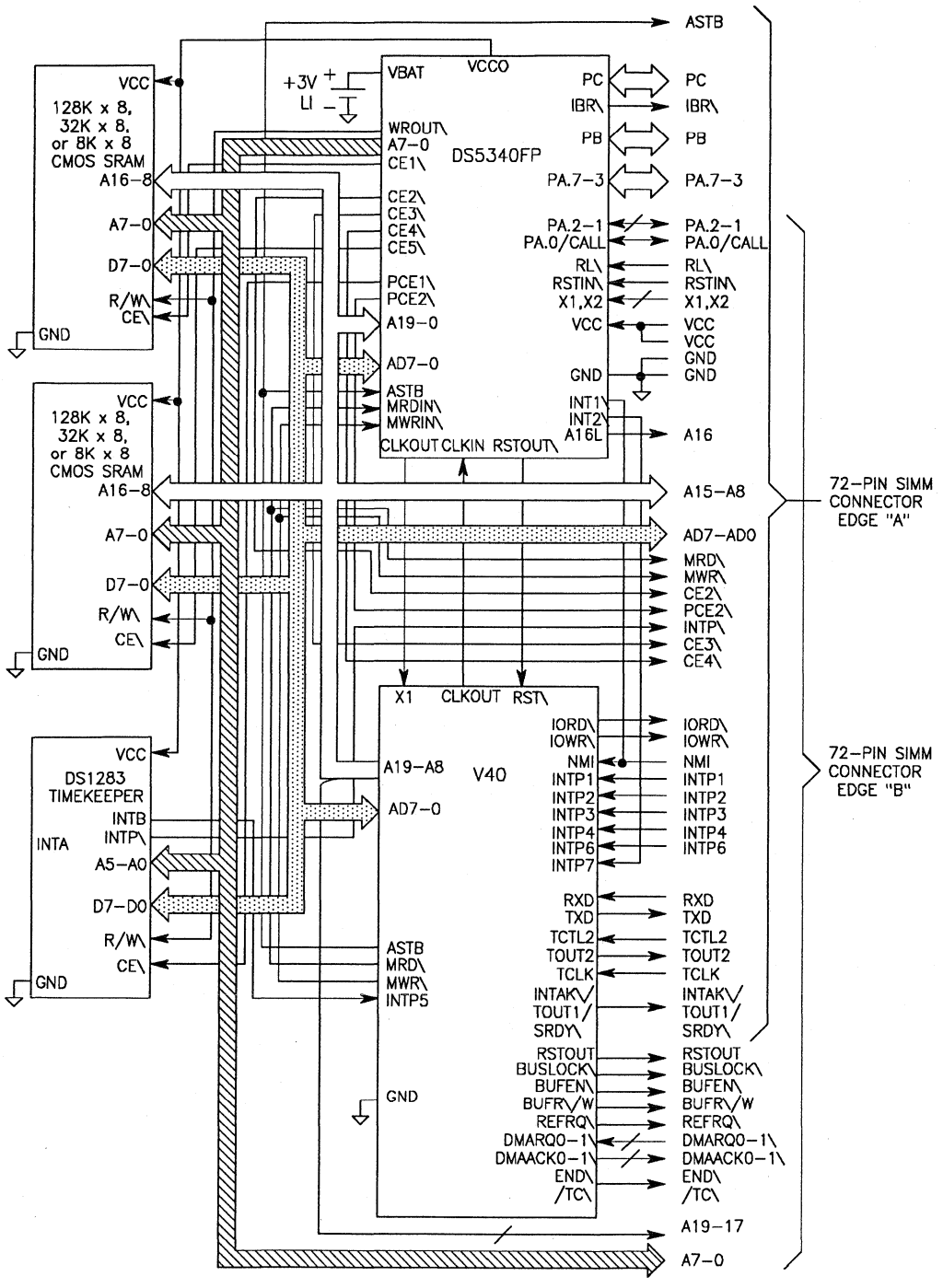
MICROPROCESSOR

The NEC V40 is a low-power CMOS microprocessor. It is instruction set-compatible with the industry standard 8086. As a result, software for the DS2340(T) is written in the native instruction set of the IBM PC, and the PC can serve as a platform for software development. In addition to the CPU functions, the V40 provides serial I/O, timer/counters, and interrupt inputs. The NEC data sheet for this device should be consulted for full operational details.

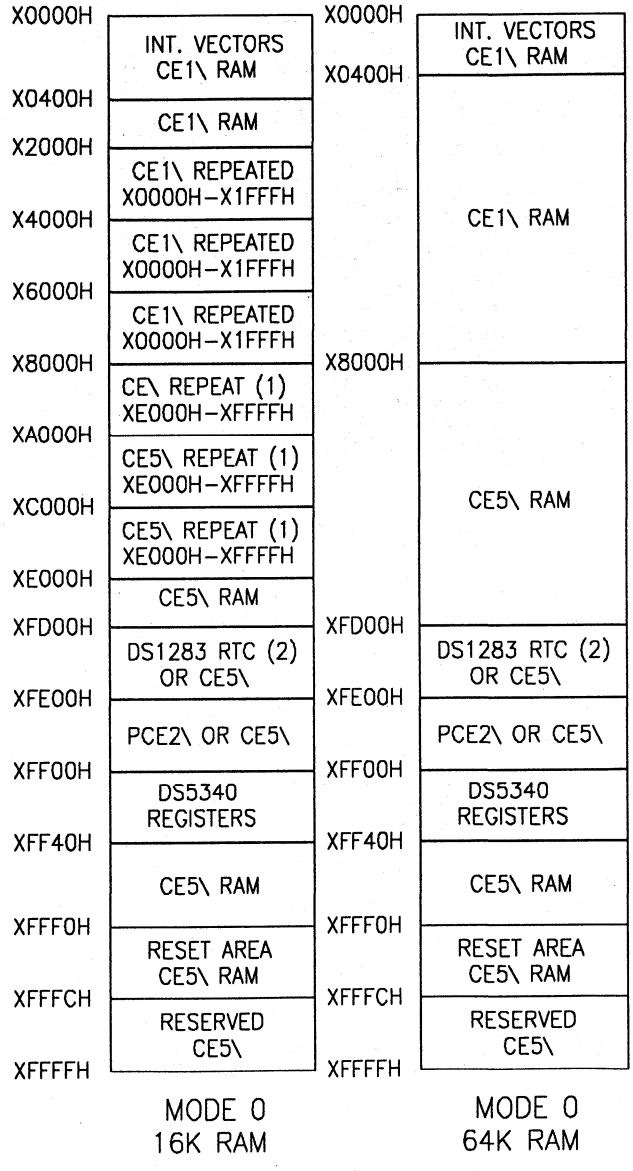
DS5340 V40 SOFTENER CHIP

The DS5340 makes possible NV SRAM management, serial bootstrap loading, crashproof operation, and watchdog timer features of the DS2340(T). For complete operational information on this device, the user should consult the DS53xx Micro Softener Chips data sheet and the DS5340 V40 Softener Chip data sheet. The features of the DS5340 that relate to the Flip Stik are described on the following pages.

DS2340(T) BLOCK DIAGRAM Figure 1

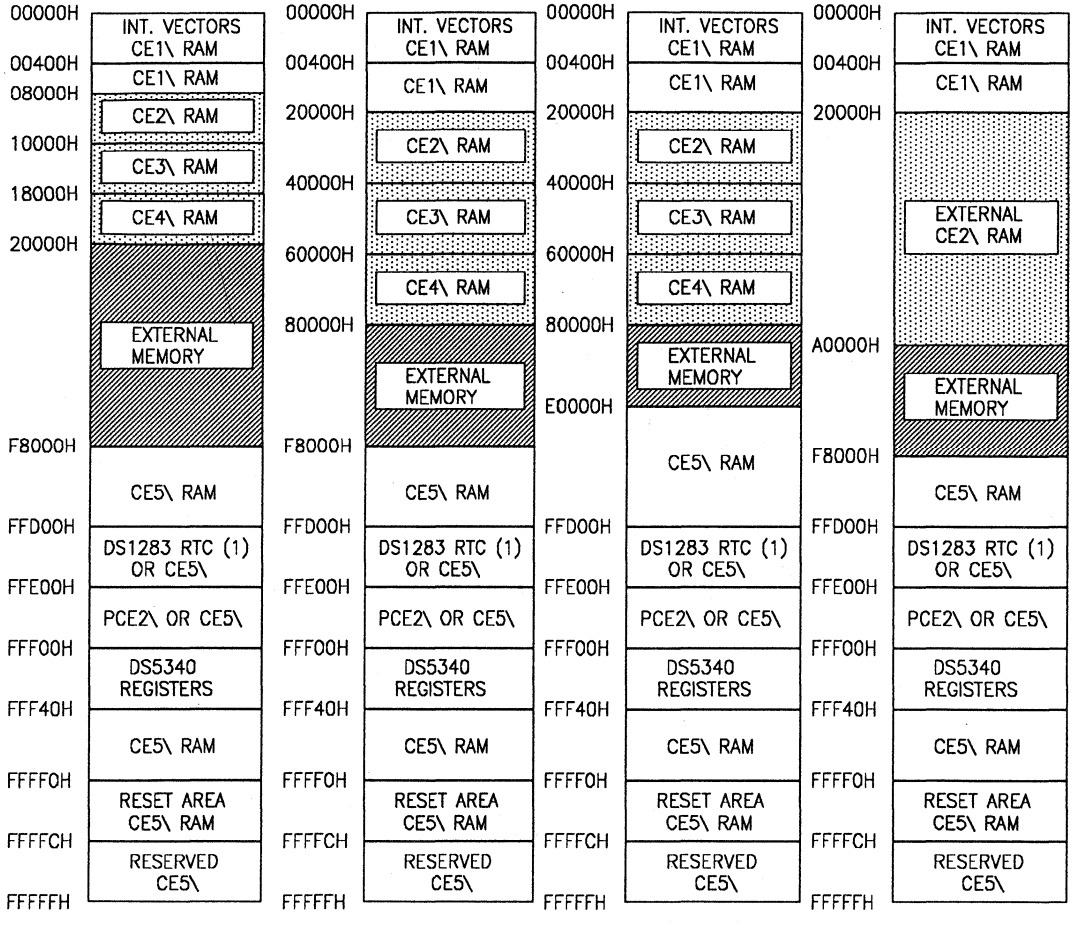


DS2340 MODE 0 MEMORY MAPS Figure 2



LEGEND:
(1) ONLY CE5\ ADDRESS SPACE IS REPEATED IN THESE AREAS – NOT PCE1\ OR PCE2\
(2) ACCESSIBLE VIA PCE3\ DS2340T

DS2340 MODES 1, 2, 3 AND 4 MEMORY MAPS Figure 3



MEMORY MAP

The memory map for the DS2340(T) is largely determined by the mode selection within the DS5340 during serial bootstrap loading. The five memory map modes implemented by the V40 Softener Chip are documented in that data sheet.

Versions of the DS2340(T) are available with either 16K, 64K, 160K, or 256K bytes of nonvolatile SRAM. The following discussion describes each of the five operating modes in terms of the typical memory size version for which they would be used in the DS2340(T). Figures 2 and 3 illustrate the resulting memory maps for these typical configurations.

Mode 0 would most likely be selected for a Soft V40 Flip Stik as a single-board system with either 16K bytes or 64K bytes of onboard nonvolatile SRAM. Chip enable outputs CE1\ and CE5\ are each activated for any memory access in the 32K byte ranges of X0000H - X7FFFH and X8000H - XFFFFH, respectively. The memory maps for Mode 0 on a DS2340(T) are illustrated in Figure 2. When a 16K byte version of the DS2340 is used, CE1\ and CE5\ are each connected to an 8K x 8 RAM. Since CE1\ and CE5\ are enabled on 32K byte boundaries, the 8K x 8 RAM space will be replicated four times for each chip enable signal, as shown in Figure 2.

Mode 1 would most likely be selected for a DS2340(T) populated with 64K bytes of NV SRAM in a system requiring offboard expansion. In this configuration, CE1\ and CE5\ would each control one of the two onboard 32K x 8 SRAMs. CE2\, CE3\, and CE4\ would each enable an offboard 32K x 8 memory space. This configuration is illustrated in Figure 3.

Modes 2 and 4 would typically be used for a DS2340(T) populated with 160K bytes of nonvolatile SRAM. In both modes, CE1\ and CE5\ would control the onboard 128K x 8 and 32K x 8 memories, respectively. In Mode 2, CE2\, CE3\, and CE4\ each control an offboard 128K x 8 memory space. In Mode 5, CE2\ controls an offboard 512K x 8 space while CE3\ and CE4\ are always disabled. These configurations are also illustrated in Figure 3.

Mode 3 would most likely be selected for a Flip Stik populated with a full 256K bytes of nonvolatile SRAM. CE1\ and CE5\ each control one of the onboard 128K x 8 SRAMs. CE2\, CE3\, and CE4\ each control an external 128K x 8 memory space as shown in Figure 3.

DS2340(T) PIN FUNCTIONS

As shown in the package outline diagram, the DS2340(T) offers two SIMM card-edges to support single-board and expanded operations. These connectors appear on opposite sides of the card and are designated as card edge A and card edge B. These designators are marked on the Stik PC board itself. This scheme allows the Flip Stik to be installed into a 72-pin SIMM connector in one of two ways to support either single-board or expanded operation.

As illustrated in Figure 1, the pinouts on both card edges support the major functions supplied by the DS5340 and the V40. These functions include the V40's non-multiplexed address lines A15-A8 and multiplexed address/data bus AD7-0, as well as the memory and I/O control lines. Also included are the V40's serial port and counter/timer I/O lines and all of its external interrupt input lines except for INTP5 and INTP7. These two lines are dedicated to the onboard DS1283 Watchdog Timekeeper Chip and V40 Softener Chip, respectively. Both card edges also bring out three lines from the DS5340's Port A as well as its crystal inputs, the Reload pin, its CE2\-CE4\ signals for interface to external memory, and its latched A16 address line from the V40.

In single-board operation using card edge A, the DS2340(T) offers a total of three parallel I/O ports. Port A allows each pin to serve as an interrupt input. Ports B and C can be configured either as parallel I/O or as a high-speed interface to allow the Flip Stik to act as a peripheral controller to a host microprocessor system. Card edge A also supports some offboard expansion capability. The ASTB pin is brought out so that the AD7-AD0 lines can be demultiplexed. For expanded operation, card edge B supports all of the 20 address lines as well as DMA handshake and bus control lines.

ORDERING INFORMATION

The following versions of the DS2340(T) are available as standard products from Dallas Semiconductor:

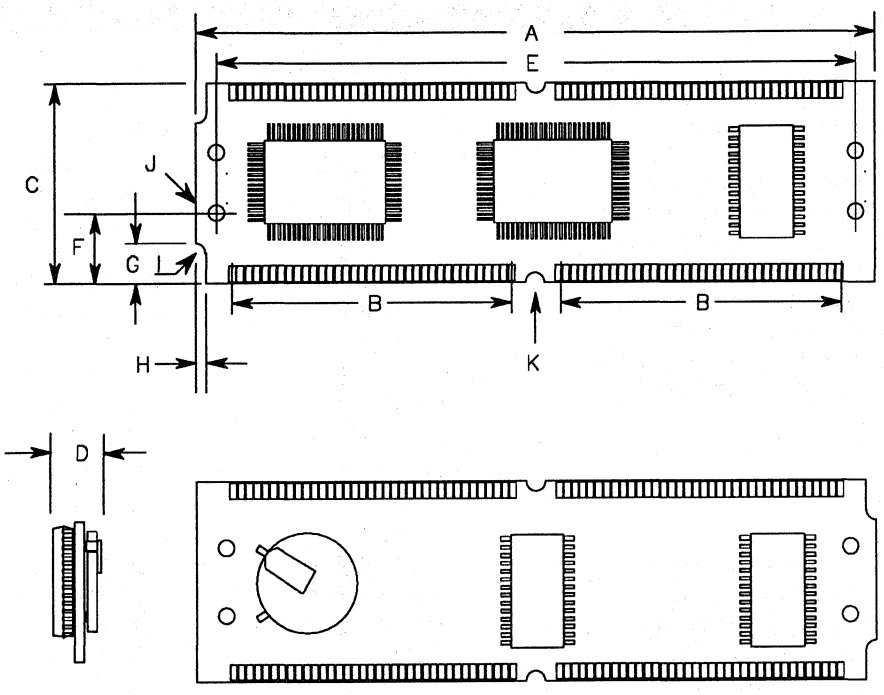
PART #	TIME-KEEPER	RAM	CLOCK
DS2340 16A	No	16K x 8	8 MHz
DS2340 64A	No	64K x 8	8 MHz
DS2340T 64-B	Yes	64K x 8	10 MHz
DS2340T 256-B	Yes	256K x 8	10 MHz

Please contact Dallas Semiconductor for ordering information on other configurations of the DS2340.

FOR FURTHER INFORMATION

Complete technical specifications for the DS5340 as well as other versions of the Micro Softener and Soft Stik products are available on request from Dallas Semiconductor.

DS2340(T)
Soft V40 Flip Stik



DIM.	INCHES	MM
A	4.250	107.95
B	1.750	44.45
C	1.250	31.75
D	0.472	12.00
E	3.984	101.19
F	0.400	10.16
G	0.250	6.35
H	0.080	2.03
I	R .062	R 1.57
J	D 0.125	D 3.18
K	R .062	R 1.57

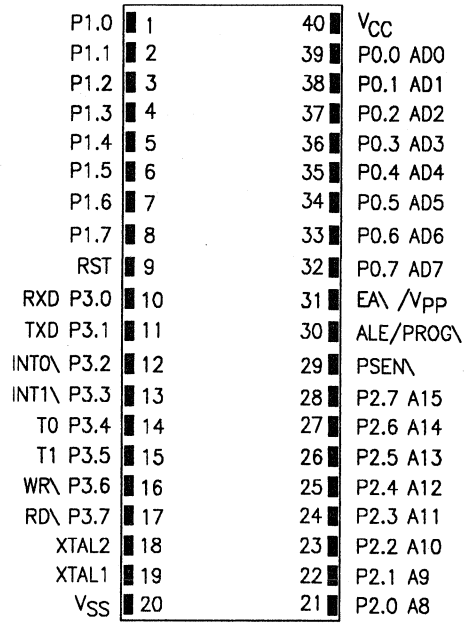
DALLAS SEMICONDUCTOR

DS5000
Soft Microcontroller

FEATURES

- 8-bit uC adapts to task-at-hand:
  - 8 or 32 Kbytes of high performance nonvolatile RAM for program and/or RAM for program and/or data memory storage
  - Initial downloading of software in end system via on-chip serial port
  - Capable of modifying its own program and/or data memory in end use
  - 128 internal nonvolatile registers for variable retention
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V_{CC}
  - Orchestrates orderly shutdown and automatic restart on power up/down
  - Automatic restart on detection of errant software execution
- Software Security Feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On-chip, full-duplex serial I/O ports
- Two on-chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout

PIN CONNECTIONS



40-Pin Encapsulated Package (700 Mil)

ORDERING INFORMATION

DS5000 –XX–XX

Clock Frequency
- 08 8 MHz
- 12 12 MHz
- 16 16 MHz

Program/Data RAM
- 08 8 Kbytes
- 32 32 Kbytes

DESCRIPTION

The DS5000 Soft Microcontroller is a high performance 8-bit CMOS microcontroller that offers "softness" in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V_{CC}. The entire program/data memory space is implemented using high speed, nonvolatile static CMOS RAM. Two memory size versions are available which offer either 8 Kbytes or 32 Kbytes of NV RAM for program/data storage. Furthermore, internal data registers and key configuration registers are also nonvolatile.

A major benefit resulting from its nonvolatility is that the Soft Microcontroller allows program memory to be changed at any time, even after the device has been installed in the end system. Additionally, the size of the program and data memory areas in the embedded RAM is variable and can be set either when the application software is initially loaded or by the software itself during execution.

Initial loading of the application software into the DS5000 is possible from either a parallel or serial interface to a host system. This function allows initialization of the nonvolatile areas of the device including program/data RAM and the configuration parameters. Serial loading uses the on-chip serial I/O port to accept incoming data from a host computer with an RS-232 port, such as a PC-based development system. Not only is it possible to initially boot via the serial port in the end system, but any subsequent software reloading can be done at will during system operation without the need for removal of the device.

The softness also provides the ultimate in adaptive system design by allowing either the data RAM or the data registers to retain information in the absence of V_{CC}. As a result, a virtually unlimited number of variables and/or data tables can be updated and maintained over the life of the product, as opposed to data being lost during a power fluctuation. This capability allows software to be developed which updates variables and data tables to reflect the cumulative knowledge of the control system from the time that it was put into service. Consequently, control systems can be given the ability to learn from experience and react by altering processing steps in response to operating conditions which change over extended periods of time.

The DS5000 Soft Microcontroller incorporates control functions which provide crashproof operation when system power is momentarily disrupted or removed entirely. These functions include the Power Fail Warning interrupt, Automatic Power Down, and Power On Restart. The Power Fail Warning interrupt provides an early warning of a potential power failure so that the operational state of the system can be stored prior to a complete removal of system V_{CC}. The Automatic Power Down feature causes all nonvolatile resources to be sustained at low current from the embedded lithium energy source while system power is removed. When V_{CC} voltage is applied once again, the processor is automatically restarted with an internal flag set indicating that a Power On sequence has just been performed. Regardless of whether the power merely fluctuates or is absent for years, upon its return, the Soft Microcontroller has the ability to resume execution when power is re-applied as if the power failure had not occurred at all.

The Soft Microcontroller's tolerance of power cycling provides an alternative for battery-powered hand-held systems which typically drain their batteries during periods of idle time, when processing is not being performed. On/off power cycling can be employed to cause such systems to consume battery power only during processing to ensure a dramatic reduction of the overall power dissipation.

The DS5000 also provides extensive software security with its unique on-chip software encryption logic. This feature prevents unauthorized individuals from reading and disassembling program/data RAM. When activated, the device loads and executes the software in an encrypted form, rendering the contents of the RAM and the execution of the program unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected 40-bit key which is programmed by the user. Any attempt to discover the key value results in its erasure, rendering the contents of the program/data RAM useless. In this manner, the investment represented by the resident software is protected from piracy.

The DS5000 incorporates these unique functions in a device which is instruction set and pin compatible with the industry standard 8051 microcontroller architecture. Development work for new designs based on the DS5000 can be performed utilizing existing development tools and software packages which support the 8051

architecture.

The DS5000 also provides a full complement of I/O functions, including two 16-bit event counter/timers, a full-duplex serial I/O port capable of asynchronous or synchronous operation, 32 parallel I/O lines, and a watchdog timer. If additional external memory is desired beyond the embedded program/data RAM, 18 parallel I/O lines may be assigned to serve the Expanded Bus function.

PIN DESCRIPTION (\ Denotes Condition Low)

V_{CC}, GND	Power Supply inputs.
P0.7-P0.0 **AD7-AD0**	Port 0: Bidirectional I/O; open drain These pins also serve the function of Address/Data Bus: Bidirectional
P1.7-P1.0	Port 1: Bidirectional I/O
P2.7-P2.0 **A15-A8**	Port 2: Bidirectional I/O These pins also serve the function of Address Bus: Outputs
P3.7-P3.0	Port 3: Bidirectional I/O Each of the pins on Port 3 may be selected to serve an alternate function; as described below.
RD **(P3.7)**	Expanded Data Memory Read Strobe: Output; active low

WR\ (P3.6)	Expanded Data Memory Write Strobe: Output; active low
T1,T0 (P3.5,P3.4)	Timer/Counter pins: Inputs; active high
INT1\, INT0\ (P3.3,P3.2)	External interrupt pins: Inputs; active low
TXD (P3.1)	Transmit Data: Output
RXD (P3.0)	Receive Data: Input
RST	Reset: Input; active high
ALE (PROG\)	Address Latch Enable: Output; active high (or Program Byte Enable: Input; active low)
PSEN	Program Store Enable: Output; active low
EA\ (VPP)	External Access Enable: Input; active low (or VPP programming voltage input)
XTAL1, XTAL2	Crystal inputs

INSTRUCTION SET

The DS5000 executes an instruction set which is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages which have been written for the 8051 are compatible with the DS5000, including cross-assemblers, high-level language compilers, and debugging tools.

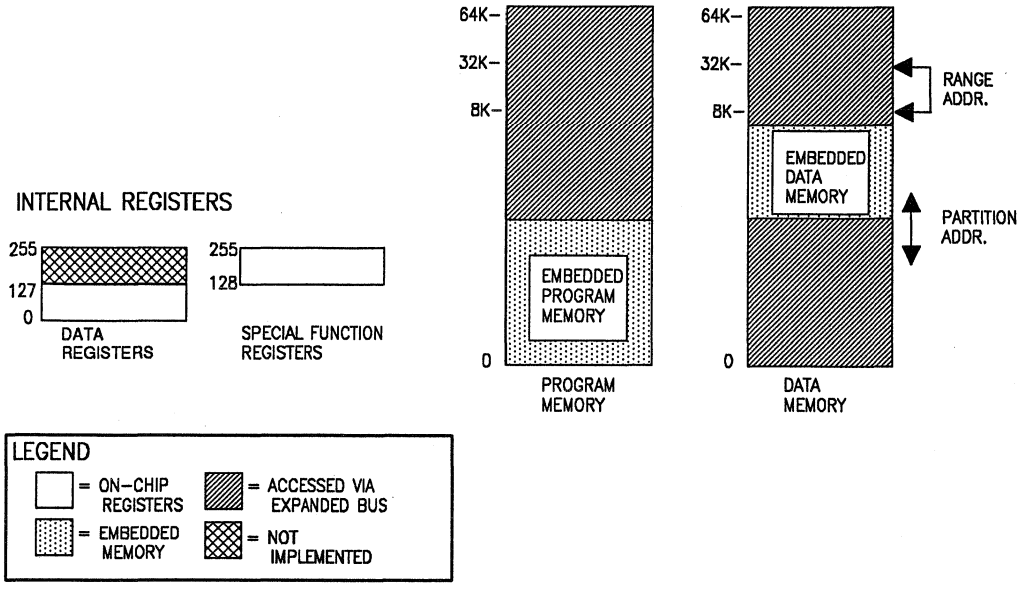
A complete description for the DS5000 instruction set is available in the DS5000 Soft Microcontroller User's Guide.

MEMORY ORGANIZATION

Figure 1 illustrates the address spaces which are accessed by the DS5000. As illustrated in the figure, separate address spaces exist for program and data memory. Since the basic addressing capability of the machine is 16 bits, a maximum of 64 Kbytes of program memory and 64 Kbytes of data memory can be accessed by the DS5000 CPU. The 8K or 32K byte embedded RAM area can be used to contain both program and data memory.

The internal register space is divided into two parts: Data Registers and Special Function Registers. There are a total of 128 data registers including four 8-byte banks of working registers (R0-R7). The Special Function Registers include the CPU Registers as well as registers which provide control and status information for the program and data memory mapping, nonvolatile operation, and on-chip I/O functions.

DS5000 LOGICAL ADDRESS SPACES Figure 1



SPECIAL FUNCTION REGISTERS

There are a total of 23 Special Function Registers which have been implemented in the DS5000. Table 5-1 lists each of these along with their respective addresses, reset values, and functional descriptions.

DS5000 SPECIAL FUNCTION REGISTER MAP Table 1

New or Modified Register	Label	Direct Register Address	Reset Value	Bit Address-able	Functional Description
	B	0F0H	00H	X	B Register
	A	0E0H	00H	X	Accumulator
	PSW	0D0H	00H	X	Program Status Word
X	TA	0C7H	055H		Timed Access
X	MCON	0C6H	RT		Memory Control
X	IP	0B8H	00H	X	Interrupt Priority Ctl.
	P3	0B0H	0FFH	X	Port 3 Parallel I/O
	IE	0A8H	00H	X	Interrupt Enable Ctl.
	P2	0A0H	0FFH	X	Port 2 Parallel I/O
	SBUF	099H	??		Serial Data Buffer
	SCON	098H	00H	X	Serial Control
	P1	090H	0FFH	X	Port 1 Parallel I/O
	TH1	08DH	00H		Timer 1 High Byte
	TH0	08CH	00H		Timer 0 High Byte
	TL1	08BH	00H		Timer 1 Low Byte
	TL0	08AH	00H		Timer 0 Low Byte
	TMOD	089H	00H		Timer Mode Select
	TCON	088H	00H	X	Timer Control
X	PCON	087H	RT		Power Control
	DPH	083H	00H		Data Pointer High Byte
	DPL	082H	00H		Data Pointer Low Byte
	SP	081H	07H		Stack Pointer
	P0	080H	0FFH	X	Port 0 Parallel I/O

NOTES:

?? indicates that the register value is indeterminate on reset.
RT indicates that the initialization performed on the register is dependent on the type of the reset.

The Power Control (PCON), Interrupt Priority (IP), Memory Control (MCON), and Timed Access (TA) registers represent modifications from the 8051 implementation, as denoted in the above table. The following is a detailed summary of these registers.

POWER CONTROL REGISTER

Label: PCON **Register Address: 087H**

D7	D6	D5	D4	D3	D2	D1	D0
SMOD	POR	PFW	WTR	EPFW	EWT	STOP	IDL

Bit Description:

PCON.7 SMOD
"Double Baud Rate" : When set to a 1, the baud rate is doubled when the serial port is being used in modes 1, 2, or 3.
Initialization: Cleared to a 0 on any reset.
Read Access: Can be read normally at any time.
Write Access: Can be written normally at any time.

PCON.6 POR
"Power On Reset": Indicates that the previous reset was initiated during a Power On sequence.
Initialization: Cleared to a 0 when a Power On Reset occurs. Remains at 0 until it is set to a 1 by software.
Read Access: Can be read normally at any time.
Write Access: Can be written only by using the Timed Access Register.

PCON.5: PFW
"Power Fail Warning": Indicates that a potential power failure is in progress. Set to 1 whenever V_{CC} voltage is below the V_{PFW} threshold. Cleared to a 0 immediately following a read operation of the PCON register. Once set, it will remain set until the read operation occurs regardless of activity on V_{CC}.
Initialization: Cleared to a 0 during a Power On Reset.
Read Access: Can be read normally anytime.
Write Access: Not writeable.

PCON.4: WTR "Watchdog Timer Reset" Set to a 1 when a reset was issued as a result of a Watchdog Timer timeout. Cleared to 0 immediately following a read of the PCON register

Initialization: Set to a 1 after a Watchdog Timeout Reset. Cleared to a 0 on a No-V_{LI} Power on Reset. Remains unchanged during other types of resets.

Read Access: May be read normally anytime.

Write Access: Cannot be written.

PCON.3: EPFW "Enable Power Fail Interrupt": Used to enable or disable the Power Fail interrupt. When EPFW is set to a 1 it will be enabled; it will be disabled when EPFW is cleared to a 0.

Initialization: Cleared to a 0 on any type of reset.

Read Access: Can be read normally anytime.

Write Access: Can be written normally anytime.

PCON.2: EWT "Enable Watch-dog Timer" Used to enable or disable the Watchdog Timeout Reset. The Watch-dog Timer is enabled if EWT is set to a 1 and will be disabled if EWT is cleared to a 0.

Initialization: Cleared to a 0 on a No-V_{LI} Power on Reset. Remains unchanged during other types of resets.

Read Access: May be read normally anytime.

Write Access: Can be written only by using the Timed Access register.

PCON.1: STOP "Stop": Used to invoke the Stop Mode. When set to a 1 program execution will terminate immediately and Stop Mode operation will commence. Cleared to a 0 when program execution resumes following a hardware reset.

Initialization: Cleared to a 0 on any type of reset.

Read Access: Can be read anytime.

Write Access: Can be written only by using the Timed Access register.

PCON.0: IDL "Idle": Used to invoke the Idle Mode. When set to a 1 program execution will be halted and will resume when the Idle bit is cleared to 0 following an interrupt or a hardware reset.

Initialization: Cleared to 0 on any type of reset or interrupt.

Read Access: Can be read normally anytime.

Write Access: Can be written normally anytime.

INTERRUPT PRIORITY REGISTER

Label: IP **Register Address: 0B8H**

D7	D6	D5	D4	D3	D2	D1	D0
RWT	–	–	PS	PT1	PX1	PT0	PX0

Bit Description:

IP.7: RWT "Reset Watch-Timer": When set to a 1 the Watchdog Timer count will be reset, and counting will begin again. The RWT bit will then automatically be cleared again to 0. Writing a 0 into this bit has no effect.
Initialization: Cleared to a 0 on any reset.
Read Access: Cannot be read.
Write Access: Can be written only by using the Timed Access register.

All of the following bits are read/write at any time and are cleared to 0 following any hardware reset.

IP.4: PS "Serial Port Priority": Programs Serial Port interrupts for high priority when set to 1. Low priority is selected when cleared to 0.

IP.3: PT1 "Timer 1 Priority": Programs Timer 1 interrupt for high priority when set to 1. Low priority is selected when cleared to 0.

IP.2: PX1 "Ext. Int. 1 Priority": Programs External Interrupt 1 for high priority when set to 1. Low priority is selected when cleared to 0.

IP.1: PT0 "Timer 0 Priority": Programs Timer 0 interrupt for high priority when set to 1. Low priority is selected when cleared to 0.

IP.0: PX0 "Ext. Int. 0 Priority": Programs External Interrupt 0 for high priority when set to 1. Low priority is selected when cleared to 0.

MEMORY CONTROL REGISTER

Label: MCON **Register Address: 0C6H**

D7	D6	D5	D4	D3	D2	D1	D0
PA3	PA2	PA1	PA0	RA32/8	ECE2	PAA	—

Bit Description:
MCON.7-4: PA3-0

"Partition Address": Used to select the starting address of data memory in embedded RAM. Program space lies below the Partition Address.

Selection:

PA3	PA2	PA1	PA0	Partition Address
0	0	0	0	0000H
0	0	0	1	0800H
0	0	1	0	1000H
0	0	1	1	1800H
0	1	0	0	2000H
0	1	0	1	2800H
0	1	1	0	3000H
0	1	1	1	3800H
1	0	0	0	4000H
1	0	0	1	4800H
1	0	1	0	5000H
1	0	1	1	5800H
1	1	0	0	6000H
1	1	0	1	6800H
1	1	1	0	7000H *
1	1	1	1	8000H *

*** A 4 Kbyte Increment (not 2 Kbytes) in the Partition Address takes place between bit field values 1110B and 1111B.**

Initialization: Set to all 1's on a No V_{LI} Power On Reset or when the Security Lock bit is cleared to a 0 from a previous 1 state. These bits are also set to all 1's when any attempt is made to have them cleared to all 0's with the SL bit set to a 1 (illegal condition).

Read Access: Can be read anytime.
Write Access: PAA bit must = 1 in order to write PA3-0. Timed Access is not required to write to PA3-0 once PAA = 1.

MCON.3: RA32/8
"Range Address": Sets the maximum usable address in Embedded Memory.
RA32/8 = 0 sets Range Address = 1FFFH (8K).
RA32/8 = 1 sets Range Address = 7FFFH (32K).

Initialization: Set to a 1 during a No V_{LI} Power On Reset and when the Security Lock bit (SL) is cleared to a 0 from a previous 1 state. Remains unchanged on all other types of resets.
Read Access: Can be read normally anytime.
Write Access: Cannot be modified by the application software; can only be written during Program Load Mode.

MCON.2: ECE2
"Enable Chip Enable 2": Used to enable or disable the CE2\ signal to additional Embedded RAM data memory space. This bit should always be cleared to 0 in the DS5000-8 and DS5000-32 versions.
Initialization: Cleared to 0 only during a No V_{LI} Power On Reset.
Read Access: Read normally anytime.
Write Access: Can be written normally at any time.

MCON.1: PAA
"Partition Address Access": Used to protect the programming of the Partition Address select bits. PA3-0 cannot be written when PAA = 0. PAA can be written only via the Timed Access register.
Initialization: PAA is cleared only on a No-V_{LI} Power On Reset.
Read Access: PAA can be read anytime.
Write Access: The Timed Access register must be used to perform any type of write operation on the PAA bit .

TIMED ACCESS REGISTER

Label: TA **Register Address: 0C7H**

D7	D6	D5	D4	D3	D2	D1	D0

Bit Description:

TAn.n: (All Timed Access bits)

"Timed Access": Used to invoke a Timed Access procedure required to write to any of the Timed Access protected bits including EWT, RWT, STOP, PAA. Timed Access is activated by three sequential write operations as in the example shown below:

```
MOV   0C7H, 0AAH      ; Write 0AAH to TA register
MOV   0C7H, 055H      ; Write 055H to TA register
ORL   IP,#80H         ; Reset Watchdog Timer
```

Initialization: Written with the value of 055H following any type of reset.
Read Access: Cannot be read from the application software.

PROGRAM LOAD MODES

The Program Load Modes allow initialization of the embedded program/data memory and non-volatile internal registers. This initialization can be performed in one of two ways:

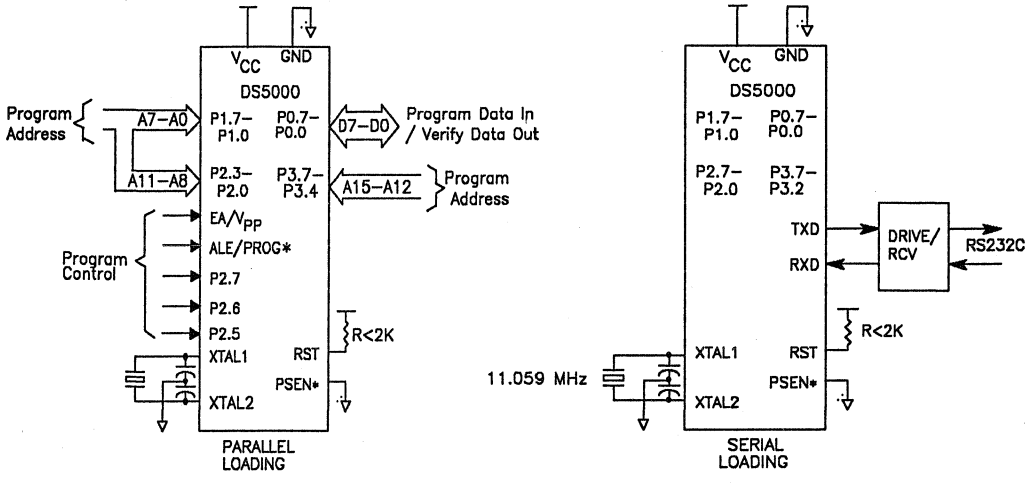
1) Serial Program Loading which is capable of performing bootstrap loading of the DS5000. This feature allows the loading of the application program to be delayed until the DS5000 is installed in the end system.

2) Parallel Program Load cycles which perform the initial loading from parallel address/data information presented on the I/O port pins. This mode is timing-set compatible with the 8751H microcontroller programming mode.

The DS5000 is placed in its Program Load configuration by simultaneously applying a logic 1 to the RST pin and forcing the PSEN\ line to a logic 0 level. Immediately following this action, the DS5000 will look for a Parallel Program Load pulse, or a serial ASCII carriage return (0DH) character received at 9600, 2400, 1200, or 300 bps over the serial port.

The hardware configurations used to select these modes of operation are illustrated in Figure 2.

PROGRAM LOADING CONFIGURATIONS Figure 2



The table below summarizes the selection of the available Parallel Program Load cycles. Figure 5 illustrates the timing associated with these cycles.

PARALLEL PROGRAM LOAD CYCLES Table 2

Mode	RST	PSEN\	PROG\	EA\	P2.7	P2.6	P2.5
Program	1	0	0	VPP	1	0	X
Security Set	1	0	0	VPP	1	1	X
Verify	1	X	X	1	0	0	X
Prog Expanded	1	0	0	VPP	0	1	0
Verify Expanded	1	0	1	1	0	1	0
Prog MCON or key registers	1	0	0	VPP	0	1	1
Verify MCON reg	1	0	1	1	0	1	1

The Program Cycle is used to load a byte of data into a register or memory location within the DS5000. The Verify Cycle is used to read this byte back for comparison with the originally loaded value to verify proper loading. The Security Set Cycle may be used to enable and disable the Software Security feature of the DS5000. One may also enter bytes for the MCON register or for the 5 encryption registers using the Program MCON cycle. When using this cycle, the absolute register address must be presented at Ports 1 and 2 as in the normal Program cycle (Port 2 should be 00H). The MCON contents can likewise be verified using the Verify MCON cycle.

When the DS5000 first detects a Parallel Program Strobe pulse or a Security Set Strobe pulse while in the Program Load Mode following a Power On Reset, the internal hardware of the

DS5000 is initialized so that an existing 4 Kbyte program can be programmed into a DS5000 with little or no modification. This initialization automatically sets the Range Address for 8 Kbytes and maps the lowest 4 Kbyte bank of Embedded RAM as program memory. The next 4 Kbytes of Embedded RAM are mapped as Data Memory.

In order to program more than 4 Kbytes of program code, the Program/Verify Expanded cycles can be used. Up to 32 Kbytes of program code can be entered and verified. Note that the expanded 32Kbyte Program/Verify cycles take much longer than the normal 4 Kbyte Program/ Verify cycles.

A typical parallel loading session would follow this procedure. First, set the contents of the MCON register with the correct range and partition only if using expanded programming cycles. Next, the encryption registers can be loaded to enable encryption of the program/data memory (not required). Then, program the DS5000 using either normal or expanded Program cycles and check the memory contents using Verify cycles. The last operation would be to turn on the security lock feature by either a Security Set cycle or by explicitly writing to the MCON register and setting MCON.0 to a 1.

SERIAL BOOTSTRAP LOADER

The Serial Program Load Mode is the easiest, fastest, most reliable, and most complete method of initially loading application software into the DS5000's nonvolatile RAM. Communication can be performed over a standard asynchronous serial communications port. A typical application would use a simple RS-232C serial interface to program the DS5000 as a final production procedure. The hardware configuration which is required for the Serial Program Load mode is illustrated in Figure 2. *Port pins 2.7 and 2.6 must be either open or pulled high to avoid placing the DS5000 in a parallel load cycle.* Although an 11.0592 MHz crystal is shown in Figure 2, a variety of crystal frequencies and loader baud rates are supported, shown in Table 3. The serial loader is designed to operate across a three-wire interface from a standard UART. The receive, transmit, and ground wires are all that are necessary to establish communication with the DS5000.

The Serial Bootstrap Loader implements an easy-to-use command line interface which allows an application program in an Intel Hex representation to be loaded into and read back from the device. Intel Hex is the typical format which existing 8051 cross-assemblers output. The serial loader responds to 11 single character commands which are summarized below:

COMMAND	FUNCTION
C	Return CRC-16 checksum of Embedded RAM
D	Dump Intel Hex File
F	Fill Embedded RAM block with constant
K	Load 40-bit Encryption Key
L	Load Intel Hex File
R	Read MCON register
T	Trace (Echo) incoming Intel Hex data
U	Clear Security Lock
V	Verify Embedded RAM with incoming Intel Hex
W	Write MCON register
Z	Set Security Lock

SERIAL LOADER BAUD RATES FOR DIFFERENT CRYSTAL FREQUENCIES*
Table 3

Crystal freq (MHz)	Baud Rate				
	300	1200	2400	4800	9600
16.000000		Y	Y		
15.000000		Y	Y	Y	Y
14.318180		Y	Y	Y	Y
12.000000		Y	Y	Y	
**11.059200	Y	Y	Y	Y	Y
11.000000	Y	Y	Y	Y	Y
10.000000		Y	Y	Y	
**9.216000	Y	Y	Y	Y	Y
8.000000		Y			
**7.372800	Y	Y	Y	Y	Y
6.144000	Y	Y	Y		
6.000000	Y	Y	Y		
5.990400	Y	Y	Y		
5.120000	Y	Y	Y		
5.068800	Y	Y	Y		
5.000000	Y	Y	Y		
4.915200	Y	Y	Y		
4.608000	Y	Y	Y	Y	
4.433620	Y	Y	Y	Y	
4.194300	Y				
4.096000	Y				
4.032000	Y				
3.579545	Y	Y	Y	Y	Y
2.457600	Y	Y			
2.000000	Y				
**1.843200	Y	Y	Y	Y	Y

*Y indicates that the baud rate for that particular crystal is supported by the DS5000 serial loader auto-baud detection scheme.
** Indicates exact generation of 9600 baud.

POWER MANAGEMENT

The DS5000 is implemented using CMOS circuitry for low-power consumption during full operation. Two software initiated modes are available for further power reduction for times when processing is not required and V_{CC} is at normal operating voltage. These are the Idle and Stop Modes. In addition, internal control circuitry automatically places the the DS5000 in its Data Retention Mode in the absence of V_{CC}.

The on-chip nonvolatile control circuitry monitors the V_{CC} for three below nominal operating voltage (Figure 3). When the voltage drops below the Power Fail Warning threshold (V_{PFW}) an interrupt will be generated to signal the processor of an impending power-fail condition. This is to allow time for a service routine to save the operational state of the microcontroller prior to the V_{CC} dropping below the V_{CCmin} threshold. When this occurs, processor operation is automatically terminated by internally halting the clock after the entire circuit has been made ready for the Data Retention Mode. Finally, once the V_{CC} voltage drops below the lithium cell voltage threshold (V_{LI}) power from the embedded lithium cell is applied to place the device in its Data Retention Mode.

When V_{CC} voltage is again applied to the system, an internal Power On Reset cycle is executed without the need for any external components on the RST pin. In addition, internal status is available to distinguish the Power On Reset from other types of resets.

SOFTWARE SECURITY

The Software Security feature is implemented using Address and Data Encryptor circuitry which is present on the DS5000 die. Operation of the Software Security feature is performed by manipulation of the 40-bit Encryption Key word and the Security Lock bit while in one of the Program Load modes. Encryption operation is first intiated by loading the 40-bit Encryption Key word.

When Software Encryption Operation is in effect and the Security Lock is disabled, the application software can be initially stored in an encrypted form during the initial loading of the device using one of the Program Load modes. As the loading is performed, the Data Encryptor logic transforms the opcode, operand, and data byte defined at each memory location defined by the software. Similarly, the Address Encryptor translates the "logical" address of each location into an encrypted address at which the byte is actually stored. Although each encryptor uses its own algorithm for encrypting data, both depend on the 40-bit key word which is contained in the Encryption Key registers (EK0-4).

As long as the Security Lock remains disabled, the actual unencrypted contents of the embedded Program/Data RAM can be read back for verification while in the Program Load mode. Once the contents have been verified, the final action performed during the Program Load mode should be the enabling of the Security Lock bit. From this point on it will be impossible to read back the unencrypted contents of the Program/Data RAM or the contents of the Encryption Key registers.

When the application software is executed, the Address and Data Encryptors provide the opcodes, operands, and data to the CPU so that execution of the application software can take place as normal. This action also takes place in real time so that no additional delays are imposed on the execution time of the software. Thus, the Software Encryption Operation is transparent to the application software.

The Software Encryption Operation is disabled and the contents of the Encryption Key registers are automatically erased whenever the Security Lock bit is cleared to a 0 from a previous 1 condition. This action renders the contents of the embedded Program/Data RAM useless, so that the application software can no longer be correctly interpreted by the DS5000 CPU. Although the contents of the Program/Data RAM can at this point be read back in a Program Load

mode, they cannot be de-encrypted since the original 40-bit key word has been lost.

ADDITIONAL INFORMATION

A complete description for all operational aspects of the DS5000, including an instruction set description, timing details, and electrical specifications, is available in the DS5000 Soft Microcontroller User's Guide.

DEVELOPMENT SUPPORT

Dallas Semiconductor offers a kit package for developing and testing user code. The DS5000TK Evaluation Kit allows the user to download Intel hex formatted code directly to the DS5000 from a PC-XT/AT or compatible computer. The kit consists of a DS5000-32-12, an interface pod, demo software, and an RS-232 connector that attaches to the COM1 or COM2 serial port of a PC. See the DS5000TK data sheet for further details.

SELECTED ELECTRICAL CHARACTERISTICS

The following are selected electrical operating characteristics of the DS5000. A full set of electrical characteristics is available in the Soft Microcontroller User's Guide.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.1 to +7.0V
Operating Temperature	0° to 70° C
Storage Temperature	-40° C to +70° C
Soldering Temperature	260° C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (t_A = 0° C to 70° C; V_{CC} = 5V ± 10%)

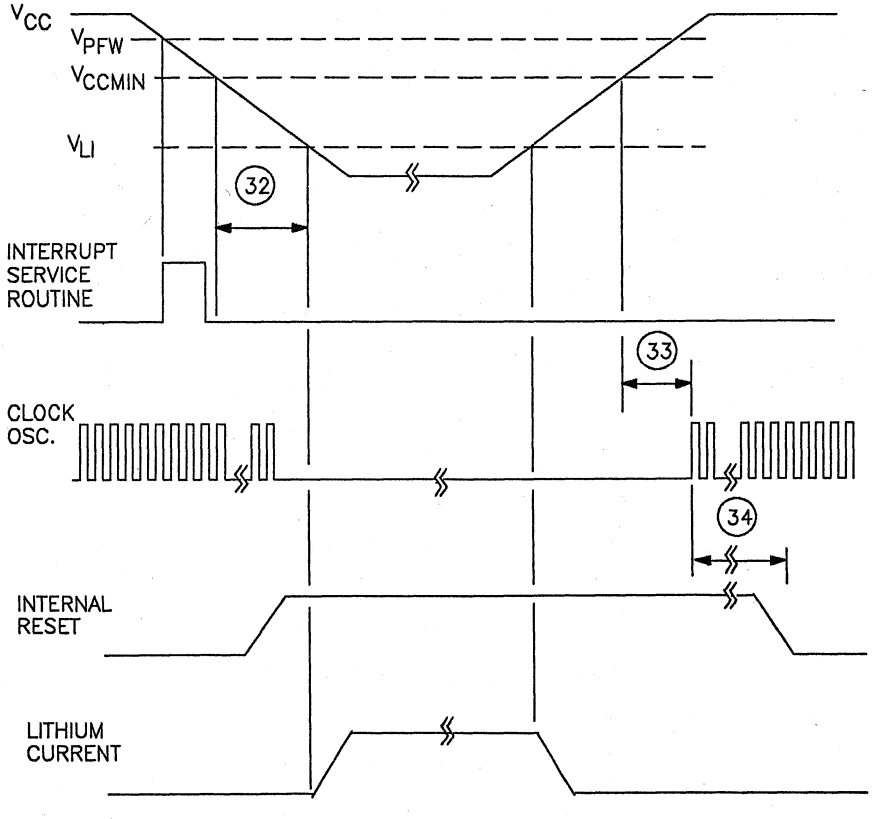
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
Stop Mode Current	I_{SM}			80	uA	4
Power Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	
Lithium Supply Voltage	V_{LI}			3.3	V	
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13.0	V	
Program Supply Current	I_{PP}		9.2	15	mA	
Operating Current DS5000-8 DS5000-32	I_{CC}		20 25	43.2 48.2	mA	
Idle Mode Current	I_{CC}			6.2	mA	

AC CHARACTERISTICS
POWER CYCLING TIMING

(t_A = 0°C to 70°C; V_{CC} = 5V ±10%)

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
32	Slew rate from V_{CCmin} to V_{LImax}	t_F	40		µs
33	Crystal Start-up Time	t_{CSU}	(note 5)		
34	Power On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLING TIMING DIAGRAM Figure 3

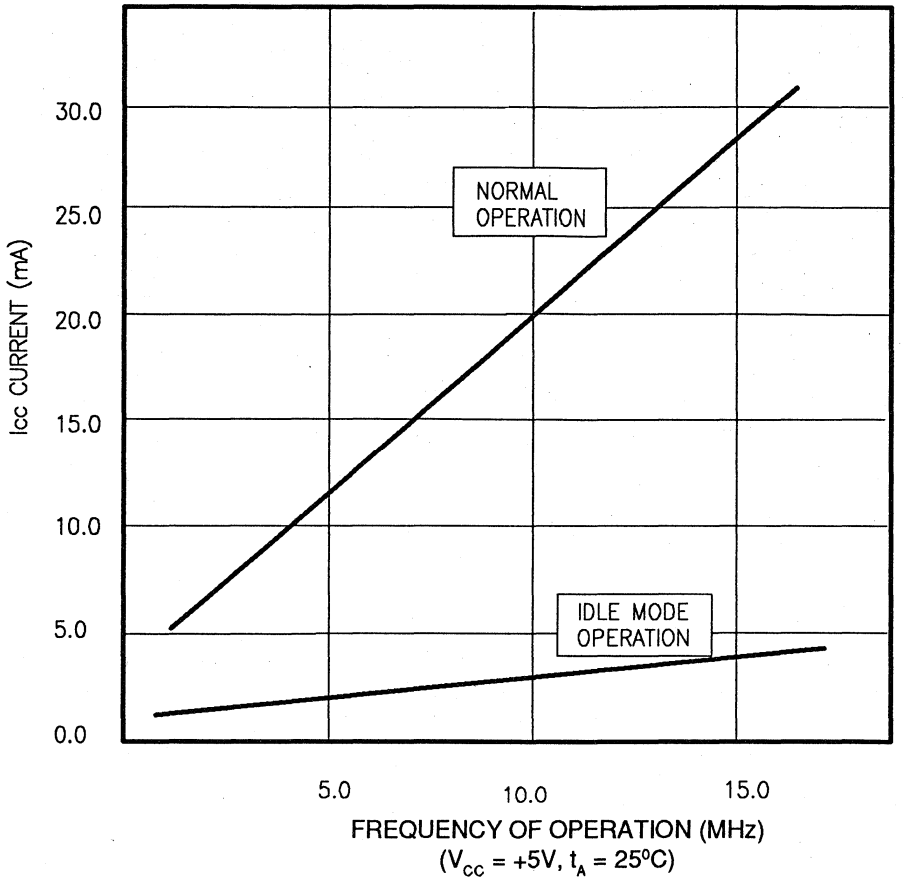


AC CHARACTERISTICS
PARALLEL PROGRAM LOAD TIMING

(t_A= 0°C to 70°C; V_{CC}= 5V +/-10%)

#	PARAMETER	SYMBOL	MIN.	MAX.	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to PROG\ Low	t_{AVPRL}	0		t_{CLK}
42	Address Hold After PROG\ High	t_{PRHAV}	0		t_{CLK}
43	Data Setup to PROG\ Low	t_{DVPRL}	0		t_{CLK}
44	Data Hold After PROG* Low	t_{PRHDV}	0		t_{CLK}
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P2XHVP}	0		t_{CLK}
46	V_{PP} Setup to PROG\ Low	t_{VPHPRL}	0		t_{CLK}
47	V_{PP} Hold After PROG\ Low	t_{PRHVPI}	0		t_{CLK}
48	PROG\ Width Low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK} t_{CLK}
50	P2.7, 2.6 Active to Data Valid	t_{DVP2XA}		48 1800*	t_{CLK} t_{CLK}
51	Data Hold after P2.7, 2.6 Inactive	t_{P2XHDI}	0	48 240*	t_{CLK} t_{CLK}
52	Delay to Reset/PSEN\ Active after Power On	t_{PORPV}	26304		t_{CLK}
53	Reset/PSEN\ Active (or Verify inactive) to V_{PP} High		1200		t_{CLK}
54	V_{PP} Inactive (between Program cycles)		1200		t_{CLK}
55	Verify Active Time	t_{VFT}	48 2400		t_{CLK} t_{CLK}

DS5000 Icc vs. FREQUENCY Figure 4



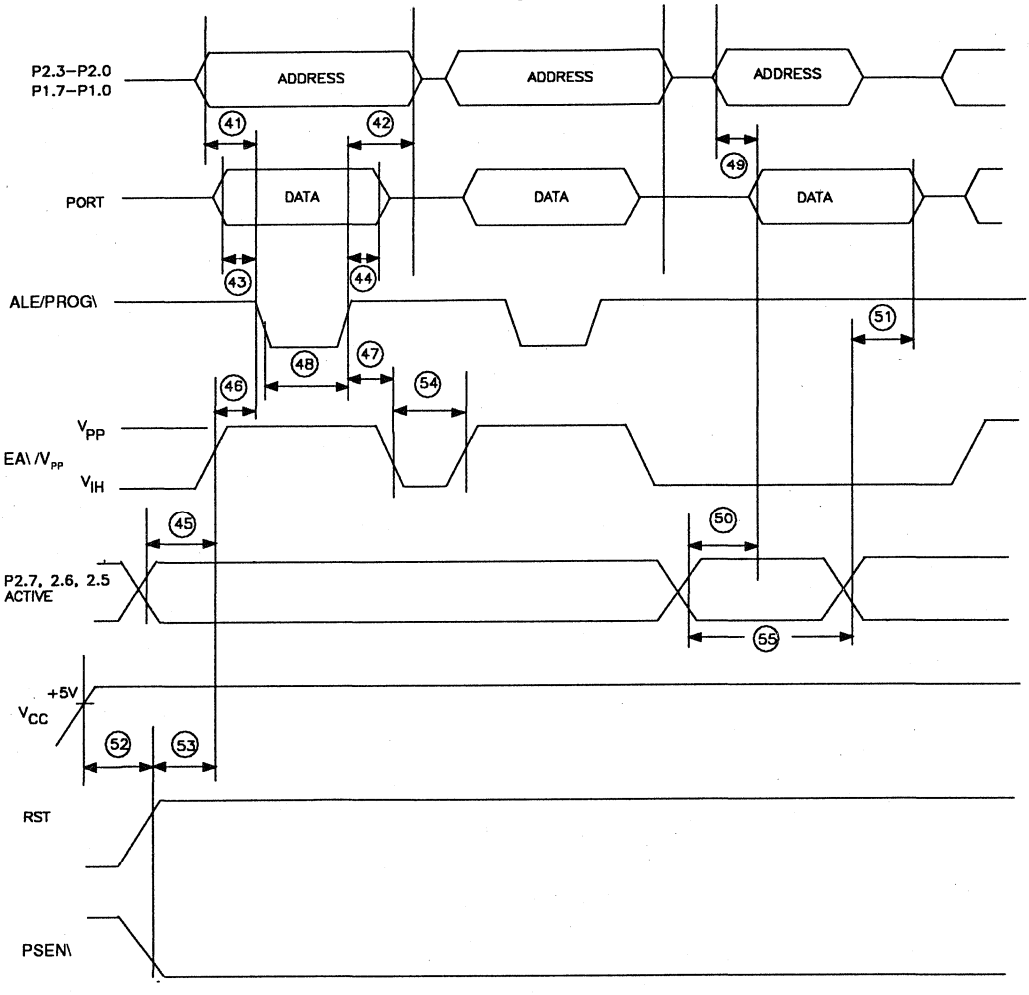
Normal operation is measured using:

1) External crystals on XTAL1 and 2.
2) All port pins disconnected.
3) RST = 0 Volts and EA = Vcc.
4) Part performing endless loop writing to internal memory.

Idle mode operation is measured using:

1) External clock source at XTAL1; XTAL2 floating.
2) All port pins disconnected.
3) RST = 0 Volts and EA = Vcc.
4) Part set IDLE mode by software.

PARALLEL PROGRAM LOAD TIMING Figure 5



NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} =0.5V, V_{IH}= 4.5V; XTAL2 disconnected; EA\ = RST = PORT0 = V_{CC}.
3. Idle Mode I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V, V_{IH} = 4.5V; XTAL2 disconnected; EA\=RST=PORT0=V_{CC}.
4. Stop Mode I_{CC} is measured with all output pins disconnected; EA\=PORT0=V_{CC}; XTAL2 not connected; RST = V_{SS}.
5. Crystal start-up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst case spec on this time.

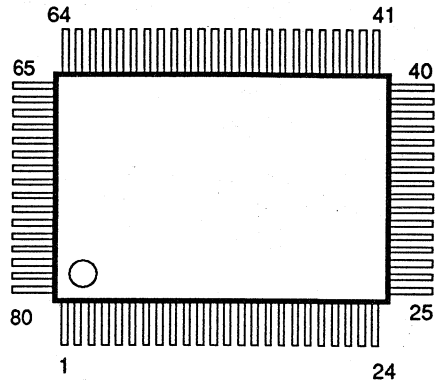
DALLAS SEMICONDUCTOR

DS5000FP
Micro Chip

FEATURES

- Offers the microcontroller die used in the DS5000 Soft Microcontroller DIP packaged in an 80-pin Quad Flat Pack (QFP)
- Provides access to bytewide address/data bus, not available on the DS5000 DIP
- Bytewide address/data bus frees up port pins for I/O use
- Direct interface to bytewide memories
- Supports up to 64 Kbytes of program/data memory
- Incorporates battery switching/monitoring circuitry for powering external memory devices in the absence of Vcc
- Ultra-low standby current--less than 75 nA
- Watchdog timer ensures program control
- Fully compatible with 8051 instruction set

PACKAGE DESCRIPTION



80-Pin Quad Flat Pack

ORDERING INFORMATION

DS5000FP-XX	-08	08 MHz
	-12	12 MHz
	-16	16MHz

DESCRIPTION

The DS5000FP Micro Chip is an 80-pin Quad Flat Pack (QFP) containing a standalone DS5000 Soft Microcontroller die which normally resides in a 40-pin DS5000 DIP package. It retains all the hardware features of a DS5000 DIP and can be used much like ROM-less versions of the 8051, except that all four ports of the DS5000FP are freed up for general-purpose I/O. An external lithium energy cell can be attached to this chip to power external SRAM(s) in the absence of Vcc. This gives the user the flexibility of using his own lithium cells and memories to implement a nonvolatile microcontroller solution with the soft features inherent in the DS5000 DIP. EPROM devices can be used for program memory in applications not requiring reloadable software.

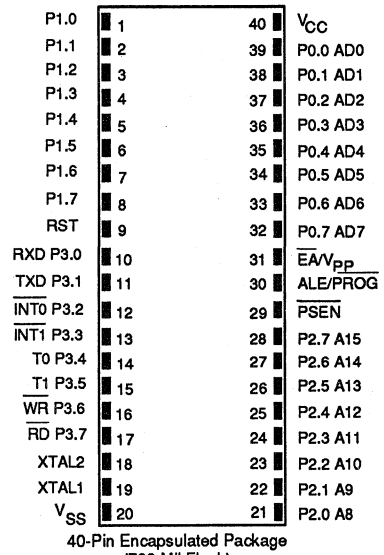
Of the 80 pins on the package, only 68 are actually tied to pads on the die. The rest of the pins are no-connects. 40 pins of the 68 signal pins are identical in function to the 40 pins of a standard DS5000. The other 28 pins are normally used to interface to the embedded RAM and the lithium source on the standard DS5000 DIP products. For complete information, refer to the Soft Microcontroller User's Guide.

DALLAS SEMICONDUCTOR

DS5000T
Time Microcontroller

FEATURES
- DS5000 Soft Microcontroller with embedded clock/calendar
- Internal lithium cell preserves clock function in the absence of V_{CC}
- Permits logging of events with time and date stamp
- 8 or 32 Kbytes of embedded nonvolatile program/data RAM
- Program loading via on-chip full-duplex serial port
- User-selectable program/data memory partition
- All 4 ports available for system control
- Resident encryptor protects program from piracy
- Power sequencer and watchdog timer help ensure crashproof operation
- Compatible with industry standard 8051 instruction set and pinout
- Clock accuracy is better than 2 min/month @25°C

PIN CONNECTIONS



40-Pin Encapsulated Package
(700 Mil Flush)

ORDERING INFORMATION

DS5000T xx - yy

xx	Program/Data RAM	
	08	8 Kbytes
	32	32 Kbytes
yy	Clock Frequency	
	08	8 MHz
	12	12 MHz
	16	16 MHz

DESCRIPTION

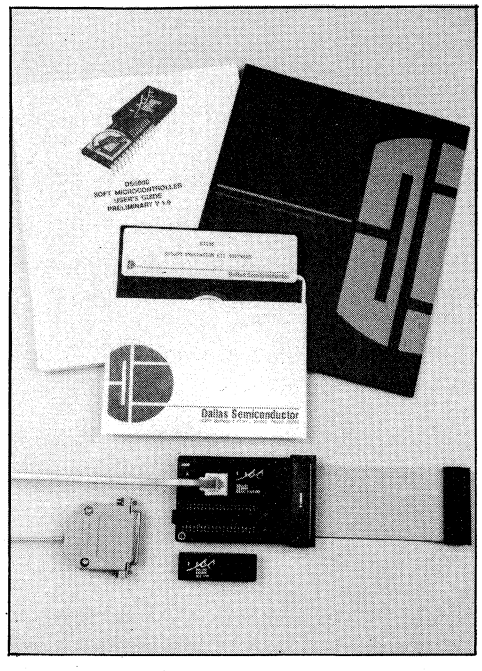
The DS5000T Time Microcontroller offers all the features of the DS5000 Soft Microcontroller with the added benefit of an embedded real-time clock/calendar function. The clock function itself is accessed as though it were a part of the embedded data RAM so that the 32 I/O pins are free for the application use. With this feature, new and existing microcontroller systems can now log events, schedule activities, and time operations. The combination of DS5000T's soft features together with a real-time clock/calendar provides a powerful controller that adapts to the needs of time-driven applications.

For complete information, see the DS5000 User's Guide.

DALLAS SEMICONDUCTOR

DS5000TK
Time Micro Evaluation Kit

FEATURES
- Allows immediate evaluation of DS5000T Time Microcontroller or DS5000 Soft Microcontroller in an existing application
- Supplied with DS5000T 32, software diskette, DS5000 User's Guide, and In-System Loader hardware
- Supports in-system serial downloading of DS5000T from an IBM PC host
- DS5000T supports all functions of DS5000 with addition of real-time clock
- Downloads/verifies Intel Hex absolute object files residing on IBM PC
- User-friendly software prompts user for required system configuration information
- Supports serial download rates up to 19200 bps
- Requires no support circuit overhead on target system



DESCRIPTION
The DS5000TK Time Micro Evaluation Kit is a development support system which is designed to allow immediate evaluation of the DS5000T Time Microcontroller in a system application. The DS5000TK is an upgraded version of the DS5000K. Since the DS5000T performs all of the functions associated with the DS5000 Soft Microcontroller, it can also be used for evaluation of any of the versions of a DS5000 for a new or existing design.

Materials provided with the kit include a DS5000T with 32 Kbytes of RAM, full documentation on the DS5000 and DS5000T, In-System Loader serial download hardware, and software for the IBM PC (KIT5K). Using the Evaluation Kit, the user can quickly configure the DS5000T for operation in the target system. This configuration can be performed without detailed knowledge of the operation of the DS5000's Serial Load Mode. The DS5000TK Evaluation Kit not only serves as a first-time evaluation system for the DS5000 or the DS5000T, but also performs the equivalent function of an EPROM programming system throughout the prototyping phase of the design cycle.

Adaptors are available for development with the DS2250 Soft Micro Stik and the DS2250T Time Micro Stik. For information on these see the DS907x data sheet. For complete information, refer to DS5000 User's Guide.

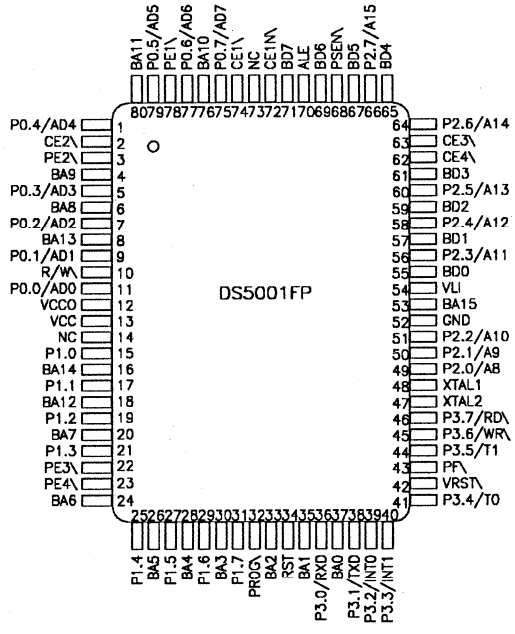
DALLAS SEMICONDUCTOR

DS5001FP
128K Micro Chip

FEATURES

- Enhanced CMOS microcontroller addresses up to 128K of NV SRAM for program/data
- Bytewide address/data bus leaves port pins for general-purpose I/O
- Multiple chip select outputs for memory-mapping of peripheral devices
- Crashproof circuitry converts CMOS SRAM into nonvolatile storage
- Reprogrammable Peripheral Controller (RPC) mode emulates 8042 for PC bus applications
- Increased flexibility in program loading
- Optional CRC-16 check of NV program/data RAM area on power-up or watchdog reset
- Bandgap reference provides tight power supply monitoring
- 100% compatible with 8051 instruction set
- 80-pin Quad Flat Pack (QFP) surface mount package

PIN CONNECTIONS



80-Pin Quad Flat Pack

DESCRIPTION

The DS5001FP 128K Micro Chip is an enhanced version of the DS5000FP Micro Chip. The DS5001FP is designed for systems with large nonvolatile SRAM and I/O requirements; its separate bytewide address/data bus accesses up to 128K bytes of nonvolatile SRAM for program/data storage. In addition, four peripheral enables allow additional I/O devices to be memory-mapped onto the bytewide bus without the need for external logic. Thus, even in the most complex systems, the 8051-compatible ports are free for general-purpose I/O. When combined with an appropriate external lithium energy cell, the DS5001FP's crashproof circuitry retains programs and data in external SRAM for 10 years in the absence of V_{CC}.

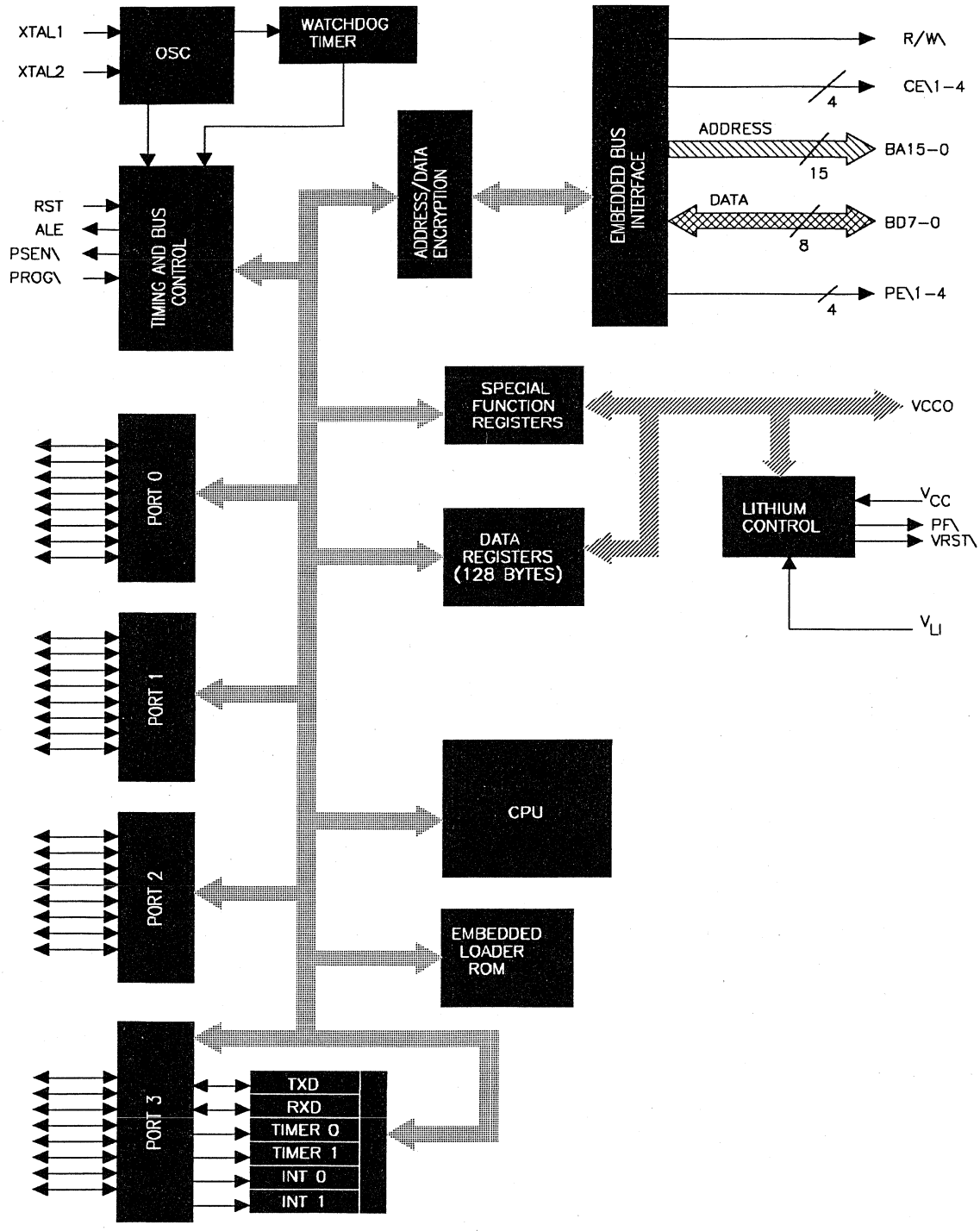
Compared to its predecessor, the DS5000 Soft Microcontroller, the DS5001FP incorporates memory capacity and flexibility enhancements, additional I/O resources, and new software loading features. Memory improvements include the ability to address 128K bytes of NV SRAM on the bytewide bus, multiple memory architectures for optimum implementation, and a peripheral memory map. Substantial flexibility in memory selection is provided by the DS5001FP's unique architecture, which allows the most cost-effective memory selection to be used.

I/O flexibility is provided by the Reprogrammable Peripheral Controller (RPC). This is an 8042 hardware emulation mode that allows the DS5001FP to act as a slaved peripheral controller for PC bus applications. When the RPC is not in use, port I/O which is fully compatible with the 80C51 remains available. Additional I/O flexibility results from the ability to address external peripheral devices on the bytewide bus, which allows the ports to be used for other functions. If desired, ports 0 and 2 can be configured for bus access similar to the 8051.

The DS5001FP supervises program loading via an internal bootstrap loader ROM. This loader allows the entire RAM memory space and certain configuration registers to be initialized from a PC via a com port. The bootstrap loader is transparent to the execution of application software. Alternatively, bootstrap loading can be performed via the parallel RPC bus. In this way, a system host such as an 8088 CPU can download application software over a PC bus.

The DS5002FP Secure Micro Chip offers the features of the DS5001FP together with software security features which have been greatly enhanced over the DS5000. Consult the DS5002FP data sheet for information on this device.

BLOCK DIAGRAM OF THE DS5001FP Figure 1



PIN DESCRIPTION
(\ Denotes Condition Low)

SIGNAL	I/O	DESCRIPTION
V_{CC}	I	Primary V_{CC} input from power supply.
V_{LI}	I	Lithium Voltage Input.
GND	I	Ground.
PF\	O	Indicates that V_{CC} has dropped below the battery voltage.
V_{CCO}	O	Voltage Output to CMOS SRAM V_{CC} pin.
VRST\	I/O	Indicates that V_{CC} has dropped below the reset threshold. Also forces a power-fail reset when pulled low externally.
CE1-4\	O	SRAM Chip Enables, lithium backed. Used with bytewide address/data bus to access bytewide memory.
CE1N\	O	Chip Enable 1. Non-lithium-backed signal equivalent to CE1\ for use with an EPROM.
PE1-2\	O	Peripheral Enables, lithium-backed.
PE3-4\	O	Peripheral Enables, non-lithium backed chip enables which access memory-mapped peripheral devices on the bytewide bus. Available when the PES bit in the MCON register is set.
R/W\	I/O	Write enable for bytewide bus access.
BA15	O	Bytewide address bus MSB. Used to monitor complete bus address, but not connected to memories.
BA14-0	O	Bytewide address bus. 15-bit bus is connected to NV SRAM and peripheral devices using PE1-4\.
BD7-0	I/O	Bytewide data bus connected to NV SRAM and peripheral devices.
PROG\	I	Invokes bootstrap loading on a falling edge.
RST	I	Reset input.
XTAL2	I	Crystal 2 Input.
XTAL1	I	Crystal 1 Input.
PSEN\	O	Program Store Enable.
ALE	O	Address Latch Enable.
P0.0-0.7 /AD0-7	I/O	General purpose Port 0 bits 0-7; multiplexed expanded address/data bus and RPC mode data bits 0-7. an 8051 compatible 8-bit port. Port 0 is RPC bus is an optional 8042 compatible hardware interface.
P1.0-1.7	I/O	General purpose Port 1 bits 0-7.
P2.0-P2.7 /A8-A15	I/O	General purpose Port 2 or Expanded address bus. Port 2 can also function as RPC control signals as follows:
P2.0 A0	I	Data/Status select input.
P2.1 CE\	I	RPC mode chip select input.
P2.2 RD\	I	RPC mode read enable.
P2.3 WR\	I	RPC mode write enable input.
P2.4 OBF	O	RPC mode output buffer full.
P2.5 IBF\	O	RPC mode input buffer full.
P2.6 DRQ	O	RPC mode request for DMA.
P2.7 DACK\	I	RPC mode DMA acknowledge input.
P3.0/RXD	I/O	General purpose Port 3 bit 0 and serial port receive data input.
P3.1/TXD	I/O	General purpose Port 3 bit 1 and serial port transmit data output.
P3.2/INT0\	I/O	General purpose Port 3 bit 2 and external interrupt input 0.

P3.3/INT1\	I/O	General purpose Port 3 bit 3 and external interrupt input 1.
P3.4/T0	I/O	General purpose Port 3 bit 4 and timer counter input 0.
P3.5/T1	I/O	General purpose Port 3 bit 5 and external timer counter input 1.
P3.6/WR\	I/O	General purpose Port 3 bit 6 and expanded bus write enable.
P3.7/RD\	I/O	General purpose Port 3 bit 7 and expanded bus read enable.

The following discussion provides information specifically about the DS5001FP. Consult the Soft

Microcontroller User's Guide for a complete explanation of the basic DS5000's features and operation.

BYTEWIDE ADDRESS/DATA BUS

The bytewide address/data bus is a separate bus structure for accessing off-chip program and data memory. In ordinary 8051-type processors, external program and data fetches use Ports 0 and 2 as a multiplexed address/data bus. In contrast, the DS5001FP provides a non-multiplexed, 15-bit bytewide address bus (pins BA0-BA14), four chip enables, and an 8-bit bytewide data bus (pins BD0-BD7) for interfacing to bytewide memories. Consequently, application software can address up to 64K x 8 of program memory and 64K x 8 of data memory (128K total) on the bytewide address/data bus, and still use all four ports for general-purpose I/O. In addition, a simple interface for peripheral I/O devices is supported on the bytewide bus for applications which require more I/O functions. Control signals for the bytewide bus consist of R/W\, CE1\ - CE4\ and PE1\ - PE4\. The R/W\ output is normally connected to WE\ inputs of all devices attached to the bytewide bus in order to indicate a read or write operation. Outputs CE1\ - CE4\ are used as chip enables for up to four separate memory devices. Note that CE2\ is no longer limited only to data memory fetches (initiated by MOVX instructions) as on the DS5000FP. Up to four peripheral devices can be accessed by using the software-controlled PE1\ - PE4\ chip enable outputs. BA15, which is logically equivalent to the MSB of a 16-bit bytewide address bus, is provided for convenience. This line is unused when addressing memories, as the information is decoded in the chip enables. It is provided to allow a logic analyzer to monitor a 16-bit address field.

MEMORY ORGANIZATION

The DS5001FP supports two categories of memory architecture. The first is a partitionable architecture similar to the DS5000FP. This mode is invoked when Partition Mode=0 (PM MCON.1). Figure 2 shows the memory map that is obtained when PM=0. Up to 64K of nonvolatile program/data RAM is available in a continuous memory space. The range address specifies the amount of memory addressed on the bytewide bus, and the programmable partition address determines the boundary between nonvolatile program space and data space. Nonvolatile program and data RAM refers to RAM accessed on the bytewide bus. Addresses below the partition are assigned as nonvolatile program RAM. Addresses above the partition and below the range are assigned as nonvolatile data RAM. The range and partition are initialized via the bootstrap loader when the application software is loaded. Table 1 illustrates the partition addresses for a 64K range. If a range of less than 64K (32K, 16K, 8K) is needed, only the relevant partitions should be used. Memory accesses outside the space defined on the bytewide bus, including program memory access above the partition, data memory access below the partition, or any access above the range, are automatically routed to the expanded bus using Ports 0 and 2.

The DS5001FP also supports setting the partition under control of the application software itself (not allowed when the partition is set to 0000H). In this partitionable configuration, CE1\ is tied to the lower RAM and CE2\ is tied to the upper RAM if needed. For any address, the DS5001FP determines which memory to enable depending on the upon the address and the

range as shown below. The single memory (range = 32K or 8K) configurations will only require CE1\. Memory range is determined by the RG1 and RG0 bits shown below (PM=0). The range control bits reside in the MCON and the RPCTL registers. A typical electrical connection for this configuration is shown in Figure 3. This figure illustrates a system using 64K SRAM consisting of two 32K devices. Lower addresses are accessed using CE1\ and higher addresses are accessed using CE2\. The address and data bus as well as the WE\ are common. Notice that by using the bytewide bus, no address decoding is required.

PM=0 RANGE SELECTIONS Table 1A

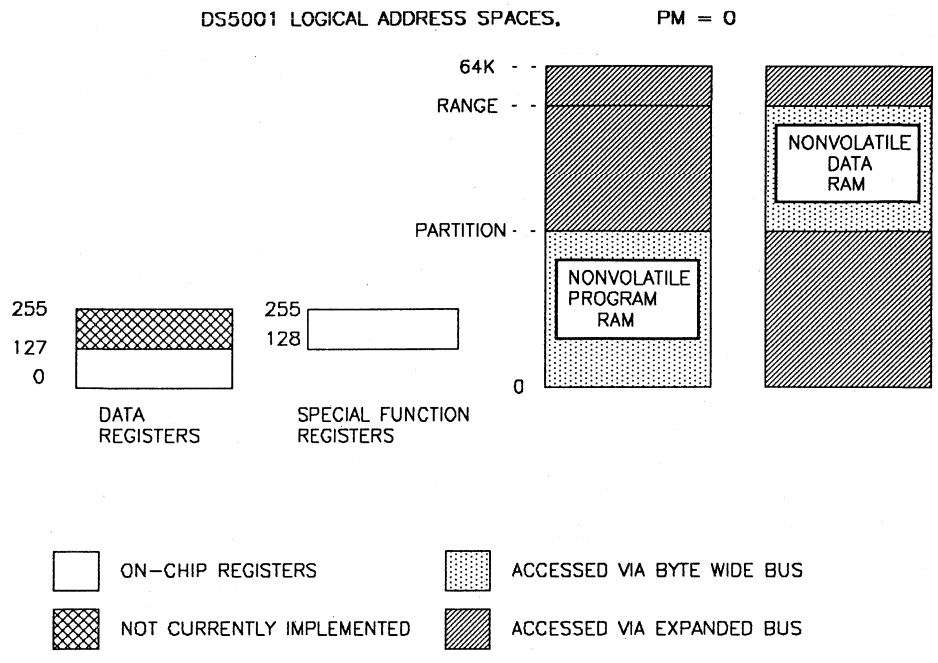
			MEMORY ACCESS ADDRESSES	
RG1	**RG0**	**RANGE**	**CE1**	**CE2**
1	1	64K	0000-7FFFH	8000-FFFFH
1	0	32K	0000-7FFFH	NA
0	1	16K	0000-1FFFH	2000H-3FFFH
0	0	8K	0000-1FFFH	NA

PM=0 PARTITION SELECTIONS Table 1B

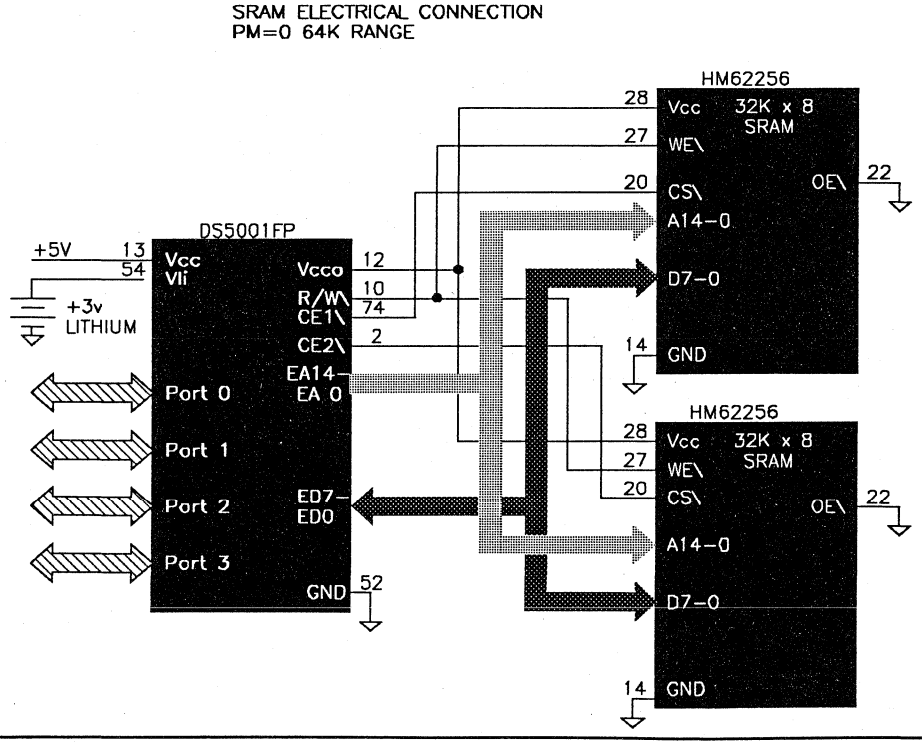
PA3	PA2	PA1	PA0	PARTITION	BYTEWIDE BUS MAP
0	0	0	0	0000H	0K PROGRAM, DATA=RANGE-0K
0	0	0	1	1000H	4K PROGRAM, DATA=RANGE-4K
0	0	1	0	2000H	8K PROGRAM, DATA=RANGE-8K
0	0	1	1	3000H	12K PROGRAM, DATA=RANGE-12K
0	1	0	0	4000H	16K PROGRAM, DATA=RANGE-16K
0	1	0	1	5000H	20K PROGRAM, DATA=RANGE-20K
0	1	1	0	6000H	24K PROGRAM, DATA=RANGE-24K
0	1	1	1	7000H	28K PROGRAM, DATA=RANGE-28K
1	0	0	0	8000H	32K PROGRAM, DATA=RANGE-32K
1	0	0	1	9000H	36K PROGRAM, 28K DATA
1	0	1	0	A000H	40K PROGRAM, 24K DATA
1	0	1	1	B000H	44K PROGRAM, 20K DATA
1	1	0	0	C000H	48K PROGRAM, 16K DATA
1	1	0	1	D000H	52K PROGRAM, 12K DATA
1	1	1	0	E000H	56K PROGRAM, 8K DATA
1	1	1	1	FFFFH	64K PROGRAM, 0K DATA

NOTE: an 8K increment takes place between E000H and FFFFH

MEMORY MAP OF THE DS5001FP WITH PM=0 Figure 2



ELECTRICAL CONNECTION FOR PM=0 Figure 3



A powerful feature for adaptive systems is the ability to reload portions of program memory without stopping execution and entering program load mode. In the partitionable mode, the application software can reload portions of itself by moving the partition to the 4K level. This allows the new application program to be received via the serial port and to be written into RAM using MOVX instructions. When loading is complete, the partition can then be raised to any desired level, converting the new data to program memory. The program kernel that performs this reloading must reside below the 4K boundary.

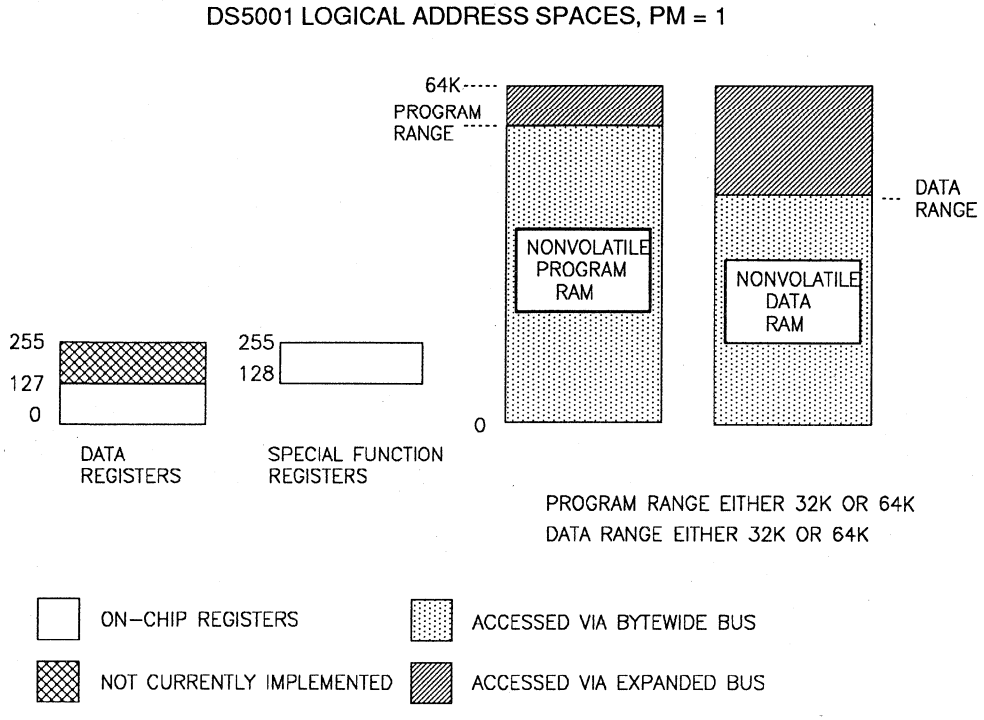
The second memory architecture includes four fixed memory choices. In this configuration, the user can determine which memory configuration provides the most cost-effective microcontroller solution. The configuration is selected by the user during bootstrap loading of the application software, by setting the PM=1 and selecting the range bits as shown below. Figure 4 illustrates the general memory map for this configuration. Note that the memory space accessed on the bytewide bus is not continuous as when PM=0. Each memory space (program and data) begins at address 0000H. Table 2 describes the configuration bits and chip enable connections for each of four fixed memory allocations. An example of this architecture is shown in Figure 5. This illustration shows a 128K system using 64K of program and 64K of data memory implemented with 32K SRAMs. CE1\ and CE2\ are used to access program memory, CE3\ and CE4\ to access data memory. The 15-bit address bus and 8-bit data bus are routed to all memories, with a common WE\. This system allows the full addressable space to be used on the bytewide bus, while leaving the ports free for other uses.

PM=1 MEMORY ARCHITECTURE Table 2

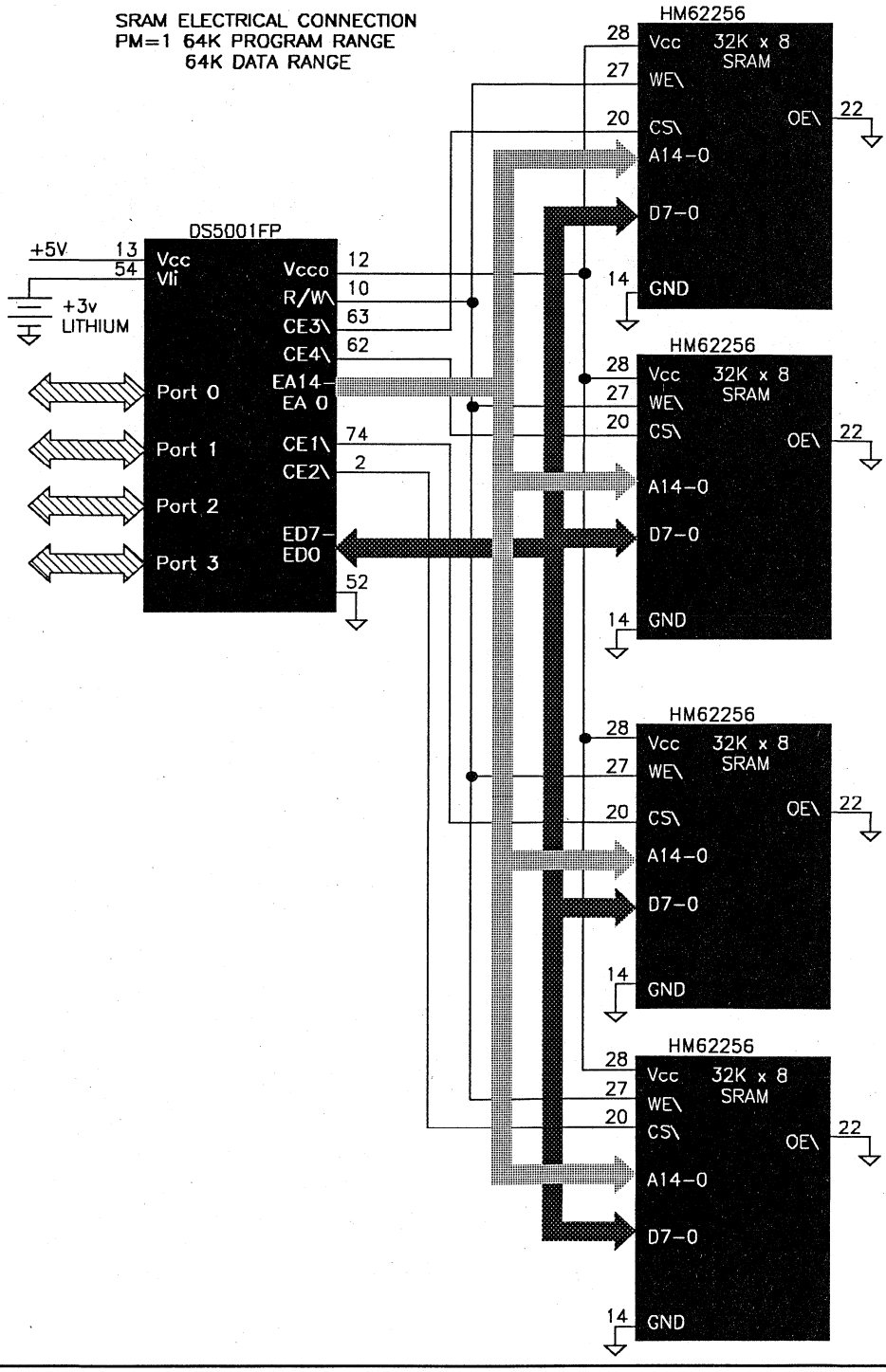
RG1	RG0	PROG	DATA	PROGRAM	DATA
0	0	32K	64K	1@32K CE\1	2@32K CE\3,4
0	1	64K	32K	2@32K CE\1,2	1@32K CE\3
1	0	64K	64K	2@32K CE\1,2	2@32K CE\3,4
1	1	64K	64K	1@128K x 8	both program and data

A special mode is available for using a 128K x 8 SRAM as shown above. In this mode, CE1\ is the chip enable and CE2\ is tied to A16. CE2\ is low when program is accessed and high when data is accessed. CE3\ is tied to A15, and CE4\ is unused. This configuration is illustrated in Figure 6. The settings that invoke this configuration are shown in the last row of Table 2 above.

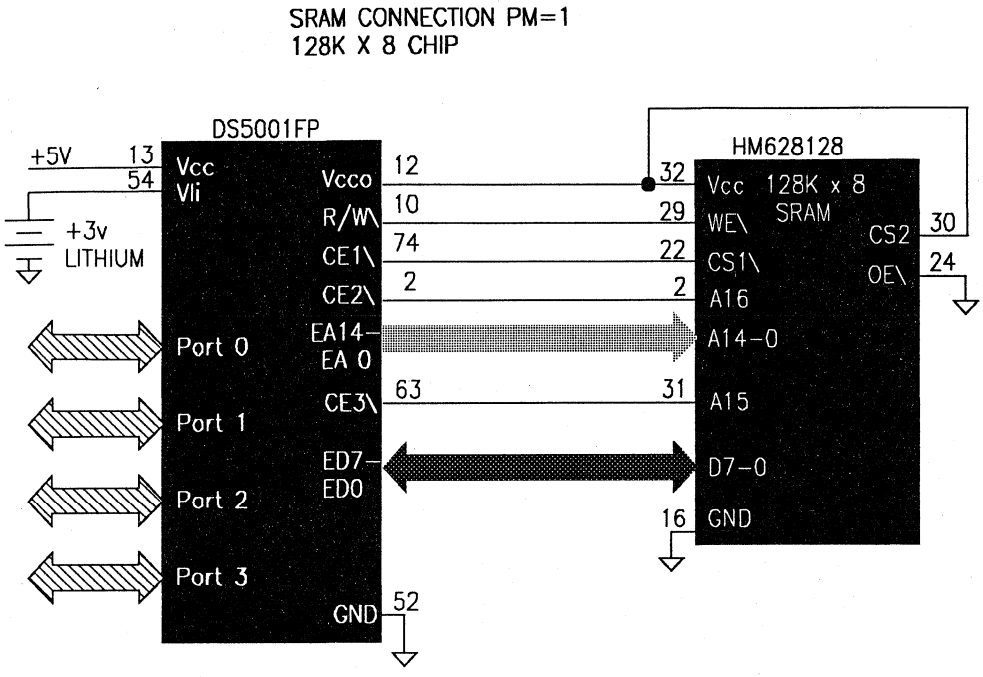
MEMORY MAP OF THE DS5001FP WITH PM=1 Figure 4



ELECTRICAL CONNECTION FOR PM=1, 32K PROGRAM, 64K DATA Figure 5



ELECTRICAL CONNECTION FOR 128K x 8 SRAM Figure 6



Portions of program memory can also be reloaded without invoking the bootstrap loader in this non-partitionable configuration. In the partitionable mode, this is accomplished by moving the partition to the 4K level. In the non-partitionable mode (PM=1), a similar feature is available when the Access Enable (AE RPCTL.4) bit is set in the RPCTL register. When AE=1, the DS5001FP will act like a partitionable device with the partition at 4K. The 64K program memory space (less the 4K kernel) may now be written using MOVX instructions. When the loading process is complete, the AE bit should be cleared, restoring the prior memory configuration.

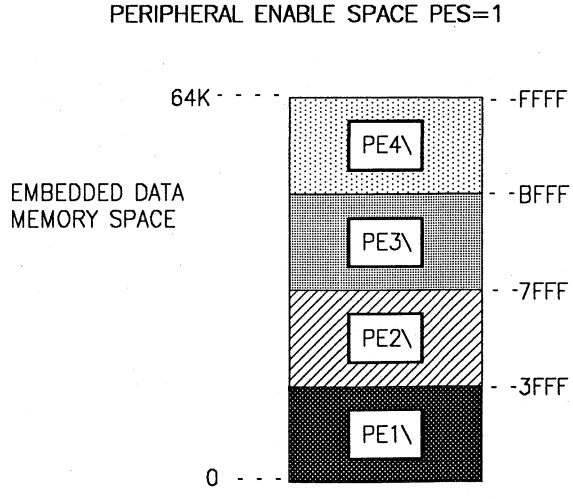
MEMORY-MAPPED PERIPHERALS

As illustrated in the above memory maps, the address space of the DS5001FP consists of 3 distinct memory areas: internal on-chip registers (128 bytes of scratchpad registers and 128 bytes of special function registers), nonvolatile program and data RAM accessed on the bytewide bus, and finally, expanded program and data memory (expanded memory is accessed via the 8051-type bus formed by Ports 0 and 2). The expanded bus is accessed automatically when either a program or data address is encountered that is outside the bytewide address configuration, determined by RG1, RG0, and the partition. It is also accessed by a MOVX instruction when the Expanded Bus Select (EXBS RPCTL.5) bit is set, regardless of the configuration. Thus using the EXBS a full 64K data memory space is available on the expanded bus without conflicting with the nonvolatile data RAM on the bytewide bus. The EXBS resides in the RPCTL register. Operation of new and modified registers is discussed on the following page.

When further memory-mapped I/O is required, an additional 64K data memory space is available on the bytewide bus. One of the new and unique features of the DS5001FP is its ability to select memory-mapped peripheral I/O devices on the bytewide bus. Four peripheral enables, PE\1-4, can be used to address up to four external devices. Each peripheral enable signal controls 16K bytes of address space in the data memory map as illustrated in Figure 7. PE1\ responds to MOVX instructions for addresses from 0000H to 3FFFH, PE2\ for addresses from 4000H to 7FFFH, etc. To use the peripheral enable signals, the Peripheral Enable Select (PES MCON.2) must be set by the application software. Once set, one of the signals PE1\ - PE4\ will transition low when a MOVX instruction uses an address in its allocated block as shown in Figure 7. Note that the blocks are mutually exclusive so that only one peripheral chip enable is active at any one time. Note also that the chip enables CE1-4\ will not be activated when a MOVX occurs as long as the PES bit is set. Thus the peripheral space does not interfere with the ordinary data memory space. The EXBS function overrides the PES function if both are selected.

Two of the peripheral enable signals, PE1\ and PE2\, are powered by the lithium cell attached to V_{LI} when V_{CC} is removed. Certain peripheral devices, such as the DS1283 Watchdog Timekeeper, as well as most CMOS SRAMs, require that the chip enable input be at the positive supply rail for minimum standby current when in lithium-backed, data retention mode. The other two enables, PE3\ and PE4\, are not lithium-backed and will drop to 0V whenever the DS5001FP has switched over to the lithium cell for powering V_{CCO}. Therefore, care must be exercised when determining which peripheral device connects to each peripheral enable.

PERIPHERAL ENABLE MAP IN THE DATA MEMORY SPACE (PES=1) Figure 7



MCON REGISTER (ADDRESS C6H)

MCON

PA3	PA2	PA1	PA0	RG1	PES	PM	–

RPS

ST7	ST6	ST5	ST4	IA0	F0	IBF	OBF

RPCTL

RNR	–	EXBS	AE	IBI	DMA	RPC	RG0

CRC

RNGE3	RNGE2	RNGE1	RNGE0	–	–	–	CRC

Bit Description:

MCON.7-4: **PA3-0**
Partition address. When PM=0, this address specifies the boundary between program and data memory in a continuous space.
Initialization: Unaffected by watchdog, external, or power-up resets. Set to 1111B on a No V_{LI} reset.
Read Access: Can be read normally at any time.
Write Access: Timed Access protected. Also, cannot be written by the application software if set to 0000B by the serial loader. If a 0000B is written via the serial loader and the security lock is set, the Partition will become 1111B. The same will occur if write access is available and application software writes a 0000B.

MCON.3: **RG1**
One of two bits that determine the range of program space. RG0 is located in the RPCTL register.
Initialization: Unaffected by watchdog, external, or power-up resets. Set to 1 on a No V_{LI} reset or a clearing of the security lock.
Read Access: Can be read at any time.
Write Access: Cannot be modified by the application software. Can only be written during program load.

MCON.2 **PES**
Peripheral Enable Select. When this bit is set, the data space is controlled by PE1\ - PE4\. Peripherals are memory-mapped in 16K blocks, and are accessed by MOVX instructions.
Initialization: Cleared by all resets.
Read Access: Can be read at any time.
Write Access: Can be written at any time.

MCON.1: **PM**
Partition Mode. When PM=0, a partitionable, continuous memory map is invoked, as described in Figure 2. When PM=1, one of four fixed allocations is used as shown in Table 2.
Initialization: Unaffected by watchdog, external, or power-up reset. Cleared on a No V_{LI} reset.
Read Access: Can be read at any time.
Write Access: Cannot be written by the application software. Can only be modified during program load.

REPROGRAMMABLE PERIPHERAL CONTROLLER (RPC)

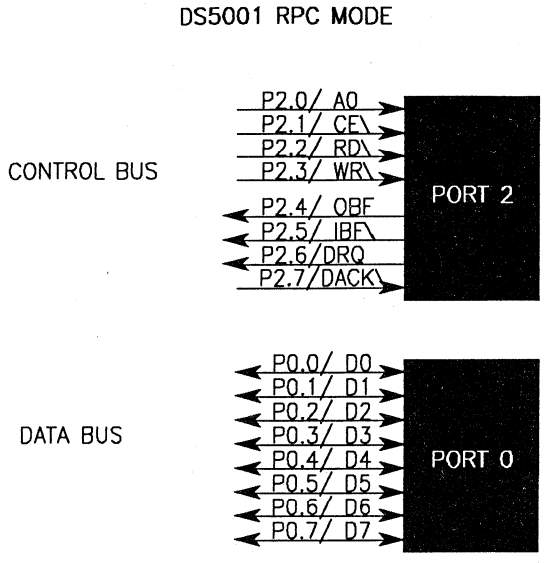
The Reprogrammable Peripheral Controller (RPC) mode of the DS5001FP emulates the 8042 slave hardware interface commonly used in IBM-compatible PCs for control of peripherals such as a keyboard or a mouse device. In addition to a direct interface to the PC backplane bus, the DS5001FP brings the advantages of up to 128K of reprogrammable, nonvolatile program and data memory to intelligent peripheral control. The nonvolatile data memory accessed by the DS5001FP can be used for system configuration, hard disk setup parameters, or even maintenance records. System peripheral developers now have the benefit of programming in the standard 8051 instruction set with its more powerful features and wider development support.

In operating as a slave controller, the DS5001FP provides communication with a host processor via three resource registers: Data Bus In (DBBIN), Data Bus Out (DBBOUT), and Status (STATUS). The host may read data or status and write data or commands. The Status register provides information about DBBIN, DBBOUT, and user-defined flags. Both DBBIN and DBBOUT share special function register address 80H with Port 0. The context will determine which register is used. The STATUS is at SFR location 0DAH.

To enable the RPC mode, the RPCON bit in the RPCTL register (described below) must be set to a 1. At this time, Ports 0 and 2 are reconfigured to emulate the 8042 hardware interface as shown in Figure 8. Port 0 becomes an 8-bit data bus that can connect directly to a PC data bus. Port 2 provides the control and address information for the data bus. Both ports are true bidirectional I/O devices in this mode. Normal operation of these ports is suspended when RPC mode is enabled. The modified port functions are described as follows:

Port 0 : D0-7 This is the 8-bit data bus of the RPC. As a bidirectional I/O bus, it can interface directly to a PC bus or other host.
Port 2.0 : A0 Address input used to determine whether the data bus word is data or command/status.
Port 2.1 : CE If a multiple RPC mode environment is required, this input can be used to select an individual DS5001FP on a common bus.
Port 2.2 :RD Input that allows the host to read data or status from the DBBOUT or STATUS.
Port 2.3 : WR Input that allows the host to write data or commands to DBBIN.
Port 2.4 : OBF Output flag that indicates to a host that the output buffer is full and should be read.
Port 2.5 :IBF Output that indicates to a host that the input buffer is empty.
Port 2.6 : DRQ Output that indicates to a host that a DMA is required.
Port 2.7:DACK Input that indicates to the DS5001FP that the host has granted a DMA.

USE OF THE RPC MODE Figure 8



CS	RD	WR	A0	REGISTER
0	0	1	0	DATA OUT
0	0	1	1	STATUS
0	1	0	0	DATA IN
0	1	0	1	COMMAND IN
1	X	X	X	NO REGISTER

RPC INTERRUPTS

RPC mode provides an additional interrupt to the standard DS5000 set. An Input Buffer Full Interrupt (IBF) will be performed (if enabled) when data is written to the DBBIN from a host. When enabled, this interrupt replaces the Timer 1 interrupt (vector location 1BH). Regardless of whether this interrupt is enabled, future writes are locked out until the DBBIN is read by the DS5001. The DS5001FP provides two outputs to interrupt the host system as needed. These are Output Buffer Full (OBF) and Input Buffer Empty (IBF\).

RPC STATUS REGISTER - RPS (Address 0DAH)

MCON

PA3	PA2	PA1	PA0	RG1	PES	PM	–

RPS

ST7	ST6	ST5	ST4	IA0	F0	IBF	OBF

RPCTL

RNR	–	EXBS	AE	IBI	DMA	RPC	RGO

CRC

RNGE3	RNGE2	RNGE1	RNGE0	–	–	–	CRC

Bit Description:

RPS.7-4: General purpose status bits that can be written by the DS5001FP and can be read by the external host.
Initialization: Cleared when RPCON=0.
Read Access: Can be read by DS5001FP and host CPU when RPC mode is invoked.
Write Access: Can be written by the DS5001FP when RPC mode is invoked.

RPS.3: **IA0**
Stores the value of the external system A0 for the last Input Buffer Write when a valid write occurs (as determined by the IBF flag).
Initialization: Cleared when RPC=0.
Read Access: Can be read by the DS5001FP and host CPU when in RPC mode.
Write Access: Automatically written when a valid Input Buffer Write occurs. Cannot be written otherwise.

RPS.2: **F0**
General purpose flag written by the DS5001FP and read by the external host.
Initialization: Cleared when RPC=0.
Read Access: Can be read by the DS5001FP and host CPU when in RPC mode.
Write Access: Can be written by the DS5001FP when in RPC mode.

RPS.1: **IBF**
Input Buffer Full Flag is set following a write by the external host, and is cleared following a read of the Input Buffer by the DS5001.
Initialization: Cleared when RPC=0.
Read Access: Can be read by the DS5001FP and host CPU when in RPC mode.
Write Access: Written automatically as part of the RPC communication. Cannot be set by the application software.

RPS.0: **OBF**
Output Buffer Full Flag is set following a write of the output buffer by the DS5001, and is cleared following a read of the Output Buffer by the external host.
Initialization: Cleared when RPC=0.
Read Access: Can be read by the DS5001 and host CPU when in RPC mode.
Write Access: Written automatically as part of the RPC communication. Cannot be set by the application software.

RPC PROTOCOL

Data is written to the DS5001FP and is placed in the Input File Buffer. At this time, the IBF flag is set in the RPC Status Register. If enabled by the IBI bit in the RPCTL register, an IBI interrupt will occur. No further updates of the Input Buffer will be allowed until the buffer is read by the DS5001FP. Once read, the IBF flag will be cleared. When the Output Buffer is written to by the DS5001FP, the OBF is set in the RPC Status Register (RPS). No future writes are allowed until the Output Buffer is read by the external host. The OBF is cleared when such a read takes place.

The RPC mode provides a simple interface to a host processor. In general, four control bits specify the operation to be performed. This works as follows:

CS\	A0	RD\	WR\	OPERATION
0	0	0	1	Read DBBOUT
0	1	0	1	Read STATUS
0	0	1	0	Write DBBIN with data
0	1	1	0	Write DBBIN with command
1	X	X	X	Disable RPC bus communication

The above conditions provide the basis of a complete slave interface. The protocol for such communication might operate as follows:

1) Host processor reads STATUS.
2) If DBBIN is empty (IBF=0), host writes a data or command word to DBBIN.
3) If DBBOUT is full (OBF=1), host reads a word from DBBOUT.
4) RPC detects IBF flag via interrupt or polling. Input data or command word is processed.
5) RPC recognizes OBF = 0, and writes a new word to DBBOUT.

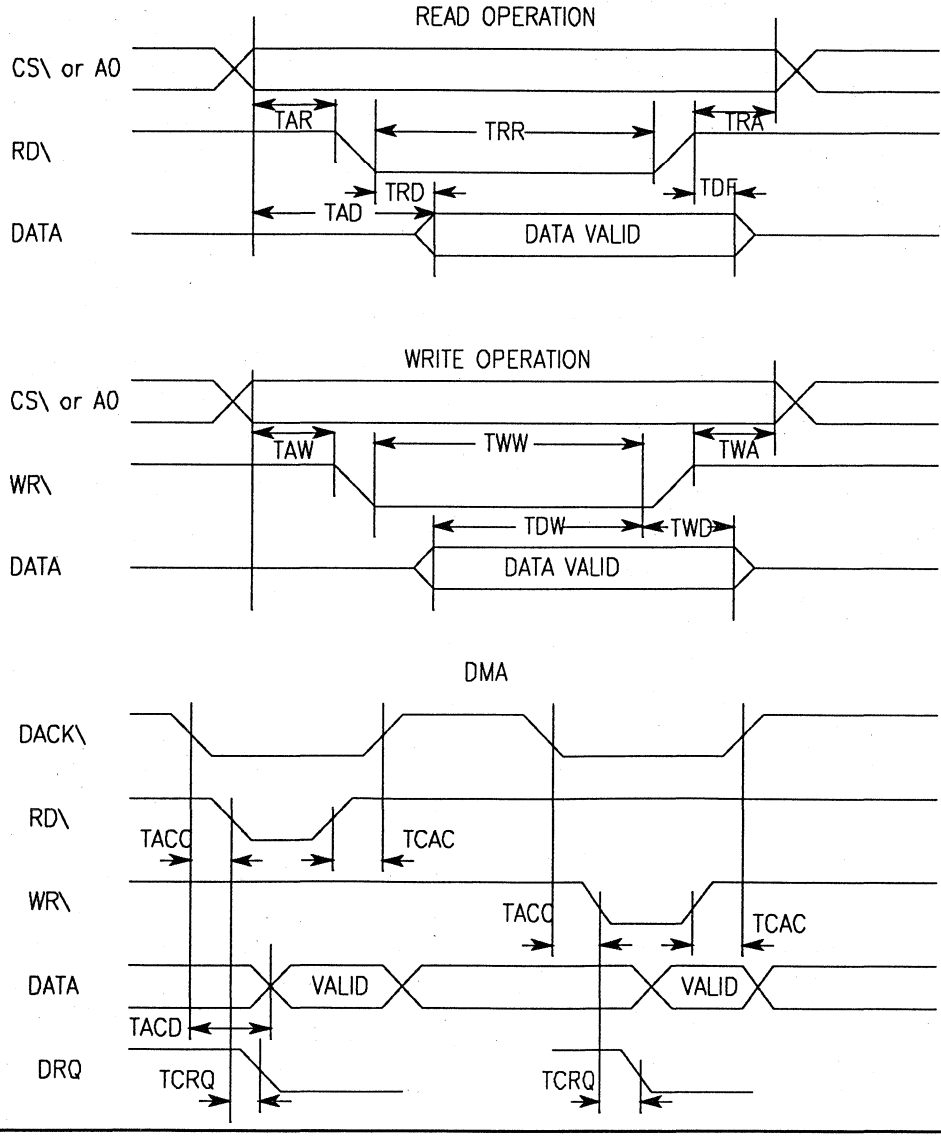
Timing diagrams in Figure 9 illustrate the operation of the RPC mode bus transfers. A DBBOUT read places the contents of DBBOUT on the data bus and clears OBF. A STATUS read places the contents of the STATUS register on the data bus. A write to DBBIN causes the contents of the data bus to be transferred to the DBBIN, and the IBF flag (STATUS) is set. A command write operates in the same way. The DS5001FP can determine whether the write was

data or command by examining the IA0 bit in the STATUS register. This bit will be equal to the A0 input of the most recent host write operation.

DMA OPERATION

If DMA transfers are required, the DS5001FP RPC mode can support them. DMA transfers are initiated by setting the DMA bit in the RPCTL register. The DRQ output is de-asserted at this time. DRQ can be asserted by writing a 1 to the DRQ line (P2.6) from software. The host CPU must respond by pulling the DACK\ input low. Data can then be transferred according to the user's required protocol. DMA mode can be cancelled by clearing the DMA bit, by a DS5001FP reset, or by clearing the RPC to leave RPC mode.

RPC MODE TIMING Figure 9



RPC CONTROL REGISTER - RPCTL (Address 0D8H)

MCON

PA3	PA2	PA1	PA0	RG1	PES	PM	–

RPS

ST7	ST6	ST5	ST4	IA0	F0	IBF	OBF

RPCTL

RNR	–	EXBS	AE	IBI	DMA	RPC	RGO

CRC

RNGE3	RNGE2	RNGE1	RNGE0	–	–	–	CRC

A new register has been added to the special function register space of the DS5001FP. As shown above, the bits have the following functions:

Bit Description:

RPCLT.7 **RNR**
The random number generator of the DS5001FP is available to the user. When a random number is required, the RNR bit signifies that one is available. This bit is cleared when the random number is read, and approximately 160 usec are required to generate the next number.
Initialization: Cleared after all resets.
Read Access: Can be read at any time.
Write Access: Cannot be written.

RPCTL.5 **EXBS**
The Expanded Bus Select routes data memory access (MOVX) to the Expanded bus formed by Ports 0 and 2 when set.
Initialization: Cleared after all resets.
Read Access: Can be read at any time.
Write Access: Can be written at any time.

RPCTL.4 **AE**
Access Enable is used when a software reload is desired without using Program Load mode. When set, the DS5001FP will be temporarily configured in a partitionable configuration with the partition at 4K. This will occur even if the PM=1. When cleared, the prior memory configuration is resumed.
Initialization: Cleared after all resets.

Read Access: Can be read at any time.
Write Access: Can be written at any time, Timed Access protected.

RPCTL.3 **IBI**
When using the RPC mode, an interrupt may be required for the Input Buffer Flag. This interrupt is enabled by setting the Input Buffer Interrupt (IBI) bit. At this time, the timer 1 interrupt is disabled, and this RPC mode interrupt is used in its place (vector location 1BH). This bit can be set only when the RPCON bit is set.
Initialization: Cleared on all resets, and when the RPCON bit is cleared.
Read Access: Can be read at any time.
Write Access: Can be written in RPC mode (when the RPC mode is set).

RPCTL.2 **DMA**
This bit is set to enable DMA transfers when RPC mode is invoked. It can only be set when RPC = 1.
Initialization: Cleared on all resets and when RPC is cleared.
Read Access: Can be read anytime.
Write Access: Can be written when RPCON bit is set.

RPCTL.1 **RPCON**
Enable the 8042 I/O protocol. When set, Port 0 becomes the data bus, and Port 2 becomes the control signals as shown in Figure 8.
Initialization: Cleared on all resets.
Read Access: Can be read at any time.
Write Access: Can be written at any time.

RPCTL.0 **RG0**
This is a Range bit which is used to determine the size of the program memory space. Its usage is shown above.
Initialization: Unaffected by watchdog, external, or power-up resets. Cleared on a No V_{LI} reset.
Read Access: Can be read at any time.
Write Access: Cannot be modified by the application software. Can only be written during Program Load.

CRC-16 SOFTWARE VERIFICATION

The DS5001FP provides optional software verification on power-up using the CRC function. Special purpose hardware provides the CRC a 64K memory space in approximately 400 ms. To support this function, the CRC register shown below is accessible through the Bootstrap Loader. The upper nibble of the CRC register (a hex value between 0 and F) defines the address space in 4K blocks over which the CRC calculation is performed. When the LSB of the CRC register is set, the CRC of the specified block is computed and stored in the last two bytes of the specified area. On power-up, the CRC will be performed and checked against these locations. If an error is detected, the DS5001FP will invoke the Bootstrap Loader and wait. Automatic CRC checking on power-up can be disabled by writing a 0 to the LSB. The CRC register can be written using the W command in program load mode. CRC hardware uses registers 0C3H and 0C2H for most and least significant byte intermediate storage. These registers are accessible for a user-performed CRC calculation.

CRC REGISTER (Address 0C1H)

MCON

PA3	PA2	PA1	PA0	RG1	PES	PM	–

RPS

ST7	ST6	ST5	ST4	IA0	F0	IBF	OBF

RPCTL

RNR	–	EXBS	AE	IBI	DMA	RPC	RG0

CRC

RNGE3	RNGE2	RNGE1	RNGE0	–	–	–	CRC

CRC.7-4: **CRCRANGE 3-0**
Determines the range over which a power-up CRC will be performed. Addresses are specified on 4K boundaries.
Initialization: Reset to 0 on a NoV_{LI} reset.
Read Access: Can be read at any time.
Write Access: Cannot be written by application software. Can be written during program load mode.

CRC.0: **CRC**
When set to 1, a CRC check will be performed on power-up. CRC will be compared to stored values. An error will initiate program load mode.
Initialization: Reset to 0 on a No V_{LI} reset.
Read Access: Can be read at any time.
Write Access: Cannot be written by application software. Can be written during program load mode.

BOOTSTRAP LOADER ENHANCEMENTS

The Bootstrap Loader can be invoked with a single program pin (PROG\) on the DS5001FP. A falling edge on this pin invokes program load mode directly. In the DS5000, program load was invoked by pulling RST high and PSEN\ low. This method also remains available in the DS5001FP. Once bootstrap loading is invoked, the DS5001FP monitors inputs to determine the appropriate type of interface to the host PC. A serial ASCII carriage return received via the serial port will invoke the Serial Bootstrap Loader, which operates in the same manner as the DS5000. Bootstrap loading is exited by asserting a rising edge on PROG\ or issuing an 'E' command to the loader. If program load mode was entered using RST and PSEN\, then the Bootstrap Loader will be exited when this condition is removed.

SERIAL BOOTSTRAP LOADER COMMANDS Table 3

COMMAND	FUNCTION
C	Return CRC-16 of the nonvolatile program/data RAM
D	Dump Intel Hex file
F	Fill nonvolatile program/data RAM block with constant
L	Load Intel Hex file
R	Read Status of SFRs (MCON, 5001, PCON, CRC)
T	Trace (echo) incoming Intel hex data
U	Clear Security Lock
V	Verify nonvolatile program/data RAM with incoming Intel Hex data
W	Write Special Function Register (MCON, 5001, PCON, CRC)
Z	Set Security Lock
N	Set Freshness Seal - All program and data will be lost
E	Exit Program Load mode and return to application software control

A new RPC Bootstrap Loader allows a system host such as an 8088 to initiate program loading using the 8042 RPC interface. In this way, the host system can determine a need to update software, then use a standard operating interface to load the application software. No additional hardware is required. The RPC mode is used to load files from a master CPU. A program for peripheral control could be loaded from a floppy or hard disk at boot-up. Software updates can be easily downloaded via diskettes, EPROM, or even over the phone lines using a modem.

RANDOM NUMBER GENERATOR

A true random number generator is incorporated into the DS5001FP. The random byte is based on a true random number generator circuit that uses the asynchronous frequency differences of an internal ring oscillator and the processor master clock (determined by XTAL1 and XTAL2). When a random number is required, the RNR bit must be checked. When a random number is available, this bit will be set. The random byte can be read from a register at location 0CFH. After a byte is read, approximately 160 usec is required to generate another. The RNR will be 0 until this time.

SPECIAL FUNCTION REGISTER MAP

The DS5001FP has several special function registers added or modified. The following table lists the registers and locations. All other registers remain the same as in the DS5000.

NEW OR MODIFIED SPECIAL FUNCTION REGISTERS Table 4

LABEL	ADDRESS	FUNCTION
STAT	DAH	RPC STATUS
5001	D8H	MEMORY AND CONTROL FUNCTIONS
RNR	CFH	RANDOM NUMBER BYTE
MCON	C6H	MODIFIED MCON REGISTER
DBBIN	80H	RPC DATA IN
DBBOUT	80H	RPC DATA OUT
CRC	C1H	CRC FUNCTION CONTROL
CRCLOW	C2H	CRC LEAST SIGNIFICANT BYTE
CRCHIGH	C3H	CRC MOST SIGNIFICANT BYTE

POWER SUPPLY MONITORING

The DS5001FP incorporates a bandgap voltage reference that allows improved accuracy for power shutdown. In addition, two pins are available that allow the control of external power switching circuits. The VRST\ pin indicates that the power is below the reset threshold, and that consequently the DS5001FP has started orderly power down (Power Down Reset). The PF\ indicates that the power has fallen below the battery voltage and that the DS5001FP has switched to lithium backup for data retention. These pins can be used in conjunction with a power switch such as the DS1336 Afterburner Chip for larger current applications that require battery backup. The VRST\ pin is effectively an active low, bidirectional reset signal. If multiple DS5001FPs are used in a system, this signal can be connected to all devices. In this way, the first DS5001FP that goes into Power Down Reset will pull this signal low, causing the remaining units to enter Power Down Reset. This assures that an operating device is not attempting communication with one that is in Power Down Reset.

FRESHNESS SEAL

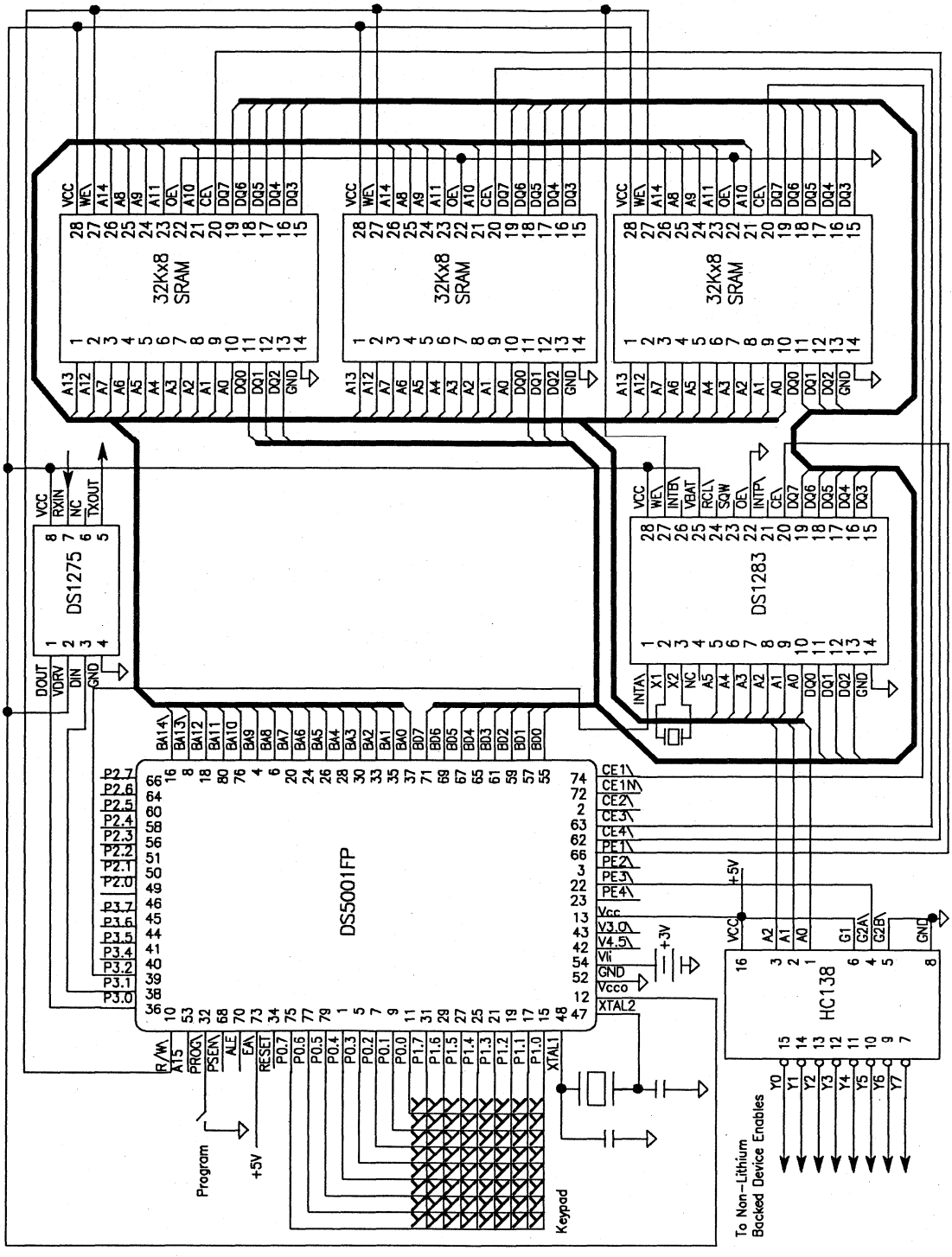
In certain applications, it is desirable to test an end system, then store it for later programming. Lithium capacity can be preserved in this situation by invoking a freshness seal using the 'N' command from the Bootstrap Loader. When this command is issued, the lithium backup will be removed from electrical connection. Upon the subsequent removal of V_{CC} following this operation, data retention will be disabled until the next system power-up. This preserves the lithium cell lifetime while a system is stored.

APPLICATIONS

Figure 10 illustrates a typical application of the DS5001FP. The schematic represents the core of a low-power instrument with nonvolatile program and data memory, as well as time-of-day monitoring. A clock\calendar alarm is provided to notify the DS5001FP that a particular time has occurred. This schematic illustrates a flexible memory architecture by providing 32K of program and 64K of data memory. RAM contents and time of day are preserved in the absence of V_{CC} for over 10 years by the DS5001's crashproof circuitry and backup lithium cell.

The memory architecture and bytewide bus allow most core functions to be memory-mapped, freeing up the ports for other I/O functions. Nonvolatile resources as well as ordinary volatile peripherals can be attached to the bytewide bus. In this example, program and data memory, timekeeping, and other volatile peripherals are memory-mapped. Port pins are used for RS232 communication, an RTC alarm interrupt, and a 64-button keypad. As shown, 13 port pins are still available for alternate uses such as an LCD display.

TYPICAL APPLICATION SCHEMATIC Figure 10



DS5001FP ENHANCEMENTS SUMMARY

As shown above, the MCON register on the DS5001FP has been modified from its original function on the DS5000FP. These modifications allow increased flexibility in the type and number of memories used on the bytewide bus. The old PAA bit (MCON.1) has been replaced by the new Partition Mode bit (PM) which determines how the PA3-0 bits map program and data memory. If PM=0, then the PA3-0 select partition addresses that are in 4K x 8 steps; if PM=1, then partitioning of a single memory device is prohibited. Instead, the Range determines the size of program and data memory used on the bytewide bus: 32K or 64K bytes. When PM=1, nonvolatile data memory occupies a separate memory map from the nonvolatile program memory. Thus, nonvolatile data memory begins at 0000H (except for the 128K x 8 RAM), as opposed to beginning at the partition address when PM=0. Note that the partition bits PA3-0 are timed access protected in the DS5001, as opposed to the PAA bit in the DS5000.

DS5001FP	DS5000FP
- 128K Memory Range	64K total memory, 32K restricted to data only
- 64K partitionable memory	32K partitionable memory
- Peripheral Enables	No extra chip enables, embedded bus consumed completely
- RPC mode	NA
- Bandgap Reference	Battery reference (fluctuates)
- EXBS Expanded Bus	Expanded bus access outside of embedded memory area only
- Serial or RPC Bootstrap loading	Serial Bootstrap loading
- Random number generator	NA
- Automatic CRC on power-up	CRC via Bootstrap Loader only
- Power monitor signals	NA

ORDERING INFORMATION

The following versions of the DS5001FP are available as standard products from Dallas Semiconductor:

PART #	CLOCK	PACKAGE
DS5001FP -08	8 MHz	80-pin QFP
DS5001FP -12	12 MHz	80-pin QFP
DS5001FP -16	16 MHz	80-pin QFP

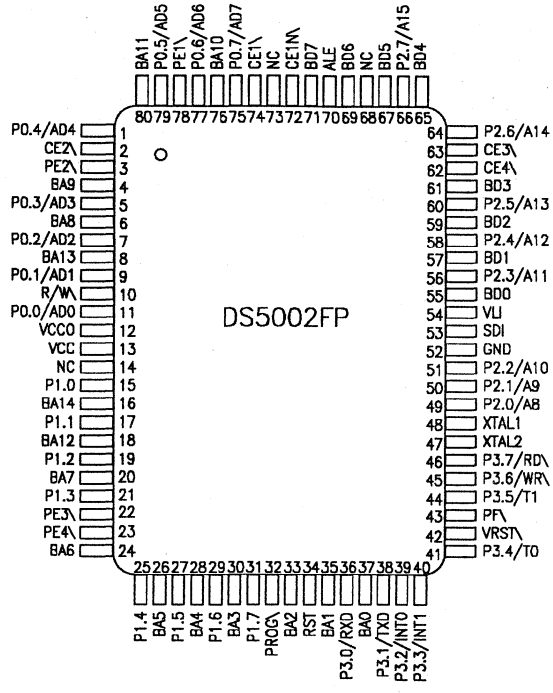
DALLAS SEMICONDUCTOR

DS5002FP
Secure Micro Chip

FEATURES

- Enhanced security features:
  - Stronger address/data encryptor
  - 64-bit encryption key word
  - Automatic true random key generation
  - SDI (Self-Destruct Input)
  - Top coating defeats microprobe attack
- Customer-specific encryption versions available
- Incorporates enhanced memory and I/O features of DS5001FP 128K Micro Chip.
- 100% compatible with 8051 instruction set
- 80-pin Quad Flat Pack (QFP) surface-mount package

PACKAGE OUTLINE



DESCRIPTION

The DS5002FP Secure Micro Chip is a secure version of the DS5001FP 128K Micro Chip. In addition to the memory and I/O enhancements of the DS5001FP, the Secure Micro Chip incorporates the most sophisticated security features available in any microcontroller. The security features of the DS5002FP include an array of mechanisms which are designed to resist all levels of threat, including observation, analysis, and physical attack. As a result, a massive effort would be required to obtain any information about memory contents. Furthermore, the soft nature of the DS5002FP allows frequent modification of the secure information, thereby minimizing the value of any secure information obtained at any given time by such a massive effort.

The DS5002FP implements a security system that is an improved version of its predecessor, the DS5000 Soft Microcontroller. Like the DS5000, the DS5002FP loads and executes application software in encrypted form in up to 128K x 8 bytes of standard SRAM on its byte-wide bus. This RAM is converted by the DS5002FP into lithium-backed nonvolatile storage for programs and data. As a result, the contents of the RAM and the execution of the

software appear unintelligible to the outside observer. The encryption algorithm uses an internally stored and protected key. Any attempt to discover the key value results in its erasure, rendering the encrypted contents of the RAM useless.

The Secure Micro Chip offers a number of major enhancements to the software security implemented in the previous generation of the DS5000 Soft Microcontroller. First, the DS5002FP provides a stronger software encryption algorithm which incorporates elements of DES encryption. Second, the encryption is based on a 64-bit key word, as compared to the DS5000's 40-bit key. Third, the key can only be loaded from an on-chip true random number generator. As a result, the true key value is never known by the user. Fourth, a Self-Destruct Input pin (SDI) is provided to interface to external tamper detection circuitry. With or without the presence of V_{CC}, activation of the SDI pin has the same effect as resetting the security lock: immediate erasure of the key word and the 48-byte vector RAM area. Fifth, a special top-coating of the die prevents access of information using microprobing techniques. Finally, customer-specific versions of the DS5002FP are available that incorporate a one-of-a-kind encryption algorithm.

When implemented as a part of a secure system design, the DS5002FP can typically provide a level of security which requires more time and resources to defeat than it is worth to unauthorized individuals who have reason to try.

FOR FURTHER INFORMATION

A complete data sheet for the DS5002FP is available on request to customers who have a signed non-disclosure agreement on file with Dallas Semiconductor.

ORDERING INFORMATION

The following versions of the DS5002FP are available as standard products from Dallas Semiconductor.

PART #	CLOCK	PACKAGE
DS5002FP -08	8 MHz	80-pin QFP
DS5002FP -12	12 MHz	80-pin QFP
DS5002FP -16	16 MHz	80-pin QFP

Please contact Dallas Semiconductor for ordering information on customer-specific versions of the DS5002FP.

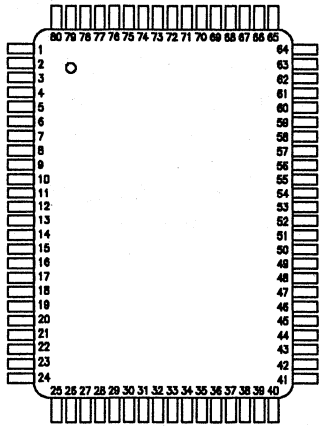
DALLAS SEMICONDUCTOR

DS53xx
Micro Softener Chips

FEATURES

- Chips provide softness for microprocessor or microcontroller-based systems
- Adapts to task-at-hand:
  - -Converts CMOS SRAM into lithium-backed NV program/data storage
  - -Freshness seal ensures maximum lithium life
  - -Serial bootstrap loading of software
  - -Code can be changed in end use
- Crashproof operation:
  - -NV storage for 10 years with no V_{CC}
  - -Orderly shutdown/ restart on power-up/down
  - -Inadvertent write protection
  - -Restart on errant software execution
- Provides enhanced 8-bit parallel I/O ports:
  - -One port generates 8 separate edge- or level-triggered interrupts
  - -Two ports support Dual Port Register file interface for PC-bus applications
- Processor-specific versions
  - -DS5340FP: Compatible with NEC V40; allows code development in PC native instruction set
  - -DS5303FP: Compatible with Hitachi HD6301/HD6303 Family
- FUTURE PRODUCTS:
  - DS5396FP: Compatible with Intel 80C196 Family
  - DS5311FP: Compatible with Motorola 68HC11 Family

PIN DESCRIPTION



80-Pin Quad Flat Pack

DESCRIPTION

The DS53xx Micro Softener Chips provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities for systems based on a variety of processor architectures.

Each version of the Micro Softener interfaces directly to a specific processor's address/data bus and control signals and can typically convert as much CMOS SRAM as can be addressed within the processor's memory map into lithium-backed nonvolatile read/write storage. This storage is initially bootstrap loaded via the serial port and can be changed at any time without the removal of components from the end system. In addition, the storage can be dynamically partitioned into separate program and data areas so that the program area is write-protected. Through proper selection of a lithium cell, the contents of the RAM can easily retain data in the absence of external power for over ten years.

The Micro Softener Chips provide crashproof operation when system power is momentarily disrupted or removed entirely. Early warning of a potential power failure is signalled by the Micro Softener so that the operational state of the system can be stored prior to a complete removal of system V_{CC}. The contents of the external nonvolatile SRAM and Micro Softener's configuration registers are automatically sustained at low current from an external lithium energy source for the entire time that V_{CC} is removed. When V_{CC} is applied once again, the Micro Softener automatically restarts the processor without the need for external circuitry. Regardless of whether the power merely fluctuates or is absent for years, upon its return the processor will have the ability to resume execution as if the power failure had not occurred at all.

Crashproof operation is provided in electrically noisy operating environments. A watchdog timer restores controlled software execution following a disruption in normal program execution, as might be caused by a transient condition. In addition, a timed access feature ensures controlled access to critical bits in the Micro Softener's configuration registers as well as to the write-protected portion of the nonvolatile SRAM.

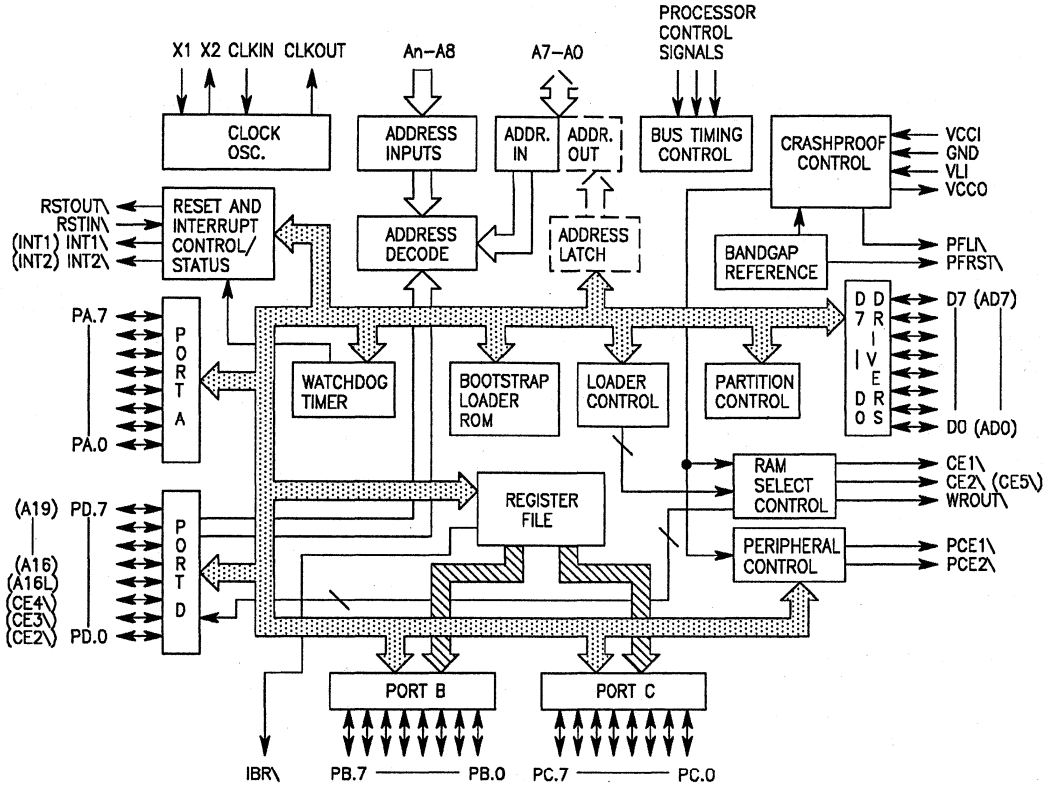
Depending on the specific version of the Micro Softener, up to four parallel I/O ports are provided which offer extended I/O capabilities. All versions incorporate one port which allows each pin to serve as an edge-triggered or level-sensitive interrupt input. In addition, all versions offer two ports that can be configured as an interface to the internal dual port register file. This software-invoked feature converts these two ports into a high-speed parallel bus interface to a host microprocessor. As a result, the Micro Softener-based system can act as an intelligent peripheral controller in a host system, such as a PC.

Finally, the Micro Softener allows interface to external peripheral devices with little or no external glue logic.

GENERIC FEATURES

Features which are generic to the entire family of Micro Softeners are described below. Detailed information for specific versions of Micro Softeners are given in individual device data sheets. Figure 1 is an internal block diagram of the generic Micro Softener.

GENERIC MICRO SOFTENER BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

V_{CCI}, GND - Power Supply Inputs
V_{CCI} is the +5V power supply voltage input; GND is tied to system ground.
V_{LI} - Lithium Supply Input
V_{LI} is tied to an external +3V lithium energy cell.
V_{CCO} - Power Supply Output
V_{CCO} is the power supply output used to power external nonvolatile CMOS SRAM and peripheral devices.
An-A8 - Address Bus Inputs
An-A8 are tied to the corresponding address output pins from the system processor.
D7-D0 - Data Bus; Bidirectional
(AD7-AD0) - Multiplexed Address/Data Bus; Bidirectional
These pins are used to interface to the system data bus. Processor-specific versions of the Micro Softener interface to either non-multiplexed data busses or multiplexed address/data busses.
A7-A0 - Address Bus Inputs (Address Bus Outputs)
For non-multiplexed data bus versions, A7-A0 are used to interface to the corresponding address output pins from the system processor. For multiplexed address/data bus systems, these pins output the demultiplexed lower 8 bits of address which are latched from the multiplexed address/ data bus pins.
Processor Control Signals
Each processor-specific version of the Micro Softener provides a set of control inputs that connect directly to the processor's bus control signals. These pins signal read or write operations on the system bus to the Micro Softener.
CE1-2\ (CE3-5\); Chip Enable Outputs
One or more of these pins are typically tied to bytewide CMOS SRAMs that are maintained as nonvolatile program/data storage by the DS53xx. Each chip enable signal is assigned to a block of the processor's memory map during serial bootstrap loading of the system. One of these pins will be driven low when a memory cycle is decoded by the DS53xx as an access to a location within one of these blocks. These pins are held in their inactive high state by lithium backup in the absence of V_{CC}.
PCE1\, PCE2\ - Peripheral Chip Enable Outputs
PCE1\ and PCE2\ are software-selectable chip enable outputs to peripheral devices interfaced to the system address/data bus. A Peripheral Enable output pin will be driven low when the processor performs a read or write cycle to an address within the range assigned to that pin.
WROUT\ - Write Output
WROUT\ is driven low when a processor write cycle is being performed under the direction of the DS53xx.
X1, X2 - Crystal Inputs
X1 and X2 are used to tie a crystal to the internal clock oscillator circuit and set the operating frequency of the system. X1 is the input to the inverting oscillator amplifier and X2 is the output.
CLKOUT - Clock Output
CLKOUT is used to output a TTL/CMOS-compatible clock output from the internal oscillator circuitry within the DS53XX. Normally, this signal is used to clock the system processor and can be tied to other peripheral devices.

CLKIN - Clock Input
CLKIN is intended to be tied to the processor's CMOS-compatible clock output. The circuitry within the Micro Softener monitors this signal as an indication of activity within the processor for detection of low power standby operating modes and/or for synchronization purposes.
RSTOUT\ - Output; Active Low
The RSTOUT\ pin is provided to place the system processor in a reset condition in response to one of several conditions: When a power-on condition has occurred, when a power-off condition is about to occur, when a watchdog time-out has occurred, or when a reload condition is invoked.
RSTIN\ - Input; active low
This pin is used to monitor a system reset line. The Micro Softener's RSTOUT\ is driven to its active level in response to an active level applied on RSTIN\.
INT1\, INT2\ (INT1, INT2) - Interrupt Outputs; Active Low
INT1\ and INT2\ are used to signal the system processor of pending interrupt conditions within the Micro Softener.
PFRST\ - Power Fail Reset; Output, Active Low
PFRST\ indicates that V_{CC} voltage has dropped below the processor's minimum operating threshold, and for that reason the processor is being held in a reset state by the Micro Softener.
PFLI\ - Power Fail Lithium; Output, Active Low
PFLI\ is used to indicate that V_{CC} voltage has dropped below the lithium cell's voltage (nominally 3.0V) and that the Micro Softener's configuration registers, the external NV SRAM, and any peripheral circuit (such as a DS1283 Watchdog Timekeeper Chip) controlled by the lithium-backed PCE1\ pin are being supplied from the lithium cell tied to V_{LI}.
IBR\ - Input Buffer Ready; Output, Active Low
When the dual port register file interface has been enabled in place of Ports B and C, the Input Buffer Ready signal is used to indicate to the host processor that the selected input buffer registers are ready to accept data from the host processor.
PA7-PA0 - Port A; Bidirectional I/O
PA7-PA0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port A. These pins can also be individually programmed as edge- or level-sensitive interrupt inputs.
PB7-PB0 - Port B; Bidirectional I/O
PB7-PB0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port B. This port can also be programmed to provide address, control, and status signals for the internal Dual Port Register File in conjunction with Port C.
PC7-PC0 - Port C; Bidirectional I/O
PC7-PC0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port C. This port may also be programmed to provide a bidirectional data bus interface for the internal Dual Port Register File in conjunction with Port B.
PD7-PD0 - Port D; Bidirectional I/O
PD7-PD0 are the interface pins to the multiple-mode bidirectional I/O port designated as Port D. On some versions of the Micro Softener, Port D is replaced with higher order address inputs and additional chip enable outputs.

ARCHITECTURAL DESCRIPTION

The following is a generic description of the internal architecture for the Micro Softener family. Figure 1 should be used for reference.

ADDRESS DECODE

During execution of processor read and write cycles, the Micro Softener accepts and decodes all of the incoming address lines from the system processor. For most designs, the Micro Softener defines the entire memory map for the system. It controls the selection of the external NV SRAM, on-chip registers, and external peripheral devices.

Each processor-specific version of the Micro Softener provides programmable chip enable outputs for control of external bytewide CMOS SRAM. Sufficient control is provided so that the majority of the processor's address space can be populated with NV SRAM under the control of the Micro Softener. The chip enable outputs are configured during serial bootstrap loading to decode blocks of memory corresponding to the density of the bytewide memory chips and/or SIMMs in the system. Depending on the processor-specific version, some combination of 8K x 8, 32K x 8, 128K x 8, or 512K x 8 blocks are decoded.

Address partition control bits within the Micro Softener allow the distinct program and data areas to be defined in the NV SRAM. The areas designated for program code cannot be overwritten via a normal processor write cycle. A multiple instruction Timed Access write sequence must be performed within a specified time window in order to modify the partition bits so that program code can be modified by the application software. The program code is thereby protected from inadvertent write operations in the event of errant software execution.

Locations in the external NV SRAM that are not accessible include those locations that are occupied by the internal registers of the processor and of the Micro Softener.

Two peripheral enable signals (PCE1\ and PCE2\) are provided to interface to chip enable inputs on peripheral devices. Each signal can be individually enabled or disabled by software during system operation. When it is enabled, the peripheral enable signal will pulse active low during a read or write cycle within a specified 256-byte block of memory. When disabled, locations within the external NV SRAM can be accessed instead of the peripheral device.

PCE1\ is designed to be a chip enable control signal for a peripheral device that is sustained from the lithium cell in the absence of V_{CC}. As a result, it remains at a logic high (inactive) level when system V_{CC} is removed. A common application for this feature would be to control the Dallas DS1283 Watchdog Timekeeper Chip, which can be permanently powered from the Micro Softener's V_{CCO} output. PCE2\ collapses to ground in the absence of V_{CC}.

LOW POWER STANDBY

The Micro Softener responds to software-initiated low-power standby modes in which the internal processor clock is halted. In some microprocessors, this is referred to as the Stop mode. In Stop mode, the processor draws a reduced amount of current from its V_{CC} line in order to retain the contents of its on-chip registers and/or RAM and thereby retain its operating state. The Micro Softener is capable of sensing such a mode of operation by the absence of a clock output signal from the processor on its CLKIN pin. In this event, the Micro Softener will disable the clock output (CLKOUT) from the processor and place itself in a low-power standby condition until a reset is issued, which is intended to resume processor operation. When such a signal is detected, the Micro Softener will once again supply a clock signal to the processor and will issue a reset signal to it.

CRASHPROOF OPERATION

The crashproof feature provided by the Micro Softener gives the embedded control system the ability to retain all information in the complete absence of V_{CC}. The on-chip nonvolatile control circuitry monitors the V_{CCI} line for three thresholds below nominal operating voltage (Figure 2). When the voltage drops below the Power Fail Warning threshold (V_{PFW}), an interrupt will be generated via the Micro Softener's INT1\ pin to signal the processor of an impending power fail condition. This is to allow time for a service routine to save the operational state of the microcontroller prior to V_{CC} dropping below the V_{CCMIN} threshold. When this occurs, processor operation is automatically terminated by the Micro Softener issuing a reset to the processor via the RSTOUT\ pin, followed by the disabling of clock pulses to the processor via the Micro Softener's CLKOUT pin. Finally, once V_{CC} voltage drops below the lithium cell voltage threshold (V_{LI}), power from the embedded lithium cell is applied to place the device in its Data Retention mode.

When V_{CC} voltage is again applied to the system, an internal Power On Reset cycle is executed without the need for any external components on the Micro Softener's RSTIN\ pin. In addition, status information is available to distinguish the Power On Reset from the watchdog timer and external resets.

The Micro Softener's tolerance of power cycling provides an alternative for battery-powered, hand-held systems to the conventional low-power standby modes described earlier. The crashproof feature actually implements a zero-power standby mode which is superior to the Stop mode in that the entire state of the system is retained in nonvolatile RAM with no current drawn whatsoever from the system's operating power source.

WATCHDOG TIMER

As part of the crashproof feature of the Micro Softener, the on-chip watchdog timer is a method of restoring proper operation in the event that controlled execution of the software is lost.

When the watchdog timer is enabled, it will eventually reach a time out condition after a programmable number of clock cycles unless it is reset by the application software. An internal reset to the CPU will be generated if the time out condition is ever reached. Application software that utilizes the watchdog timer should therefore be written to periodically reset it so that the time-out condition will never be reached during normal operation.

The watchdog time-out period is programmable during initial loading of the application software via the serial bootstrap loader. The time-out period is programmed in terms of a number of crystal clock oscillator periods (t_{OSC}) of the Micro Softener. One of the following seven time out intervals can be selected: 2^{14}, 2^{15}, 2^{16}, 2^{17}, 2^{18}, 2^{19}, 2^{20}, or 2^{21} t_{OSC} periods.

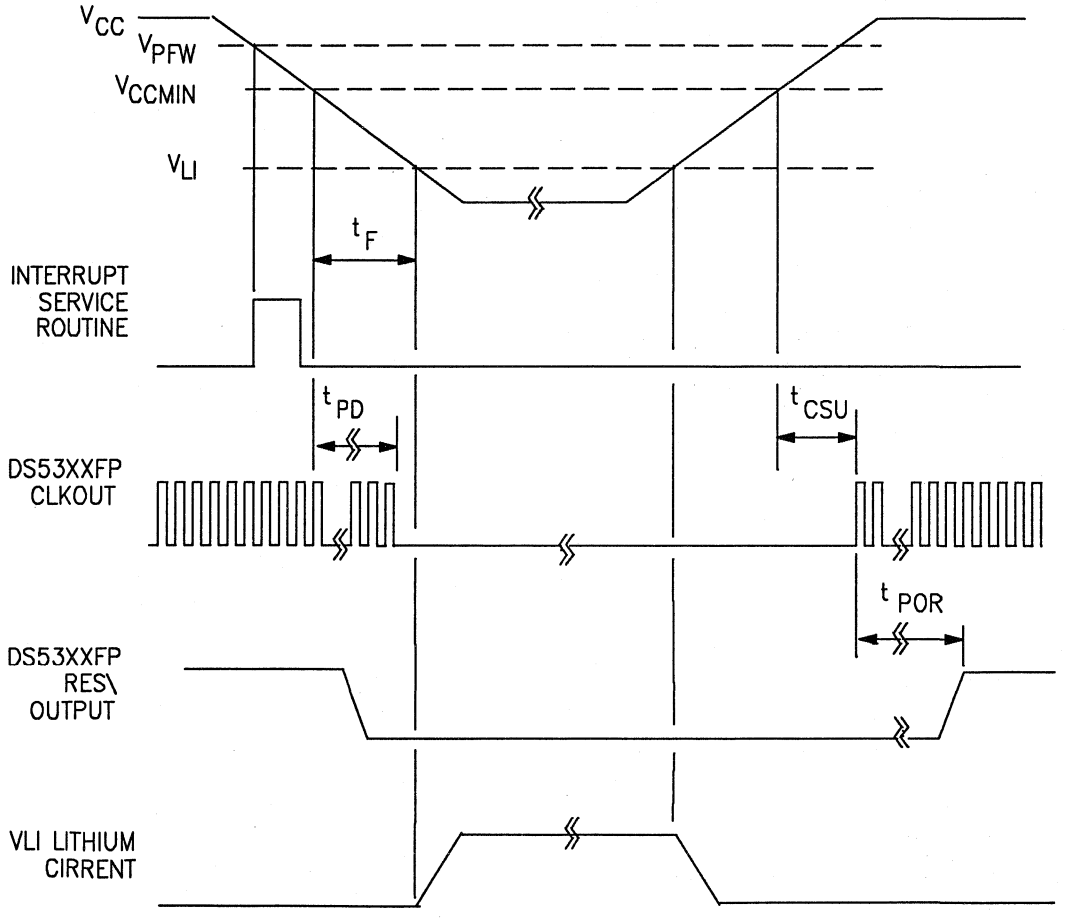
PARALLEL I/O PORTS

Depending on the version of the Micro Softener, there is a total of either three or four 8-bit bidirectional I/O ports. The ports are designated as A, B, C, and D. Ports A, B, and C are available on all versions. Port D is available on those versions which interface to a processor with a maximum of 16 address lines.

Each bit of the four ports can be software selected to operate as a true bidirectional or pseudo bidirectional port bit. In addition, each port gives the user the ability to read either the port pin state or the output latch state on an independent basis.

Port A has an additional feature: each of its bits can serve as an individually-maskable interrupt

CRASHPROOF OPERATION TIMING Figure 2



input. Furthermore, each of these bits can be programmed to be level-sensitive or edge-sensitive. Each bit can also be programmed to interrupt on positive or negative signals. The processor is signalled by the DS53xx that such an interrupt has occurred via one of the processor's external interrupt lines. A register is provided within the Micro Softener which can then be polled by the processor to determine the source of the interrupt.

DUAL PORT REGISTER FILE

Ports B and C can also be software selected to serve an alternate function as an interface to an internal Dual Port Register File on the DS53xx. The Dual Port Register File interface allows the Micro Softener-based system to serve as a user-defined peripheral controller in a multiprocessor system. The host microprocessor can communicate over its data bus at high speed with the Micro Softener-based subsystem via the register file. In effect, the subsystem functions as a very sophisticated, user-reprogrammable peripheral device. The register file manages the transfer of data independent of the processor.

The register file function can be enabled or disabled from the application software. When it is enabled, the pins of Ports B and C are automatically redirected to serve the alternate functions as shown in Figure 3.

Within the Micro Softener, the register file consists of 8 input buffer registers, 8 output buffer registers, and a status register and interrupt control capability for both the host microprocessor and the subsystem's processor.

SERIAL BOOTSTRAP LOADER

The serial bootstrap loader is a firmware package contained within a special ROM area on the Micro Softener. It can be invoked either by external activation of the Reload pin, by the application software, or by detection of an error in the NV SRAM following a power-on or watchdog timer reset. When it is invoked, the processor is first internally reset and then executes code contained within the ROM. The firmware responds to commands from a host PC via the processor's asynchronous serial I/O port.

Initial loading of the application software and setting of the configuration registers within the Micro Softener is performed via the serial bootstrap loader. Once this information is loaded, it is sustained as nonvolatile information by the Micro Softener under power supplied by the lithium cell.

A variety of crystal frequencies and resulting baud rates are supported across a three-wire interface from the processor's serial I/O port.

When initialization is complete, the ROM is no longer present in the memory map of the processor, and the application software can be executed. The ROM is therefore transparent to the execution of application software.

The bootstrap serial loader implements an easy-to-use command line interface which facilitates communication from a PC. Functions that can be performed via the serial bootstrap loader include:

-Initialize memory range
-Load/dump application program into/from NV SRAM (absolute hex format)
- Verify application program in NV SRAM
- Fill memory range in NV SRAM
- Calculate, report, and store CRC value for requested NV SRAM range
-Initialize program/data partition
-Initialize freshness seal
-Select watchdog time-out value

DATA RETENTION AND FRESHNESS SEAL

Through proper memory and lithium selection, 10 years of data retention at room temperature can be achieved in the absence of V_{CC}. The Micro Softener draws no current from the lithium cell when V_{CC} is applied. Therefore, the 10 year figure is a cumulative amount of time for which lithium backup is required. Some capacity will be lost due to age of the lithium cell. However, lithium cells have an extremely long shelf-life when they are not supplying current, typically on the order of 30 to 40 years. As a result, such shelf-life considerations typically do not affect the data retention time for a given application.

The Micro Softener also incorporates a freshness seal feature that allows data retention to be disabled in the absence of V_{CC}. This feature is provided so that the lithium capacity can be preserved during times when the system is in storage and no data retention is required. The freshness seal is enabled during serial bootstrap loading by a special command. Upon the subsequent removal of V_{CC} following this operation, data retention will be disabled until the next time the system is powered up. After that time, data retention will again be enabled.

DEVICE DATA SHEETS

The user should consult the individual device data sheets for detailed information on a particular processor-specific version of the Micro Softener. Product previews are currently printed in the 1990-91 Dallas Semiconductor data book for the following versions:

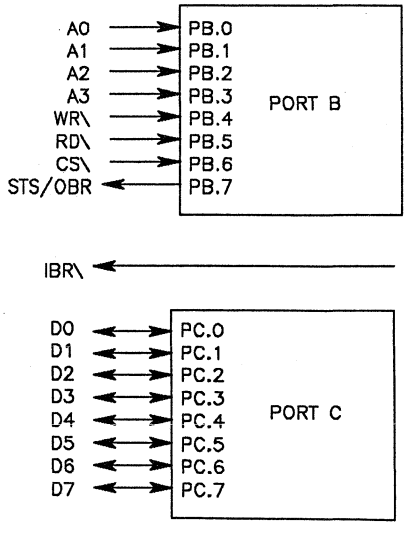
DS5340 V40 Softener Chip
DS5303 6303 Softener Chip

In addition, product previews are printed in this data book for small, single-board soft Stik microcontroller systems based on these Micro Softeners:

DS2340 Soft V40 Flip Stik
DS2301 Soft 6301 Stik

Complete specifications on these products as well as information on future Micro Softener products is available on request from Dallas Semiconductor.

DUAL PORT REGISTER FILE PIN FUNCTIONS Figure 3



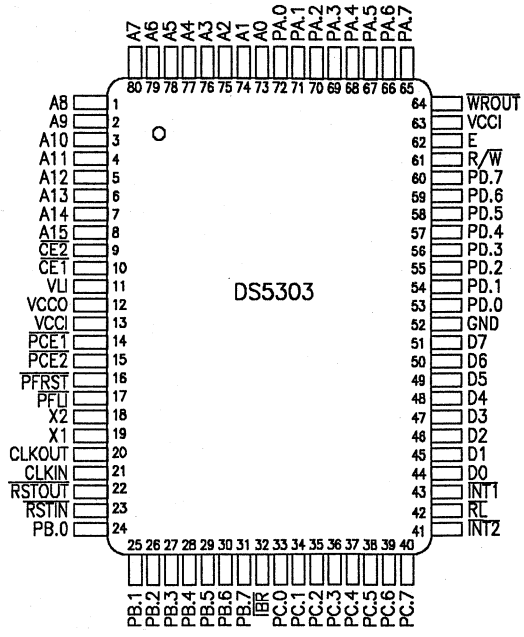
DALLAS SEMICONDUCTOR

DS5303
6303 Softener Chip

FEATURES

- Provides softness for HD6303-based systems:
- Adapts to task-at-hand:
  - Converts up to 64K bytes of CMOS
  - SRAM into lithium-backed NV program/data storage
  - Serial bootstrap loading of software
  - Code can be changed in end use
- Crashproof operation during transient power conditions
- Provides 4 enhanced 8-bit parallel I/O ports

PACKAGE OUTLINE



80-Pin Quad Flat Pack

DESCRIPTION

The DS5303 6303 Softener is a member of the Micro Softener family that is designed to provide the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities, as discussed in the DS53xx Micro Softener Chips data sheet, for systems based on the popular Hitachi HD6303 microprocessor. The DS5303 interfaces directly to HD6303's address/data bus and control signals, and converts up to 64K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the HD6303, DS5303 Softener Chip, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered DS1283 Watchdog TimeKeeper Chip, can be added to the system without the need for additional glue logic.

Also available from Dallas Semiconductor is the DS2301V and DS2301Y Soft 6301 Stiks, which are complete implementations of the embedded control system described above. These Stiks are implemented as small daughter-boards that plug into the industry-standard 40- or 68-pin SIMM connector scheme which supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2301V and DS2301Y can be used as high-level building blocks in a system design, resulting in a quick time to market for a Softener-based HD6303 system. Alternatively, they can be used for fast prototyping of a system that will ultimately incorporate the DS5303 6303 Softener Chip itself. Consult the DS2301V/DS2301Y data sheet for information on this application of the DS5303.

PIN DESCRIPTION

The table shown below summarizes the pins of the DS5303 by function type.

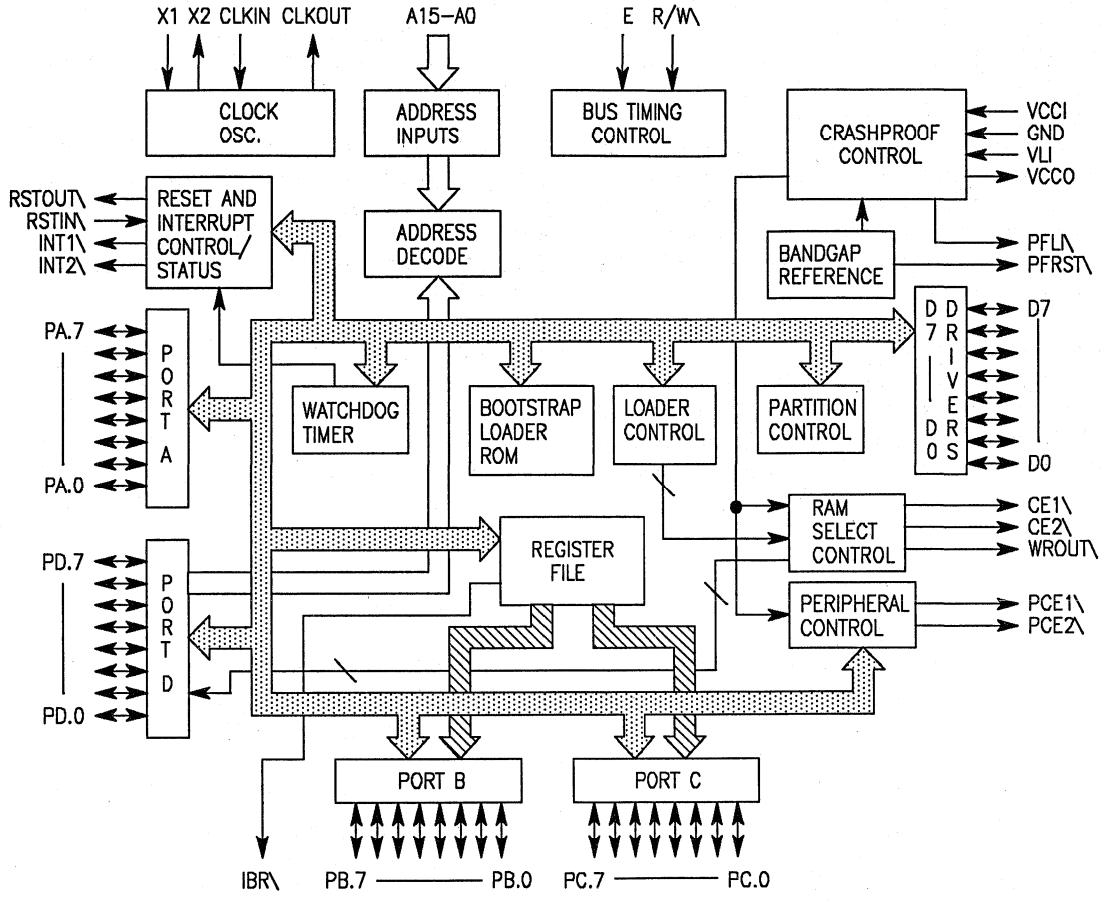
TABLE 1: DS5303 PIN DESCRIPTION (\ Denotes Condition Low)

NAME	DESCRIPTION
V_{CCI}	+5V Power Supply Input
GND	Ground
V_{LI}	+3V Lithium Supply Input
V_{CCO}	Lithium-Backed Power Supply Output
PFRST\	Power Fail Reset Threshold Output
PFLI\	Power Fail Lithium Threshold Output
X1	Crystal Oscillator Input
X2	Crystal Oscillator Output
RL\	Reload Input
CLKIN	Clock Input from HD6303
CLKOUT	Clock Output to HD6303
A15-A0	Address Bus Inputs from HD6303
D7-D0	Data Bus to/from HD6303; bidirectional
E	Enable Output from HD6303
R/W\	Read/Write Input from HD6303
CE1\, CE2\	Chip Enable Outputs to RAM
PCE1\-PCE2\	Peripheral Chip Enable Outputs
WROUT\	Write Output
RSTIN\	Reset Input
RSTOUT\	Reset Output to HD6303
INT1\	Interrupt Output 1 to HD6303
INT2\	Interrupt Output 2 to HD6303
PA7-PA0	Port A; Bidirectional
PB7-PB0	Port B; Bidirectional
PC7-PC0	Port C; Bidirectional
PD7-PD0	Port D; Bidirectional
IBR\	Input Buffer Ready Status Output

BLOCK DIAGRAM

A conceptual block diagram of the DS5303 is illustrated in Figure 1. Consult the DS53xx Micro Softener Chips data sheet for complete operational details that are common to all of the versions of the Micro Softener. Features unique to the DS5303 are described on the following pages.

FIGURE 1: DS5303 MICRO SOFTENER BLOCK DIAGRAM



ADDRESS/DATA BUS CONTROL

The DS5303 interfaces directly to the Hitachi HD6303's non-multiplexed address and data busses. All 16 address lines as well as the E and R/W\ control signals are monitored so that all external bus accesses performed by the processor are interpreted by the DS5303. The DS5303 decodes external bus addresses and controls access to internal I/O resources, to the CMOS RAMs converted by the Softener into NV SRAM, and to external peripherals such as the DS1283 clock/calendar circuit.

CE1\ and CE2\ are the chip enable signals used to control the external CMOS RAM. As illustrated in Figure 2, two different system memory maps can be selected by programming an internal range control bit during system initialization via the Serial Bootstrap Loader. By programming this bit, the chip enable outputs can be assigned to each control either an 8K x 8 or a 32K x 8 CMOS static RAM. As a result, a minimum of 8K bytes up to a maximum of 64K bytes of program/data storage is supported. This operating mode information is retained in the absence of V_{CC}.

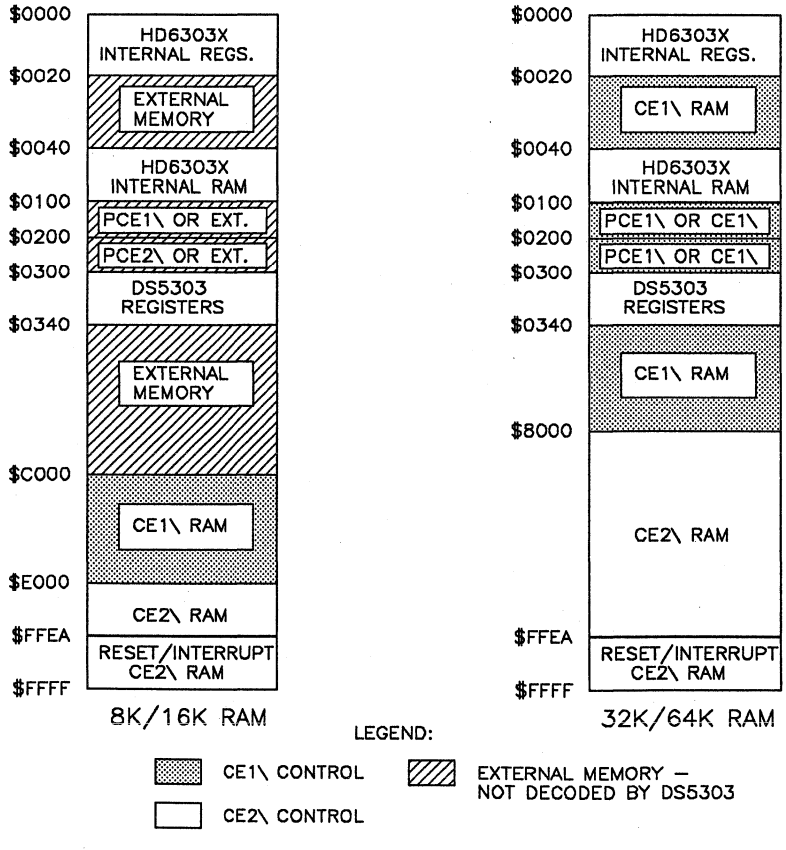
The diagram shown in Figure 2 illustrates the resulting memory maps for a DS5303 used with the HD6303X version. As shown in the figure, the HD6303X processor maps its internal registers in the region from $0000 - $001F and its internal RAM in the region from $0040 - $00FF. As a result, no accesses are performed on its external address and data busses when these internal locations are addressed, and the corresponding locations in NV SRAM under the control of CE1\ are not accessible when a 64K byte range is selected.

For accesses that are performed on the external bus, the DS5303 performs the necessary decoding for its internal registers and the external NV SRAM and peripherals under its control. The DS5303 registers are located in the 64-byte space from $0300 to $033F. If a 32K byte SRAM is interfaced on the CE1\ signal, then the locations within that RAM which correspond to the register space will not be accessible from the processor.

The DS5303 can also be used with other versions of the 6303, with certain implications to the memory map. In fact, the DS2301 6301 Soft Stik is implemented using the HD6303Y. Consult the DS2301 data sheet for further information on this application of the DS5303.

The reset and interrupt vectors for the HD6303 are stored in the region from $FFEA - $FFFF. If a single SRAM (8K x 8 or 32K x 8) is used with the DS5303, then it should be interfaced on the CE2\ line in order to accommodate these vector locations.

FIGURE 2: DS5303 MEMORY MAPS



As described in the DS53xx Micro Softener Chips data sheet, the PCE1\ and PCE2\ lines are available for the interface of peripheral devices.

PARALLEL I/O

The DS5303 Softener Chip incorporates a total of four additional 8-bit parallel I/O ports which are easily accessed by the microprocessor. The ports are designated as A, B, C, and D. These ports function as described in the DS53xx Micro Softener Chips data sheet.

BOOTSTRAP LOADER

The general function of the Serial Bootstrap Loader is described in the DS53xx data sheet.

Motorola Hex representation is the format used to load program/data information into the NV SRAM of a 6303/DS5303-based system. Motorola Hex is the typical format that is generated by existing 6803 assemblers.

A command summary specfically for the DS5303 Serial Bootstrap Loader is given below.

COMMAND	FUNCTION
C [range]	Calculate, store, and report CRC-16 value
D [range]	Dump Motorola Hex
E	Exit Serial Bootstrap Loader
F val [range]	Fill NV SRAM with constant
K	Clear CRC values
L	Load Motorola Hex
N	Set Freshness Seal
R	Read DS5303 Registers
V [range]	Verify Motorola Hex
W	Write DS5303 Register(s)

ORDERING INFORMATION

The following versions of the DS5303 are available as standard products from Dallas Semiconductor:

PART #	CLOCK	PACKAGE
DS5303FP	1.0 MHz	80-pin QFP
DS5303FP-B	2.0 MHz	80-pin QFP

FOR FURTHER INFORMATION

Complete technical specifications for the DS5303 as well as other versions of the Micro Softener and the Soft Stik products are available upon request from Dallas Semiconductor.

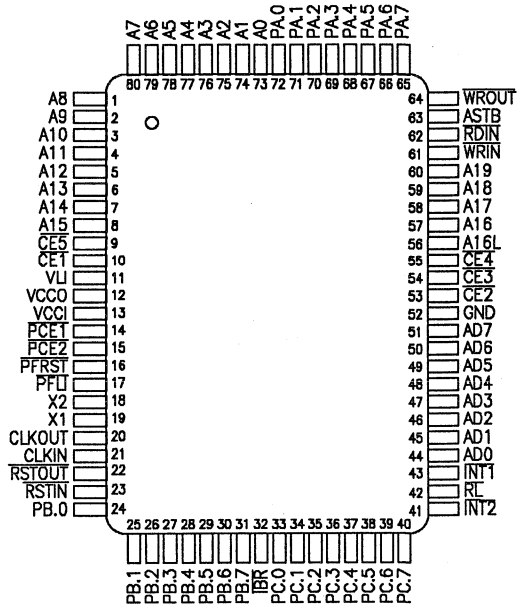
DALLAS SEMICONDUCTOR

DS5340
V40 Softener Chip

FEATURES

- Provides softness for V40-based systems
- Adapts to task-at-hand:
  - -Converts up to 672K bytes of CMOS SRAM into lithium-backed NV program/data storage
  - -Serial bootstrap loading
  - -Code can be changed in end use
- Crashproof operation during transient conditions
- Provides 3 enhanced 8-bit parallel I/O ports

PIN DESCRIPTION



80-Pin Quad Flat Pack

DESCRIPTION

The DS5340 V40 Softener Chip provides the benefits of adaptability, crashproof operation, and enhanced parallel I/O capabilities, as discussed in the DS53xx Micro Softener Chips family data sheet, for systems based on the popular NEC V40 microprocessor. The DS5340 interfaces directly to the V40's address/data bus and control signals and converts up to 672K bytes of CMOS SRAM into nonvolatile read/write storage.

An embedded control system with the above attributes can be implemented using only the V40, DS5340 V40 Softener Chip, CMOS static RAM, and a lithium cell. Additional peripheral functions, such as a permanently powered clock/calendar function (using the DS1283 Watchdog Timekeeper Chip) can be added to the system without the need for additional glue logic. Because the V40 is code-compatible with the 8086, application code can be developed on

a PC in its native instruction set. As a result, a multitude of high-level language compilers, assemblers, and debugging packages are available to support development of a V40/DS5340-based embedded control system.

Also available from Dallas Semiconductor is the DS2340 Soft V40 Flip Stik, which is a complete implementation of the embedded control system described above. The DS2340 is implemented as a small daughterboard that plugs into an industry-standard 72-pin SIMM connector scheme that supports redundant contacts, simple insertion/extraction, and low overall height profiles. The DS2340 can be used as a high-level building block in a system design resulting in a quick time to market for a Softener-based V40 system. Alternatively, it can be used for fast prototyping of a system which will ultimately incorporate the DS5340 V40 Softener Chip itself. Consult the DS2340 data sheet for information on this application of the DS5340.

PIN DESCRIPTION

The table shown below summarizes the pin functions of the DS5340 by function type.

DS5340 PIN DESCRIPTION Table 1

NAME	DESCRIPTION
V_{CCI}	+5V Power Supply Input
GND	Ground
V_{LI}	+3V Lithium Supply Input
V_{CCO}	Lithium-Backed Power Supply Output
PFRST\	Power Fail Reset Output
PFLI\	Power Fail Lithium Output
X1	Crystal Oscillator Input
X2	Crystal Oscillator Output
RL\	Reload Input
CLKIN	Clock Input from V40
CLKOUT	Clock Output
A19-A8	Address Bus Inputs from V40
A16L	Latched A16 Line; Output
AD7-AD0	Mux. Address/Data Bus to/ from V40; bidirectional
ASTB	Address Strobe Input from V40

NAME	DESCRIPTION
MRDIN\	Memory Read Input from V40
MWRIN\	Memory Write Input from V40
A7-A0	Demux. Address Bus; Outputs
CE1\-CE5\	Chip Enable Outputs
PCE1\-PCE2\	Peripheral Chip Enable Outputs
WROUT\	Write Output
RSTIN\	Reset Input
RSTOUT\	Reset Output to V40
INT1\	Interrupt Output 1 to V40
INT2\	Interrupt Output 2 to V40
PA.7-PA.0	Port A; Bidirectional
PB.7-PB.0	Port B; Bidirectional
PC.7-PC.0	Port C; Bidirectional
IBR\	Input Buffer Ready Status Output

BLOCK DIAGRAM

A conceptual block diagram of the DS5340 is shown in Figure 1. Consult the DS53xx Micro Softener Chip family data sheet for complete operational details which are common to all of the versions of the Micro Softener. Features unique to the DS5340 are described below.

MEMORY MAP

The DS5340 interfaces directly to the NEC V40's multiplexed address/data bus. All 20 address lines as well as the ASTB, MRD\, and MWR\ control signals are monitored so that all memory accesses performed by the V40 are interpreted by the DS5340. The V40 Softener Chip decodes incoming addresses and controls access to its internal registers, to external CMOS SRAMs, and to external peripherals such as the DS1283 Watchdog Timekeeper Chip.

CE1\-CE5\ are the chip enable signals used to control the external CMOS SRAMs. The decoding of the chip enable signals is controlled by programming mode control bits within the DS5340 during system initialization via the bootstrap loader. Through selection of these modes, the chip enable outputs can be assigned to control various combinations of 32K x 8 and/or 128K x 8 CMOS SRAMs. This allows a minimum of 64K bytes of program/data storage up to a maximum of 672K bytes of program/data storage. This operating mode information is retained in the absence of V_{CC}.

As illustrated in Figure 2, five different system memory maps can be selected via the mode control bits. Mode 0 implements a contiguous 64K byte memory map for minimal system designs. Address bits A19-A16 are ignored when this mode is in effect. Both CE1\ and CE5\ are intended to be connected to the chip enable inputs of 32K x 8 CMOS SRAMs. CE2\,CE3\, and CE4\ are disabled when mode 0 is in effect. CE1\ is activated for all memory accesses from X0000H to X7FFFH, and CE5\ is activated for all memory accesses from X8000H to XFFFFH. The application program can be written to occupy the contiguous 64K byte area complete with interrupt vector information in the lowest portion of the map and with the reset information at the top portion of the map.

Modes 1-4 all decode the total 1M byte system memory map. As can be seen from the figure, Modes 1-3 select various combinations of 32K x 8 and/or 128K x 8 CMOS SRAMs under control of each of the chip enable signals CE1\-CE5\. When Mode 4 is selected, CE1\ and CE5\ select a 128K x 8 and a 32K x 8 CMOS SRAM, respectively, while CE2\ selects a 512K x 8 CMOS SRAM array. CE3\ and CE4\ are disabled in Mode 4.

As described in the DS53xx Micro Softener Chip family data sheet, the PCE1\ and PCE2\ lines are available for the interface of peripheral devices.

PARALLEL I/O

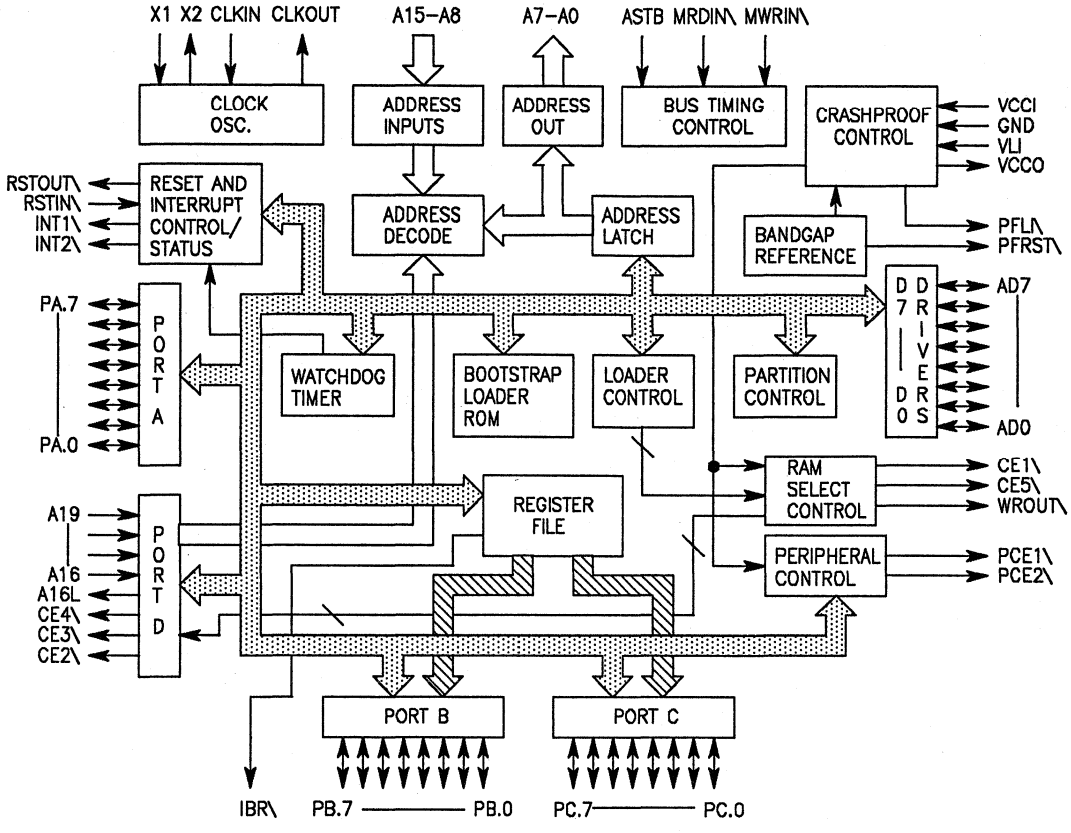
The DS5340 incorporates a total of three additional 8-bit parallel I/O ports which are easily accessed by the microprocessor. The ports are designated as A, B, and C. These ports function as described in the DS53xx data sheet.

BOOTSTRAP LOADER COMMANDS

The general function of the serial bootstrap loader is described in the DS53xx data sheet. In addition to the standard method of communication to a local PC via the V40's on-chip serial I/O port, the DS5340's serial bootstrap loader can be configured to communicate to a host PC at a remote location via a DS2245 Soft Modem Stik in the embedded system.

Extended Intel Hex representation is the format used to load program/data information into the nonvolatile SRAM of a V40/DS5340-based system. Extended Intel Hex is the typical format which is generated by existing 6803 assemblers.

DS5340 V40 SOFTENER BLOCK DIAGRAM Figure 1



DS5340 SERIAL BOOTSTRAP LOADER Table 2

COMMAND	FUNCTION
C [range]	Calculate, store and report CRC-16 value
D [range]	Dump Extended Intel Hex
E	Exit Serial Bootstrap Loader
F val [range]	Fill NV SRAM with Constant
K	Clear CRC values
L	Load Extended Intel Hex
M	Enable/Disable Modem Communication
N	Set Freshness Seal
R	Read DS5340 Registers
V [range]	Verify Extended Intel Hex
W	Write DS5340 Register

A command summary specifically for the DS5340 serial bootstrap loader is given on the preceeding page (Table 2).

ORDERING INFORMATION

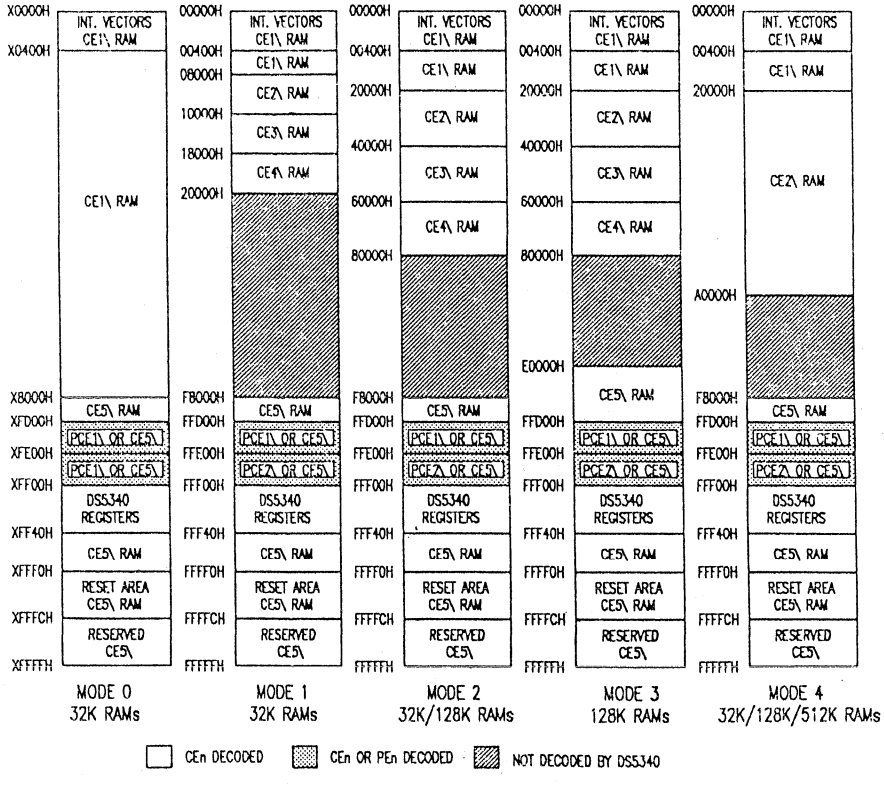
The following versions of the DS5340 are available as standard products from Dallas Semiconductor.

PART #	CLOCK	PACKAGE
DS5340FP	8 MHz	80-pin QFP
DS5340FP-A	10 MHz	80-pin QFP

FOR FURTHER INFORMATION

Complete technical specifications for the DS5340 as well as other versions of the Micro Softener and Soft Stik products are available on request from Dallas Semiconductor.

DS5340 MEMORY MAP MODES Figure 2



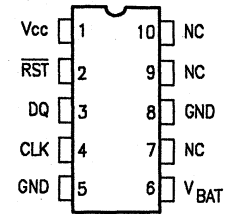
Nonvolatile RAM

DALLAS SEMICONDUCTOR

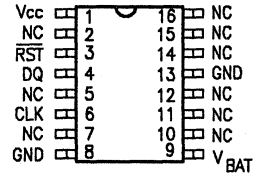
DS1200
Serial RAM Chip

FEATURES
- 1024 bits of read/write memory
- Low data retention current for battery backup applications
- 4 million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Low-power CMOS circuitry
- Applications include:
  - software authorization
  - computer identification
  - system access control
  - secure personnel areas
  - calibration
  - automatic system setup
  - traveling work record

PIN CONNECTIONS



10-Pin DIP (300 MIL)



16-Pin SOIC (300 Mil)

PIN NAMES(\ Denotes Condition Low)

V_{CC}	- +5 Volts
RST\	- RESET
DQ	- Data Input/Output
CLK	- Clock
GND	- Ground
V_{BAT}	- Battery (+)
NC	- No Connection

DESCRIPTION

The DS1200 Serial RAM Chip is a miniature read/write memory which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, RST\, and DATA INPUT/OUTPUT.

Nonvolatility can be achieved by connecting a battery of 2 to 4 volts at the battery input V_{BAT}. A load of 0.5 uA should be used to size the external battery for the required data retention time. If nonvolatility is not required the V_{BAT} pin should be grounded.

For a complete description of operating conditions, electrical characteristics, bus timing, and signal descriptions other than V_{BAT}, see the DS1201 Electronic Tag 1024-Bit data sheet.

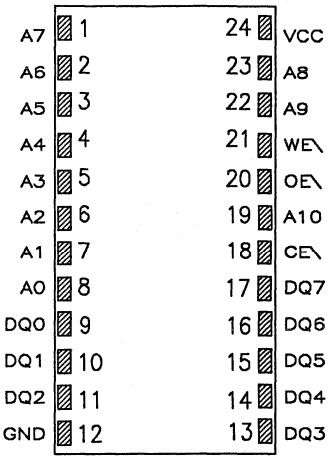
DALLAS SEMICONDUCTOR

DS1220AB/AD
16K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN DESCRIPTION



24-PIN ENCAPSULATED PACKAGE
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A_0-A_{10}	- Address Inputs
CE\	- Chip Enable
GND	- Ground
DQ_0-DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
WE\	- Write Enable
OE\	- Output Enable

DESCRIPTION

The DS1220AB and DS1220AD are 16,384-bit, fully static, nonvolatile RAMs organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The DS1220AB/AD can be used in place of existing 2K x 8 SRAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220AB also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220AB and DS1220AD execute a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that the CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1220AB and DS1220AD are in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1220AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5V. The DS1220AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1220AD and 4.75 volts for the DS1220AB.

SHIPPING AND START-UP

The DS1220AB/AD is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS
DS1220AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
DS1220AD Power Supply Voltage	V_{CC}	4.50	5.0	5.50	V
Input Logic 1	V_{IH}	2.2		V_{CC}	V
Input Logic 0	V_{IL}	0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10% for DS1220AD)
(0°C to 70°C; V_{CC} = 5V ± 5% for DS1220AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-1.0		+1.0	uA
I/O Leakage Current CE\ ≥ V_{IH} ≤ V_{CC}	I_{IO}	-1.0		+1.0	uA
Output Current @ 2.4V	I_{OH}	-1.0			mA
Output Current @ 0.4V	I_{OL}	2.0			mA
Standby Current CE\=2.2V	I_{CCS1}		5.0	10.0	mA
Standby Current CE\= V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA
Operating Current t_{CYC}=200ns (Commercial)	I_{CCO1}			75	mA
Operating Current t_{CYC}=200ns (Industrial)	I_{CCO1}			85	mA
Write Protection Voltage (DS1220AB)	V_{TP}	4.5	4.62	4.75	V
Write Protection Voltage (DS1220AD)	V_{TP}	4.25	4.37	4.5	V

DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/Output Capacitance	$C_{I/O}$	5	10	pF

AC ELECTRICAL CHARACTERISTICS

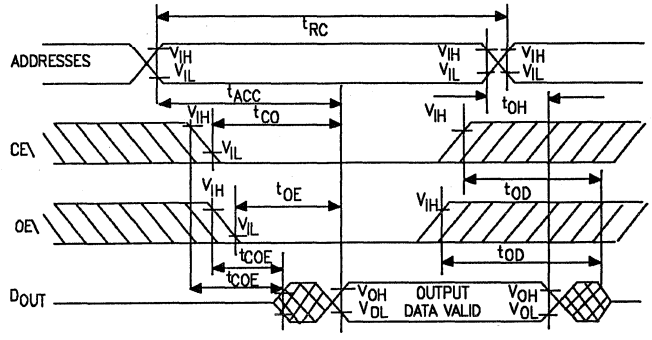
(0°C to 70°C, V_{CC} = 5.0V ± 10% for DS1220AD)
(0°C to 70°C, V_{CC} = 5.0V ± 5% for DS1220AB)

		DS1220AD-100 / DS1220AB-100		DS1220AD-120 / DS1220AB-120		DS1220AD-150 / DS1220AB-150		DS1220AD-200 / DS1220AB-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		150		200		ns	
Access Time	t_{ACC}		100		120		150		200	ns	
OE\ to Output Valid	t_{OE}		50		60		70		100	ns	
CE\ to Output Valid	t_{CO}		100		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		35		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	100		120		150		200		ns	
Write Pulse Width	t_{WP}	75		90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		20		ns	
Output High Z from WE\	t_{ODW}		35		40		70		80	ns	5
Output Active from WE\	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	40		50		60		80		ns	4
Data Hold Time	t_{DH}	20		20		20		20		ns	4

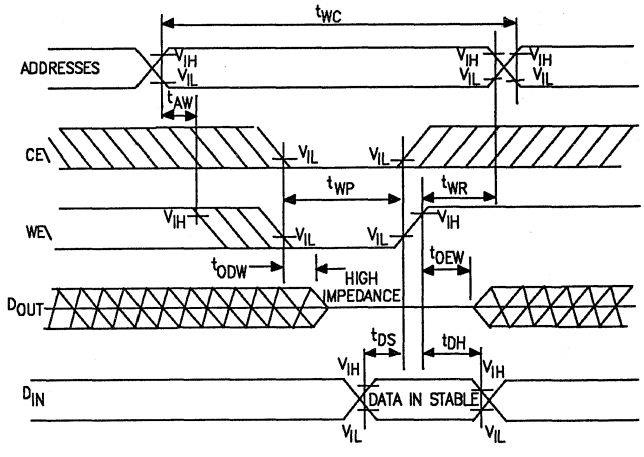
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0V - 3.0V
Timing Measurement Reference Levels:
Input: 1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

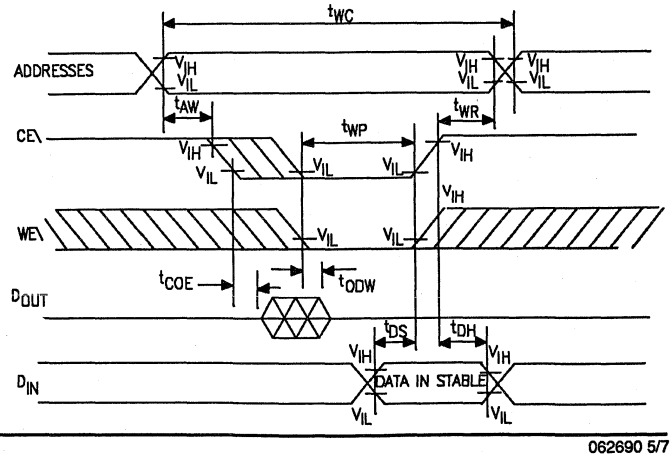
READ CYCLE (1)



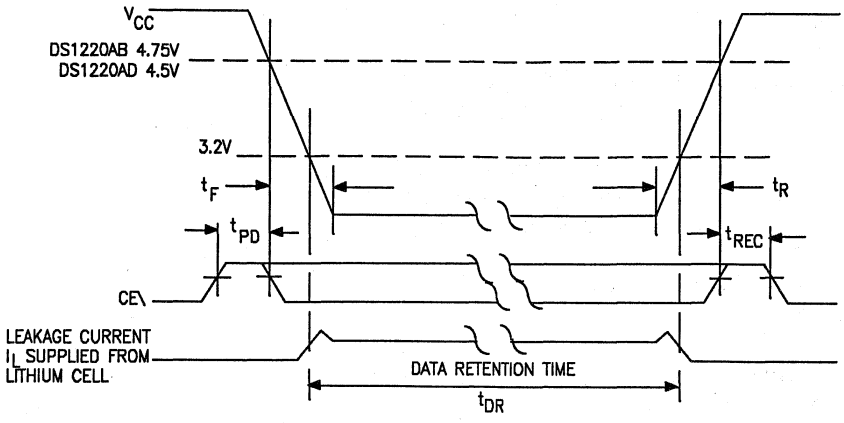
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	10
t_F	V_{CC} Slew from 4.75V to 0V (CE\ at V_{IH})	300		us	DS1220AB
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	300		us	DS1220AD
t_R	V_{CC} Slew from 0V to 4.75V (CE\ at V_{IH})	0		us	DS1220AB
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	0		us	DS1220AD
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in the battery backup mode.

NOTES:

1. WE\ is high for a Read Cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1220 AB/AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

10. See the DS1210 Nonvolatile Controller Chip data sheet for battery backup operation.

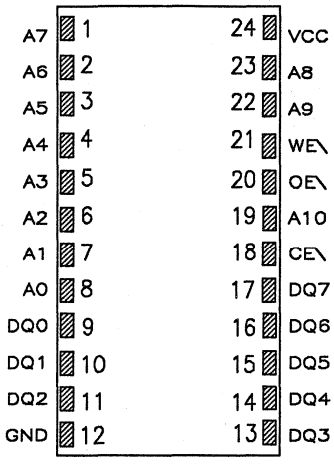
DALLAS SEMICONDUCTOR

DS1220Y
16K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 2K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 24-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN DESCRIPTION



24-Pin Encapsulated Package
(720 mil Extended)

PIN NAMES

A_0-A_{10} - Address Inputs
CE\ - Chip Enable
GND - Ground
DQ_0-DQ_7 - Data In/Data Out
V_{CC} - Power (+5V)
WE\ - Write Enable
OE\ - Output Enable
V_{CC} -Power (+5V)

DESCRIPTION

The DS1220Y 16K Nonvolatile SRAM is a 16,384-bit, fully static, nonvolatile RAM organized as 2048 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 2K x 8 RAMs directly conforming to the popular bytewide 24-pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1220Y executes a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 11 address inputs (A_0-A_{10}) defines which of the 2048 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1220Y is in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The NV SRAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1220Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Logic 1	V_{IH}	2.2		V_{CC}	V
Input Logic 0	V_{IL}	0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	
I/O Leakage Current CE\ ≥ V_{IH} ≤ V_{CC}	I_{IO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current CE\=2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current CE\=V_{CC} - 0.5V	I_{CCS2}		2.0	4.0	mA	
Operating Current t_{CYC}= 200ns (Commercial)	I_{CCO1}			75	mA	
Operating Current t_{CYC}= 200ns (Industrial)	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}		4.20		V	10

DC TEST CONDITIONS

Outputs open.
All voltages are referenced to ground.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/Output Capacitance	$C_{I/O}$	5	10	pF

AC ELECTRICAL CHARACTERISTICS

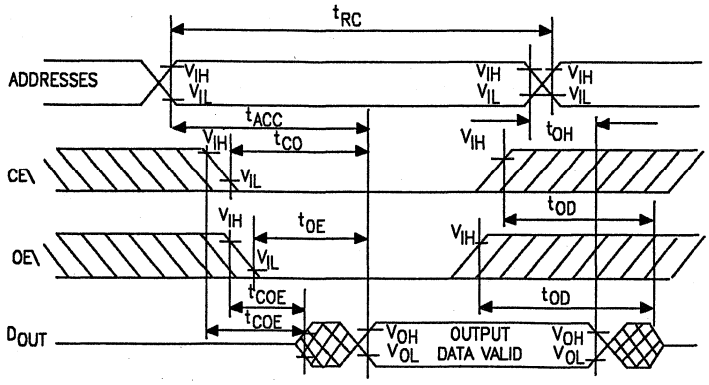
(0°C to 70°C; V_{CC}=5.0V±10%)

		DS1220Y-100		DS1220Y-120		DS1220Y-150		DS1220Y-200		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Read Cycle Time	t_{RC}	100ns		120ns		150ns		200ns		
Access Time	t_{ACC}		100ns		120ns		150ns		200ns	
OE\ to Output Valid	t_{OE}		50ns		60ns		70ns		100ns	
CE\ to Output Valid	t_{CO}		100ns		120ns		150ns		200ns	
OE\ or CE\ to Output Active	t_{COE}	5ns		5ns		5ns		5ns		5
Output High Z from Deselection	t_{OD}		35ns		40ns		70ns		100ns	5
Output Hold from Address Change	t_{OH}	5ns		5ns		5ns		5ns		
Write Cycle Time	t_{WC}	100ns		120ns		150ns		200ns		
Write Pulse Width	t_{WP}	75ns		90ns		100ns		150ns		3
Address Setup Time	t_{AW}	0ns		0ns		0ns		0ns		
Write Recovery Time	t_{WR}	20ns		20ns		20ns		20ns		
Output High Z from WE\	t_{ODW}		35ns		40ns		70ns		80ns	5
Output Active from WE\	t_{OEW}	5ns		5ns		5ns		5ns		5
Data Setup Time	t_{DS}	40ns		50ns		60ns		80ns		4
Data Hold Time	t_{DH}	20ns		20ns		20ns		20ns		4

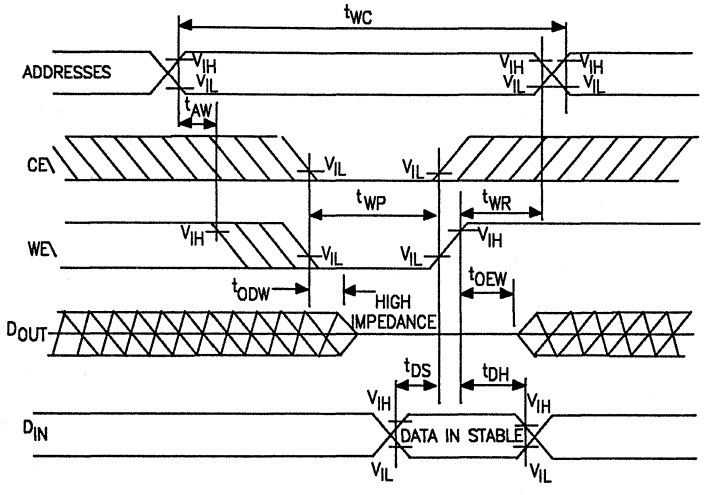
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

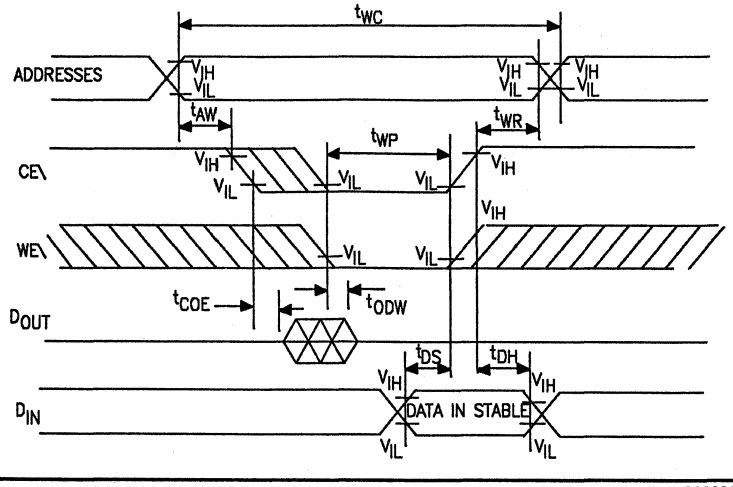
READ CYCLE (1)



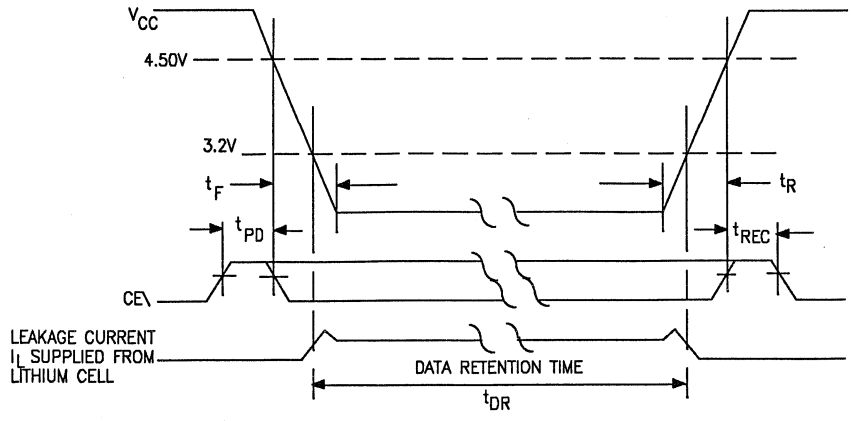
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS
t_{PD}	CE\ at V_{IH} before Power-Down	0		us
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	100		us
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		us
t_{REC}	CE\ at V_{IH} after Power-Up		2	ms

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. WE\ is high for a read cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during the write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1220Y is marked with a four-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

10. Power supply noise transients may activate the write-protect circuitry of the DS1220Y if those transients are less than V_{CCMIN}. A decoupling capacitor of 0.10uF across the device supply pins is recommended to reduce these transients.

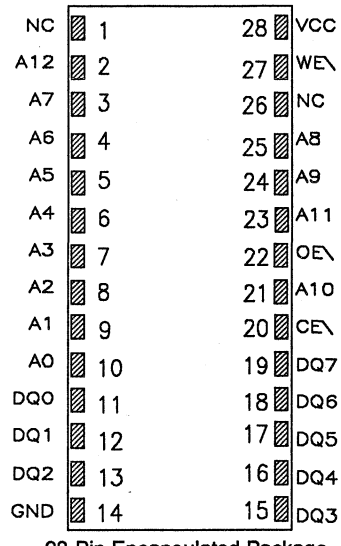
DALLAS SEMICONDUCTOR

DS1225AB/AD
64K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, 170ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN DESCRIPTION



28-Pin Encapsulated Package
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A_0 - A_{12} - Address Inputs
CE\ - Chip Enable
GND - Ground
DQ_0-DQ_7 - Data In/Data Out
V_{CC} - Power (+5V)
WE\ - Write Enable
OE\ - Output Enable
NC - No Connect

DESCRIPTION

The DS1225AB and DS1225AD 64K Nonvolatile SRAMs are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 8K x 8 static RAM directly conforming to the popular bytewide 28-pin DIP standard. The DS1225AB also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION - READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

OPERATION - WRITE MODE

The DS1225AB and DS1225AD are in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

OPERATION - DATA RETENTION MODE

The DS1225AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1225AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The NV SRAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1225AD and 4.75 volts for the DS1225AB.

FRESHNESS SEAL

The DS1225AB and DS1225AD are shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10% for DS1225AD) (0°C to 70°C; V_{CC} = 5V ± 5% for DS1225AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	10
I/O Leakage Current CE\ ≥ V_{IH} ≤VCC	I_{IO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current CE\ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current CE\ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=200ns (Comm.)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=200ns (Ind.)	I_{CCO1}			85	mA	
Write Protection Voltage (DS1225AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1225AD)	V_{TP}	4.25	4.37	4.5	V	

DC Test Conditions
Outputs Open
All voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/Output Capacitance	$C_{I/O}$	5	10	pF

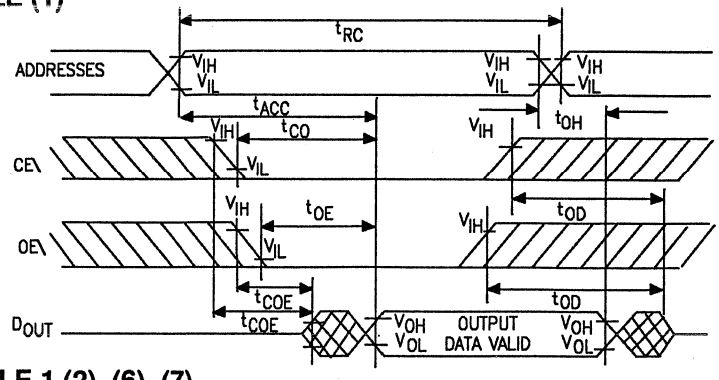
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10% for DS1225AD)
(0°C to 70°C; V_{CC} = 5V ± 5% for DS1225AB)

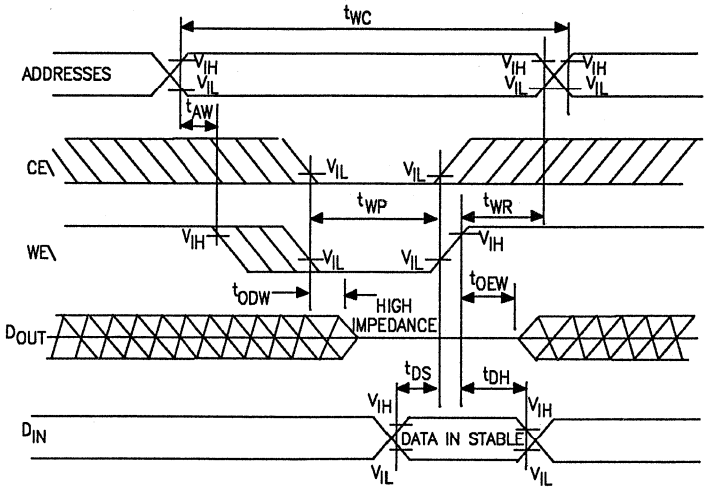
PARAMETER	SYM	DS1225-100		DS1225-120		DS1225-150		DS1225-200		NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	100ns		120ns		150ns		200ns		
Access Time	t_{ACC}		100ns		120ns		150ns		200ns	
OE\ to Output Valid	t_{OE}		50ns		60ns		70ns		100ns	
CE\ to Output Valid	t_{CO}		100ns		120ns		150ns		200ns	
OE\ or CE\ to Output Active	t_{COE}	5ns		5ns		5ns		5ns		5
Output High Z from Deselection	t_{OD}		35ns		40ns		70ns		100ns	5
Output Hold from Address Change	t_{OH}	5ns		5ns		5ns		5ns		
Write Cycle Time	t_{WC}	100ns		120ns		150ns		200ns		
Write Pulse Width	t_{WP}	75ns		90ns		100ns		150ns		3
Address Setup Time	t_{AW}	0ns		0ns		0ns		0ns		
Write Recovery Time	t_{WR}	20ns		20ns		20ns		20ns		
Output High Z from WE\	t_{ODW}		35ns		40ns		70ns		80ns	5
Output Active from WE\	t_{OEW}	5ns		5ns		5ns		5ns		5
Data Setup Time	t_{DS}	40ns		50ns		60ns		80ns		4
Data Hold Time	t_{DH}	20ns		20ns		20ns		20ns		4

AC Test Conditions
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

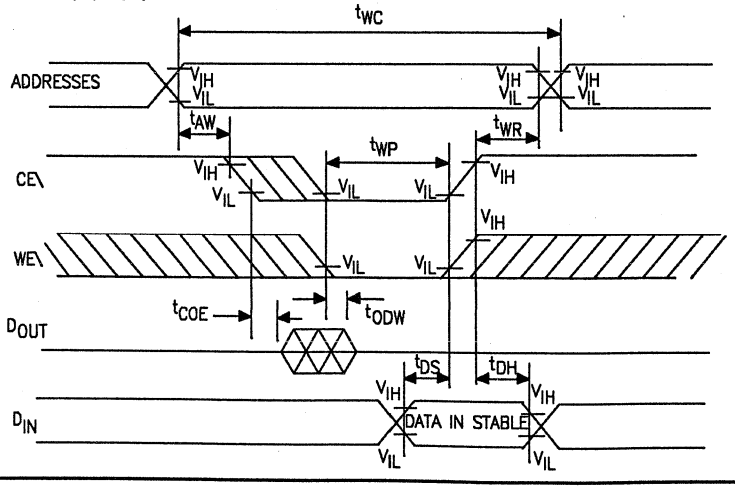
READ CYCLE (1)



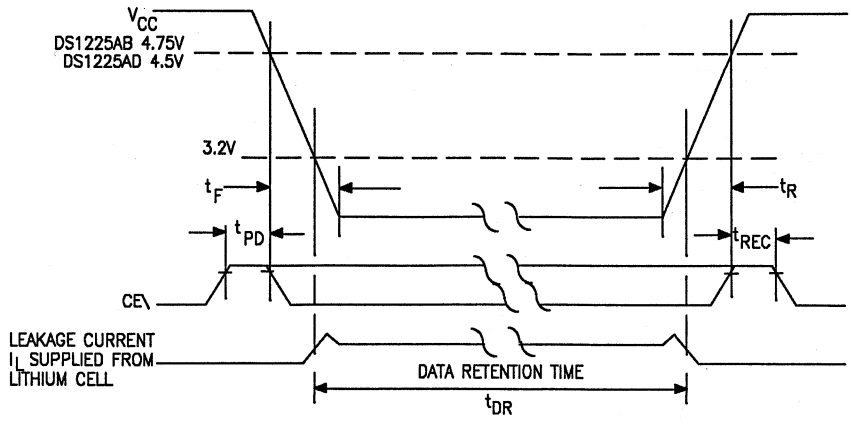
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} Slew from 4.75V to 0V (CE\ at V_{IH})	300		us	DS1225AB
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	300		us	DS1225AD
t_R	V_{CC} Slew from 0V to 4.75V (CE\ at V_{IH})	0		us	DS1225AB
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		us	DS1225AD
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. WE\ is high for a Read Cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1225 AB/AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

10. Measured with CE\ high.

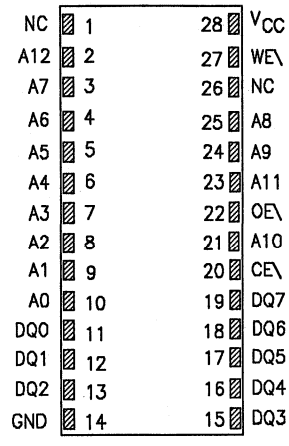
DALLAS SEMICONDUCTOR

DS1225D/E
64K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically write protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Available in 70 or 100 ns read access times
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Read cycle time equals write cycle time
- Optional ±5% and ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN DESCRIPTION



28-Pin Encapsulated Package
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A0-A12	Address Inputs
CE\	Chip Enable
GND	Ground
DQ0-DQ7	Data In/Data Out
V_{CC}	Power (+5V)
WE\	Write Enable
OE\	Output Enable
NC	No Connect

NOTE: Pins 1 & 26 missing by design

DESCRIPTION

The DS1225D and DS1225E are 65,536-bit, fully static, nonvolatile RAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 8K x 8 static RAM directly conforming to the popular bytewide 28-pin DIP standard. The DS1225D/E also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION - READ MODE

The DS1225D/E executes a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A0-A12) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

OPERATION - WRITE MODE

The DS1225D/E are in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

OPERATION - DATA RETENTION MODE

The DS1225E provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1225D provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The NV SRAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for the DS1225D and 4.75 volts for the DS1225E.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
DS1225D Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
DS1225E Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10% for DS1225D)
(0°C to 70°C; V_{CC} = 5V ± 5% for DS1225E)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	10
I/O Leakage Current CE\ ≥ V_{IH} ≤V_{CC}	I_{IO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current CE\ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current CE\ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=100ns (Comm.)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=100ns (Ind.)	I_{CCO1}			85	mA	
Write Protection Voltage (DS1225E)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1225D)	V_{TP}	4.25	4.37	4.5	V	

DC Test Conditions
Outputs Open
All voltages are referenced to ground.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/Output Capacitance	$C_{I/O}$	5	10	pF

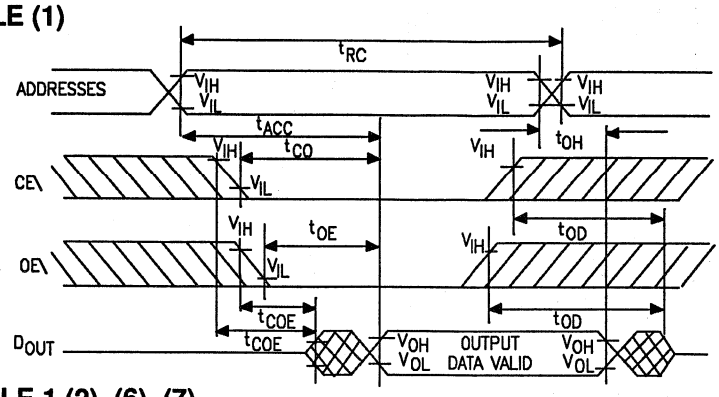
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10% for DS1225D)
(0°C to 70°C; V_{CC} = 5V ± 5% for DS1225E)

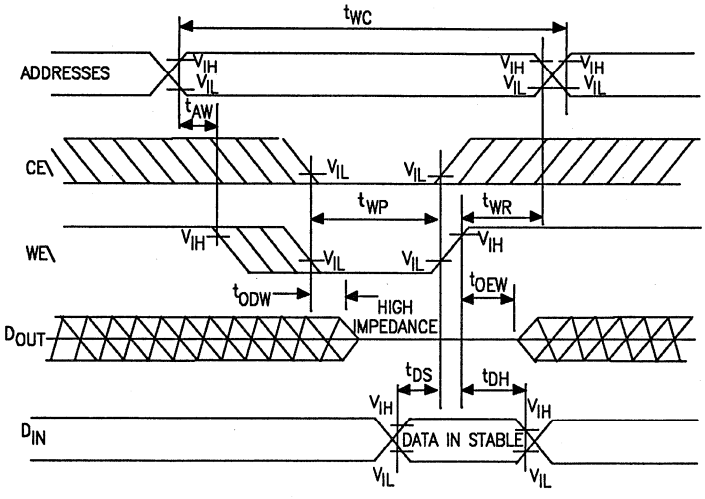
PARAMETER	SYM	DS1225D/E-70		DS1225D/E-100			
		MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100		
OE\ to Output Valid	t_{OE}		35		50	ns	
CE\ to Output Valid	t_{CO}		70		100		
OE\ or CE\ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR}	20		20		ns	
Output High Z from WE\	t_{ODW}		25		35	ns	5
Output Active from WE\	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH}	20		20		ns	4

AC Test Conditions
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

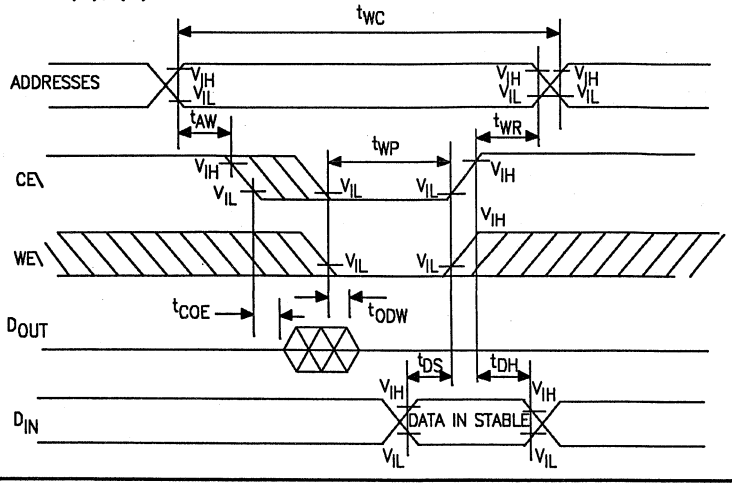
READ CYCLE (1)



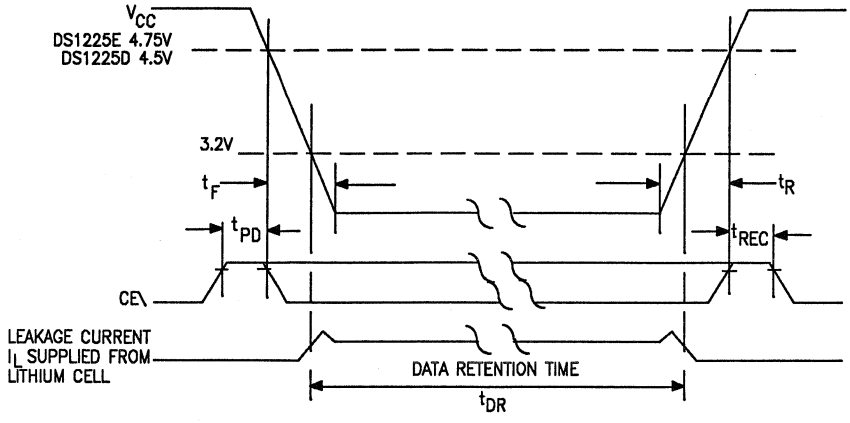
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} Slew from 4.75V to 0V (CE\ at V_{IH})	300		us	DS1225E
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	300		us	DS1225D
t_R	V_{CC} Slew from 0V to 4.75V (CE\ at V_{IH})	0		us	DS1225E
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		us	DS1225D
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. WE\ is high for a Read Cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1225D/E has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

10. Measured with CE\ high.

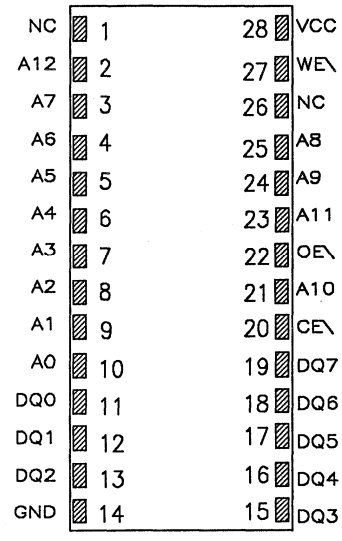
DALLAS SEMICONDUCTOR

DS1225Y
64K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 100ns, 120ns, 150ns, 170ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN DESCRIPTION



28-Pin Encapsulated Package
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A_0 - A_{12} - Address Inputs
CE\ - Chip Enable
GND - Ground
DQ_0-DQ_7 - Data In/Data Out
V_{CC} - Power (+5V)
WE\ - Write Enable
OE\ - Output Enable
NC - No Connect

DESCRIPTION

The DS1225Y 64K Nonvolatile SRAM is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source automatically switches on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 8K x 8 static RAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1225Y executes a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1225Y is in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The NV SRAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1225Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Logic 1	V_{IH}	2.2		V_{CC}	V
Input Logic 0	V_{IL}	0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	11
I/O Leakage Current CE\ ≥ V_{IH} ≤ V_{CC}	I_{IO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current CE\ = 2.2V	I_{CCS1}		3.0	7.0	mA	
Standby Current CE\ = V_{CC}-0.5V	I_{CCS2}		2.0	4.0	mA	
Operating Current t_{CYC}=200ns (Comm.)	I_{CCO1}			75	mA	
Operating Current t_{CYC}=200ns (Ind.)	I_{CCO1}			85	mA	
Write Protection Voltage	V_{TP}		4.20		V	10

DC Test Conditions

Outputs open.
All voltages are referenced to ground.

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=5.0V+/-10%)

		DS1225Y-100		DS1225Y-120		DS1225Y-150		DS1225Y-200		
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**NOTES**
Read Cycle Time	t_{RC}	100ns		120ns		150ns		200ns		
Access Time	t_{ACC}		100ns		120ns		150ns		200ns	
OE\ to Output Valid	t_{OE}		50ns		60ns		70ns		100ns	
CE\ to Output Valid	t_{CO}		100ns		120ns		150ns		200ns	
OE\ or CE\ to Output Active	t_{COE}	5ns		5ns		5ns		5ns		5
Output High Z from Deselection	t_{OD}		35ns		40ns		70ns		100ns	5
Output Hold from Address Change	t_{OH}	5ns		5ns		5ns		5ns		
Write Cycle Time	t_{WC}	100ns		120ns		150ns		200ns		
Write Pulse Width	t_{WP}	75ns		90ns		100ns		150ns		3
Address Setup Time	t_{AW}	0ns		0ns		0ns		0ns		
Write Recovery Time	t_{WR}	20ns		20ns		20ns		20ns		
Output High Z from WE\	t_{ODW}		35ns		40ns		70ns		80ns	5
Output Active from WE\	t_{OEW}	5ns		5ns		5ns		5ns		5
Data Setup Time	t_{DS}	40ns		50ns		60ns		80ns		4
Data Hold Time	t_{DH}	20ns		20ns		20ns		20ns		4

AC Test Conditions

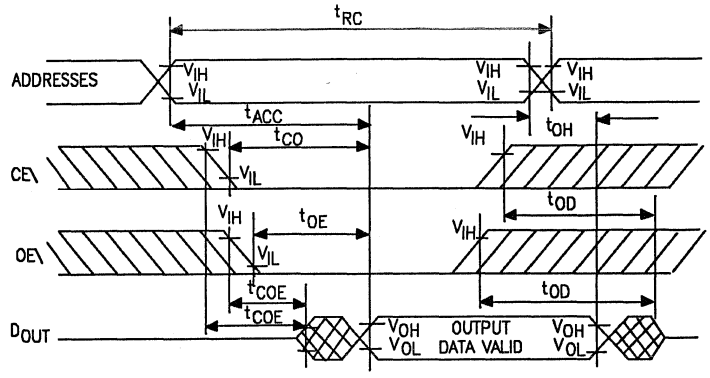
Output Load: 100pF + 1TTL Gate
Input Pulse Levels:: 0-3.0V
Timing Measurement Reference Levels
Input:1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

CAPACITANCE

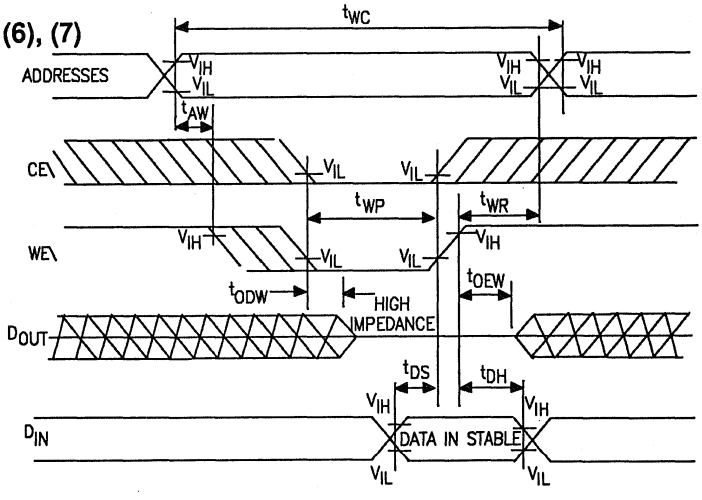
(t_A = 25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/Output Capacitance	$C_{I/O}$	5	10	pF

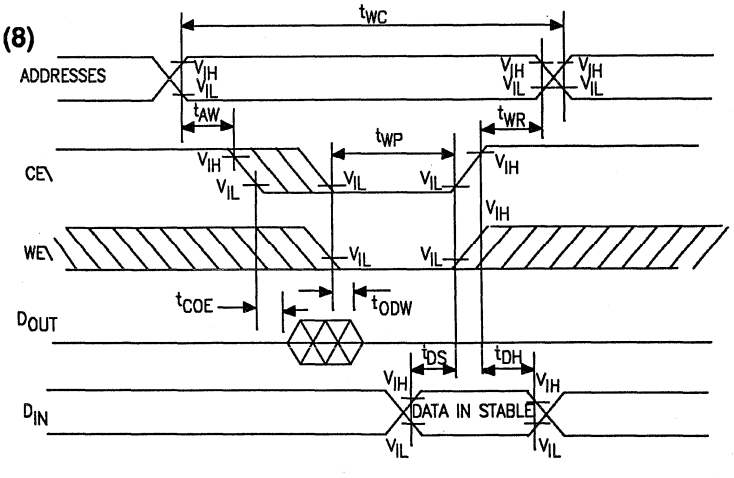
READ CYCLE (1)



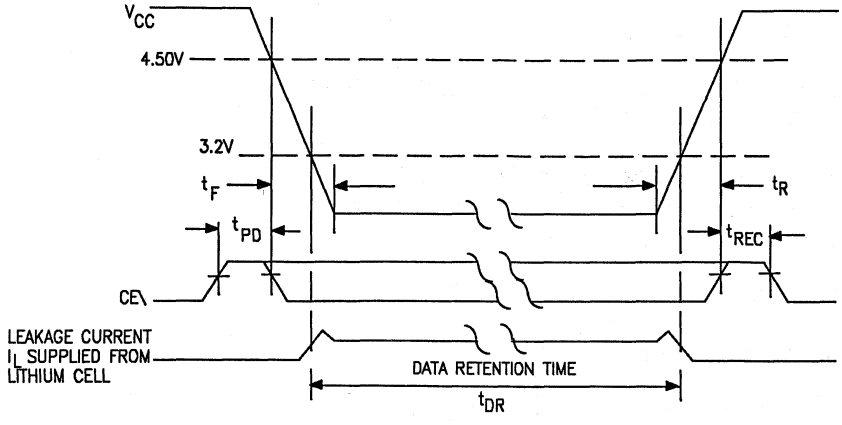
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	100		us	
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		us	
t_{REC}	CE\ at V_{IH} after Power-Up		2	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. WE\ is high for a read cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

10. Power supply noise transients may activate the write-protect circuitry of the DS1225Y if those transients are less than V_{CCmin}. A decoupling capacitor of 0.10uF across the device supply pins is recommended to reduce these transients.

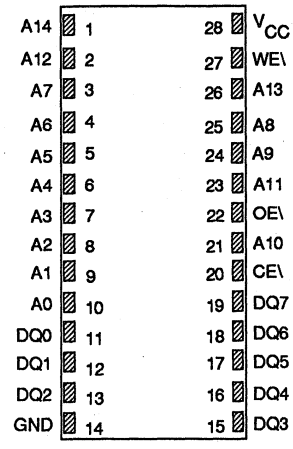
11. Measure with CE\ high.

DALLAS SEMICONDUCTOR

DS1230Y/AB
256K Nonvolatile SRAM

FEATURES
- Data retention in the absence of V_{CC}
- Data is automatically protected during the decrease in V_{CC} at power loss
- Directly replaces 32K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70ns, 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional ±5% and ±10% operating range

PIN DESCRIPTION



28-Pin Encapsulated Package
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A0 - A14	- Address Inputs
CE\	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
WE\	- Write Enable
OE\	- Output Enable

DESCRIPTION
The DS1230AB and DS1230Y 256K Nonvolatile SRAMs are 262,144-bit, fully static, nonvolatile RAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 32K x 8 static RAMs directly conforming to the popular bytewide 28-pin DIP standard. The DS1230AB also matches the pinout of the 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

READ MODE

The DS1230AB and DS1230Y execute a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0-A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1230AB and DS1230Y are in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1230AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1230Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for DS1230Y and 4.75 volts for the DS1230AB.

FRESHNESS SEAL AND BATTERY REDUNDANCY

The DS1230Y and DS1230AB are shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

Battery redundancy is also provided to ensure reliability. The DS1230Y and DS1230AB contain two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1230AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1230Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10% for DS1230Y)
(0°C to 70°C; V_{CC} = 5V ±5%forDS1230AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	
I/O Leakage Current CE\ ≥ V_{IH} ≤ V_{CC}	I_{IO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current CE\=2.2V	I_{CCS1}		5.0	10	mA	
Standby Current CE\=V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 200ns	I_{CCO1}			85	mA	
Write Protection Voltage (DS1230AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1230Y)	V_{TP}	4.25	4.37	4.5	V	

DC Test Conditions:
Outputs open; all voltages are referenced to ground.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	$C_{I/O}$	5	10	pF	

AC ELECTRICAL CHARACTERISTICS

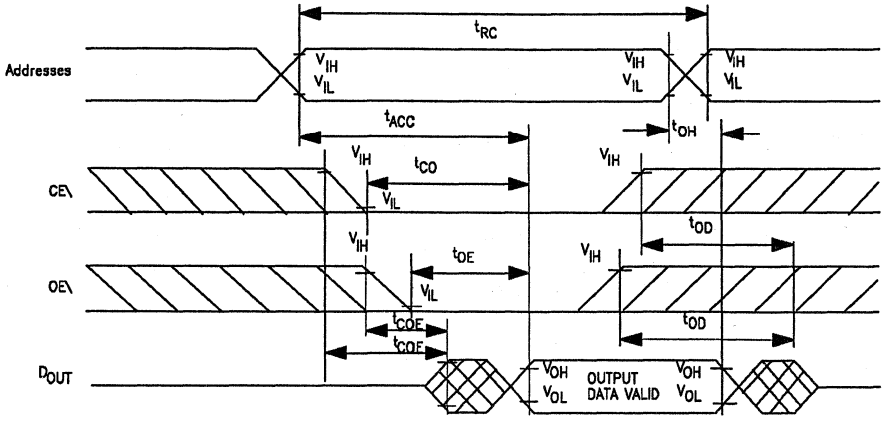
($0^{o}C$ to $70^{o}C$; V_{CC}=5.0V ± 10% for DS1230Y)
($0^{o}C$ to $70^{o}C$; V_{CC}=5.0V ± 5% for DS1230AB)

		DS1230Y-70 1230AB-70		DS1230Y-100 1230AB-100		DS1230Y-120 1230AB-120		DS1230Y-150 1230AB-150		DS1230Y-200 DS1230AB-200			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Read Cycle Time	t_{RC}	70		100		120		150		200		ns	
Access Time	t_{ACC}		70		100		120		150		200	ns	
OE\ to Output Valid	t_{OE}		35		50		60		70		100	ns	
CE\ to Output Valid	t_{CO}		70		100		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		5		ns	
Write Cycle Time	t_{WC}	70		100		120		150ns		200		ns	
Write Pulse Width	t_{WP}	55		75		90		100		100		ns	3
Address Setup Time	t_{AW}	0		0		0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		20		20		ns	
Output High Z from WE\	t_{ODW}		25		35		40		70		80	ns	5
Output Active from WE\	t_{OEW}	5		5		5		5		5		ns	5
Data Setup Time	t_{DS}	30		40		50		60		80		ns	4
Data Hold Time from WE\	t_{DH}	20		20		20		20		20		ns	4

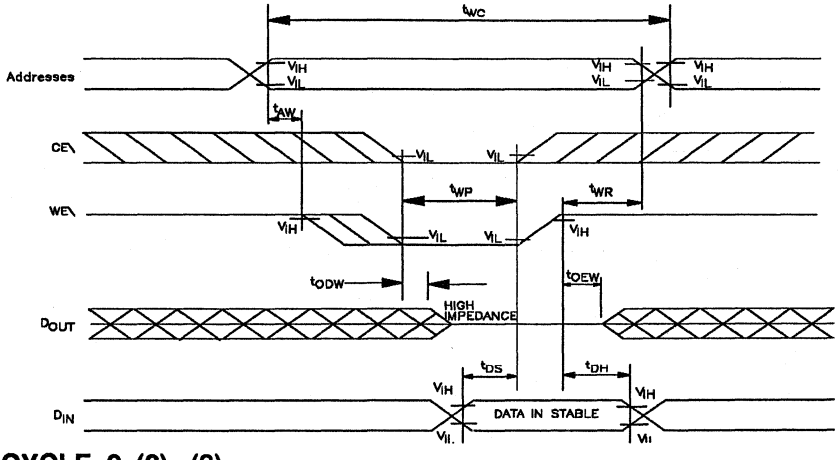
AC Test Conditions

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

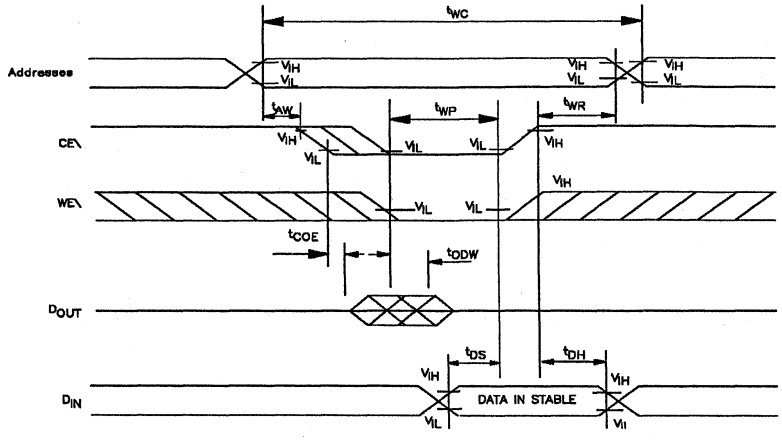
READ CYCLE (1)



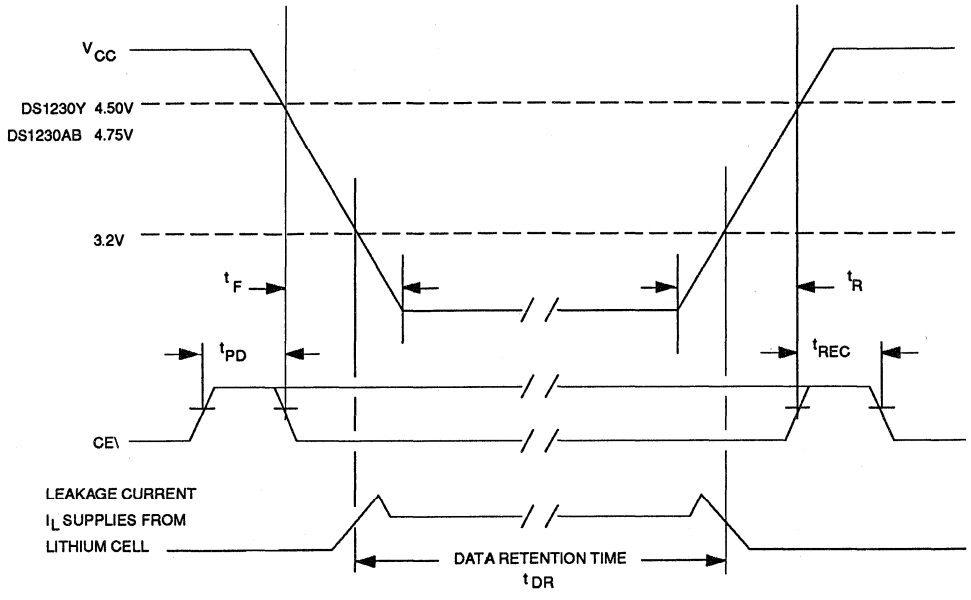
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} Slew from 4.75V to 0V (CE\ at V_{IH})	300		us	DS1230AB
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	300		us	DS1230Y
t_R	V_{CC} Slew from 0V to 4.75V (CE\ at V_{IH})	0		us	DS1230AB
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		us	DS1230Y
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. WE\ is high for a read cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\.
t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1230 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

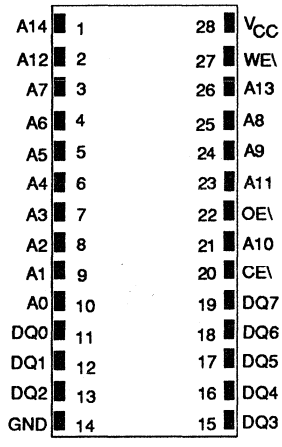
DALLAS SEMICONDUCTOR

DS1235Y/AB
256K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 32K x 8 volatile static RAMs or EEPROMs
- Unlimited write cycles
- Low-power CMOS
- Over 5 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 100, 120, 150, and 200 ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ± 10% operating range (DS1235Y)
- Optional ± 5% operation range (DS1235AB)

PIN DESCRIPTION



28-PIN ENCAPSULATED PACKAGE
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A0 - A14	- Address Inputs
CE\	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
WE\	- Write Enable
OE\	- Output Enable

DESCRIPTION

The DS1235Y/AB 256K Nonvolatile SRAM is a 262, 144-bit, fully static SRAM organized as 32,768 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

The nonvolatile SRAM can be used in place of existing 32K x 8 SRAMs directly conforming to the popular bytewide 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

READ MODE

The DS1235Y/AB executes a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0-A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\, rather than address access.

WRITE MODE

The DS1235Y/AB is in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile SRAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25V nominal (V_{CC} greater than 4.75V and write protect at 4.62V nominal for DS1235AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1235Y/AB constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself; all inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for the DS1235AB).

FRESHNESS SEAL AND SHIPPING

The DS1235Y/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

BATTERY REDUNDANCY

Battery redundancy ensures reliability. The DS1235Y/AB contains two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1235Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1235AB Power Supply Voltage	V_{CC}	4.75	5.0	4.25	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

(0°C to 70°C; V_{CC}=5V +/- 10% for DS1235Y)

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V +/- 5% for DS1235AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	*u* A	
I/O Leakage Current CE\≥V_{IH}≤V_{CC}	I_{IO}	-1.0		+1.0	*u* A	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current CE\ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current CE\ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CC01}			85	mA	
Write Protection Voltage (DS1235Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1235AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A=25°C)

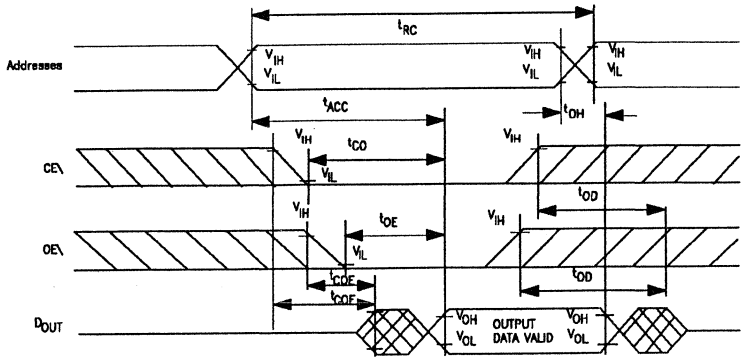
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

AC ELECTRICAL CHARACTERISTICS

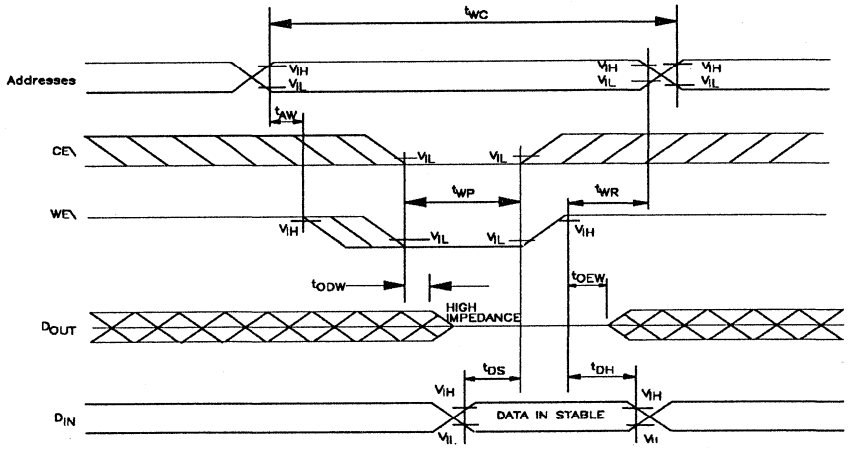
(0°C to 70°C; V_{CC}=5.0V ± 10% for DS1235Y)
(0°C to 70°C; V_{CC}=5.0V ± 5% for DS1235AB)

		DS1235Y/AB-100		DS1235Y/AB-120		DS1235Y/AB-150		DS1235Y/AB-200			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		150		200		ns	
Access Time	t_{ACC}		100		120		150		200	ns	
OE\ to Output Valid	t_{OE}		50		60		70		100	ns	
CE\ to Output Valid	t_{CO}		100		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		5		ns	5
Output High Z From De-selection	t_{OD}		35		40		70		100	ns	5
Output Hold From Address Change	t_{OH}	5		5		5		5		ns	
Write Cycle Time	t_{WC}	100		120		150		200		ns	
Write Pulse Width	t_{WP}	75		90		100		150		ns	3
Address Setup Time	t_{AW}	0		0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		20		ns	
Output High Z From WE\	t_{ODW}		35		40		70		80	ns	5
Output Active From WE\	t_{OEW}	5		5		5		5		ns	5
Data Setup Time	t_{DS}	40		50		60		80		ns	4
Data Hold Time	t_{DH}	20		20		20		20		ns	4

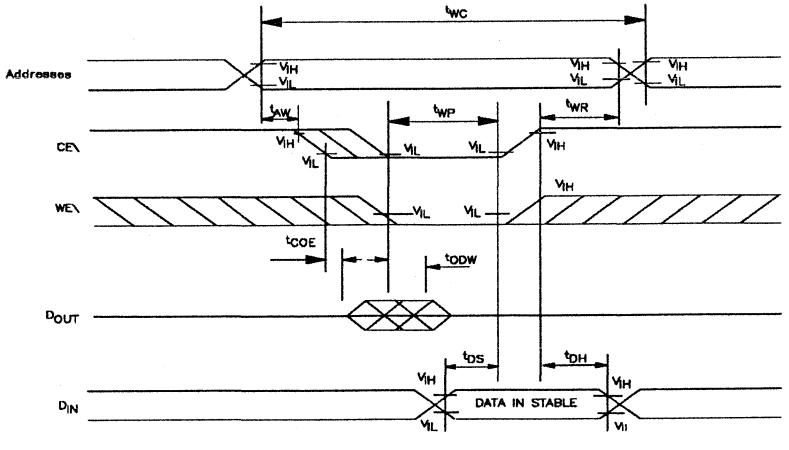
READ CYCLE (Note 1)



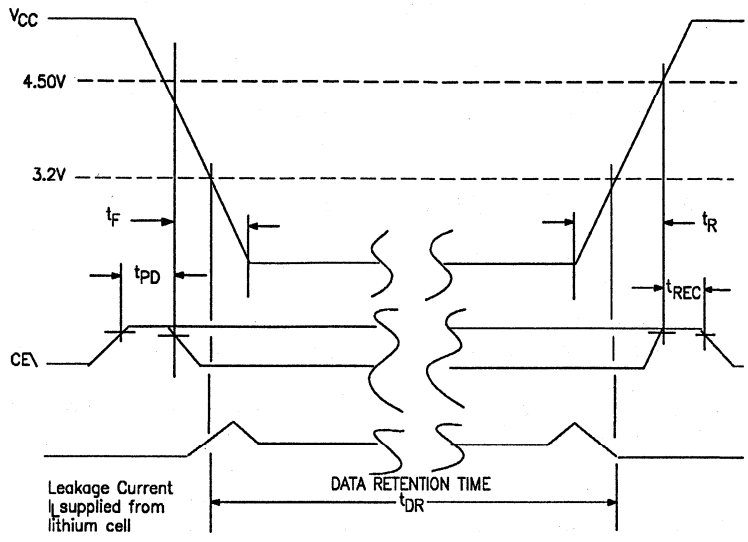
WRITE CYCLE 1 (Notes 2, 6, 7)



WRITE CYCLE 2 (Notes 2, 8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		*u* s	
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	300		*u* s	
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	0		*u* s	
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. WE\ is high for a read cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\.
   t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in write Cycle 1, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.

9. Each DS1235Y/AB has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

DC Test Conditions

Outputs Open
t Cycle = 200ns
All Voltages Are Referenced to Ground

AC Test Conditions

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

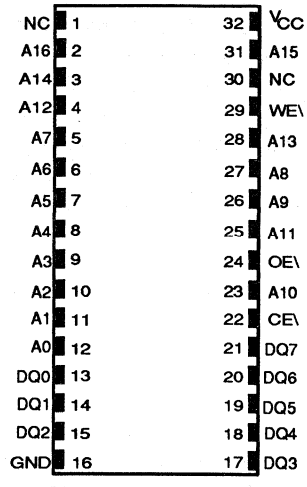
DALLAS SEMICONDUCTOR

DS1245Y/AB
1024K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 128K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in either 100 or 120 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range (DS1245Y)
- Optional ± 5% operating range (DS1245AB)
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

PIN DESCRIPTION



32-Pin Encapsulated Package
(740 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A0 - A16	- Address Inputs
CE\	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
WE\	- Write Enable
OE\	- Output Enable
NC	- No Connect

DESCRIPTION

The DS1245Y/AB 1024K Nonvolatile SRAM is a 1,048,576-bit, fully static, nonvolatile SRAM organized as 131,072 words by 8 bits. The DS1245Y/AB has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 128K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

READ MODE

The DS1245Y executes a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 17 address inputs (A_0-A_{16}) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1245Y is in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The nonvolatile static RAM provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal (V_{CC} greater than 4.75 V and write protect at 4.62 V nominal for DS1245AB). Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1245Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts (4.75 volts for the DS1235AB).

FRESHNESS SEAL

The DS1245Y is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is applied at a level of greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

BATTERY REDUNDANCY

Battery redundancy is provided to ensure reliability. The DS1245Y contains two lithium energy cells separated by an internal isolation switch. During battery back-up time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1245Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
DS1245AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 5% for DS1245AB)
(0°C to 70°C; V_{CC}=5V ± 10% for DS1245Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	*u* A	
I/O Leakage Current CE\ ≥V_{IH}≤V_{CC}	I_{IO}	-1.0		+1.0	*u* A	
Output Current @2.4V	I_{OH}	-1.0			mA	
Output Current @0.4V	I_{OL}	2.0			mA	
Standby Current CE\ = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current CE\ = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 120ns	I_{CC01}			85	mA	
Write Protection Voltage (DS1245Y)	V_{TP}	4.25	4.37	4.5	V	
Write Protection Voltage (DS1245AB)	V_{TP}	4.50	4.62	4.75	V	

CAPACITANCE

(t_A=25°C)

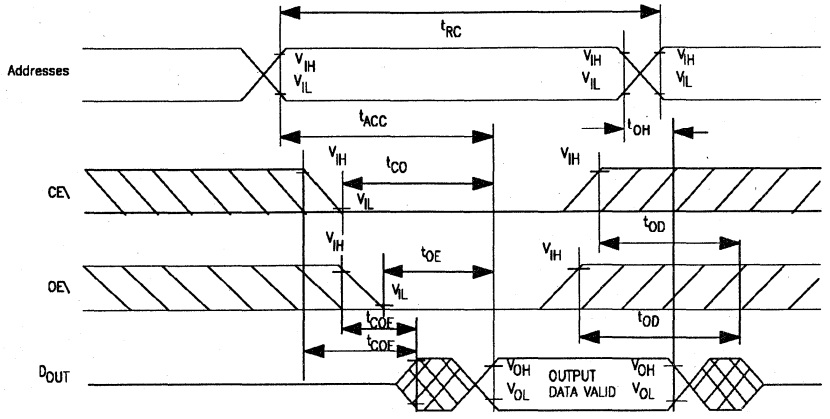
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

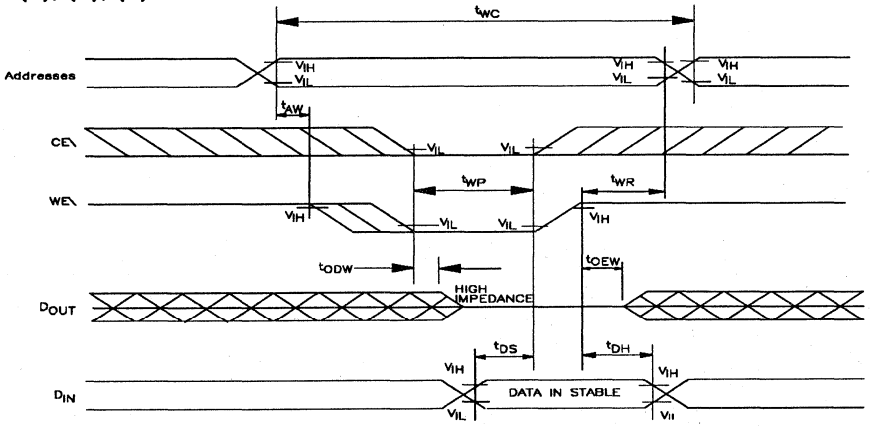
(0°C to 70°C; V_{CC}=5V ± 5% for DS1245AB)
(0°C to 70°C; V_{CC}=5V ± 10% for DS1245Y)

		DS1245Y/AB-100		DS1245Y/AB-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	100		120		ns	
Access Time	t_{ACC}		100		120	ns	
OE\ to Output Valid	t_{OE}		50		60	ns	
CE\ to Output Valid	t_{CO}		100		120	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		ns	5
Output High Z From De-selection	t_{OD}		35		40	ns	5
Output Hold From Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		120		ns	
Write Pulse Width	t_{WP}	75		90		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recov-ery Time	t_{WR}	20		20		ns	
Output High Z From WE\	t_{ODW}		35		40	ns	5
Output Active from WE\	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	40		50		ns	4
Data Hold Time From WE\	t_{DH}	20		20		ns	4

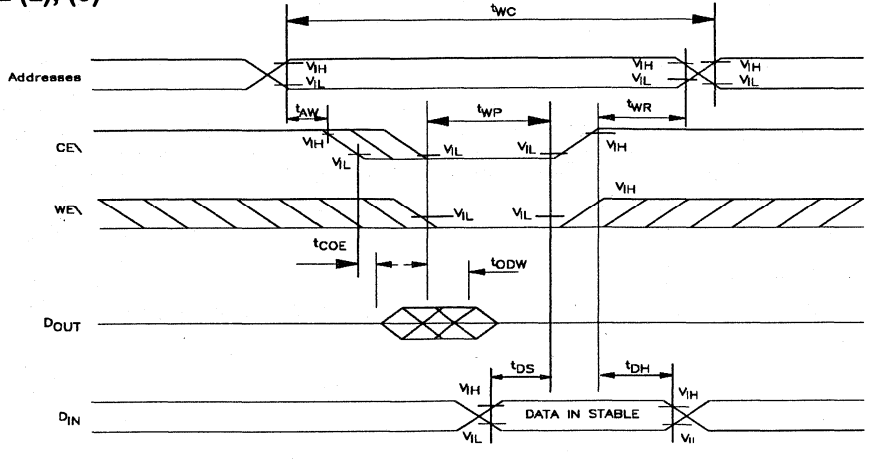
READ CYCLE (1)



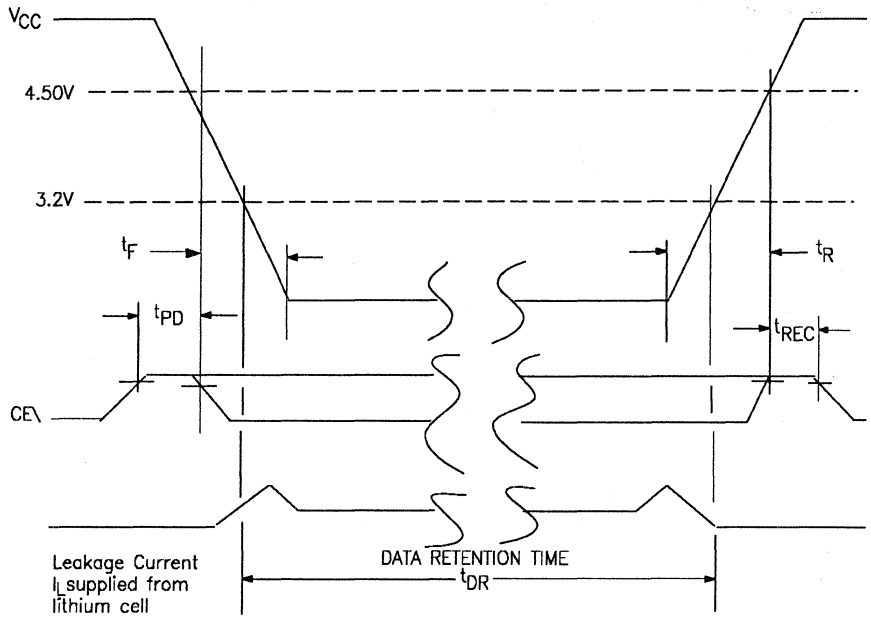
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		*u* s	
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	300		*u* s	
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	0		*u* s	
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. WE\ is high for a Read Cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impeddance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\.
   t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or latter from the WE\ low transition in a Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in high impedance state during this period.

9. Each DS1245Y has a built-in switch which disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

DC Test Conditions
Outputs Open
All Voltages Are Referenced to Ground

AC Test Conditions
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

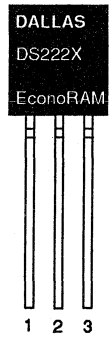
DALLAS SEMICONDUCTOR

DS222x
EconoRAM

FEATURES

- Low-cost general-purpose 256-bit memory
  - DS2223 has 256-bit SRAM
  - DS2224 has 32-bit ROM, 224-bit SRAM
- Reduces control, address and data interface to a single pin
- Each DS2224 32-bit ROM is factory-lasered with a unique serial number
- Minimal operating power: 36 nanocoulombs per transaction @1.5V
- Less than 1nA standby current at 25°C
- Nonvolatile data retention easily acheived via low-cost alkaline batteries or capacitors
- Directly connects to a port pin of popular micro-controllers
- Operation from 1.2 to 5.5 volts
- Popular TO-92 plastic transistor package

PACKAGE OUTLINE



BOTTOM VIEW

PIN CONNECTIONS

Pin 1	GND - Ground
Pin 2	DQ - Data In/Out
Pin 3	V_{CC} - Supply

ORDERING INFORMATION

DS2223	256-bit SRAM
DS2224	32-bit serial number (ROM), 224-bit SRAM

DESCRIPTION

The DS2223 and DS2224 EconoRAMs are fully static, micropowered, read/write memories packaged in a low-cost TO-92 package. The DS2223 is organized as a serial 256 x 1 bit static read/write memory. The DS2224's first 32 bits are lasered in with a unique ID code at the time of manufacture; the remaining 224 bits are static read/write memory. Signaling necessary for reading or writing is reduced to just one interface lead.

OPERATION

All communications to and from the EconoRAM are accomplished via a single interface lead. EconoRAM data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction. **Note that once a specific transaction has been initiated, either a read or a write, it must be completed for all memory locations before another transaction can be started.**

WRITE TIME SLOTS

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one-microsecond recovery time between individual write cycles.

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot. (See Figure 1.)

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot. (See Figure 2.)

READ TIME SLOTS

The host generates read time slots when data is to be read from the EconoRAM. A read time slot is initiated when the host pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the EconoRAM is then valid for the next 14 microseconds minimum. The host therefore must stop driving the DQ pin to read its state 1 to 15 microseconds from the start of the read slot (see Figure 3). At some point between 15 and 60 microseconds into the read time slot, the DQ pin will pull back high via the external pullup resistor (30 microseconds typically). All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

COMMAND WORD

The command word consists of 8 bits that are transmitted LSB first from the host to the EconoRAM with write time slots (see Figure 4). The first bit of the command word is set to a Logic 1 level. This indicates to the EconoRAM that a command word is being written. The next two bits are the select bits whic denote the physical address of the EconoRAM that is to be accessed (set to 00 currently). The remaining five bits determine whether a read or a write operation is to follow. If a write operation is to be performed, all five bits are set to a Logic 1 level. If a read operation is to be performed, any or all of these bits are set to a Logic 0 level. All eight bits of the command word are transmitted to the EconoRAM with a separate time slot for each bit.

READ OR WRITE TRANSACTION

Read or write transactions are performed by initializing the EconoRAM to a known state, issuing a command word, and then generating the time slots to either read EconoRAM contents or write new data. Each transaction consists of 264 transaction time slots. Eight are for the command word and 256 are for the data bits being transferred. (See Figure 5.) Once a transaction is started, it must be completed for all memory bits before another transaction can begin.

To initially set the EconoRAM into a known state, 264 Write Zero time slots must be sent to it. These Write Zero time slots will not corrupt the data in the EconoRAM since a command word has not been written. This operation will increment the address pointer internal to the EconoRAM to its maximum count value. Upon reach-

ing this maximum value, the EconoRAM will ignore all additional Write Zero time slots issued to it and the internal address pointer will remain locked at the top count value. This condition is removed by the reception of a Write One time slot, typically the first bit of a command word.

Once the EconoRAM has been set into a known state, the command word is transmitted to the EconoRAM with eight write time slots. This resets the address pointer internal to the EconoRAM and prepares it for the appropriate operation, either a read or a write.

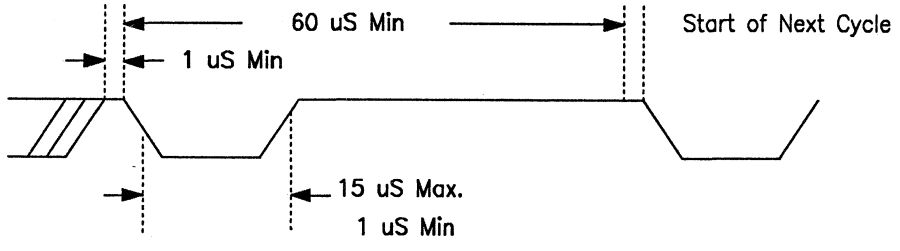
After the command word has been received by the EconoRAM, the host initiates the appropriate data transfer operation. In the case of a read transaction, the host issues 256 read time slots.

In the case of a write transaction, the host issues 256 write time slots. As stated previously, these time slots, either read or write, cannot be intermixed within the same transaction cycle.

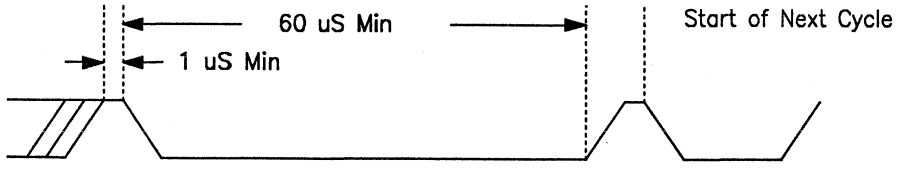
HOST SYSTEM INTERFACE

The host system must have an open drain driver with a pullup resistor of approximately 5K ohms to system V_{cc} on the data signal line. The EconoRAM has an internal open-drain driver with a 500K ohm pulldown resistor to ground (see Figure 8). **The open-drain driver allows the EconoRAM to be powered by a small standby energy source, such as a single 1.5 volt alkaline battery, and still have the ability to produce CMOS/TTL output levels.** The pulldown resistor holds the DQ pin at ground when the EconoRAM is not connected to the host.

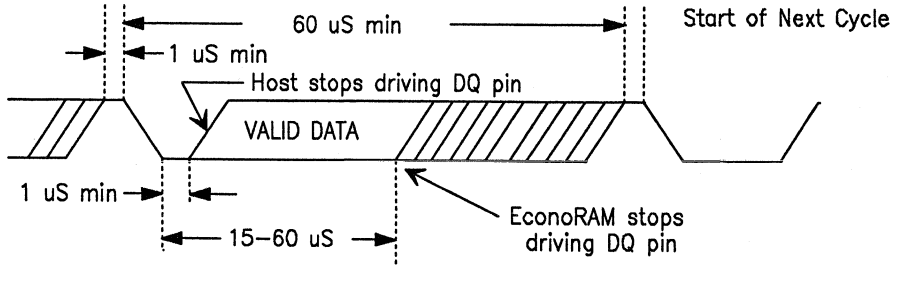
WRITE ONE TIME SLOT Figure 1



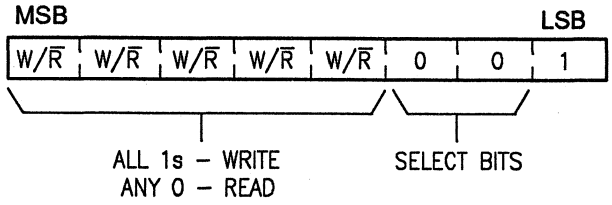
WRITE ZERO TIME SLOT Figure 2



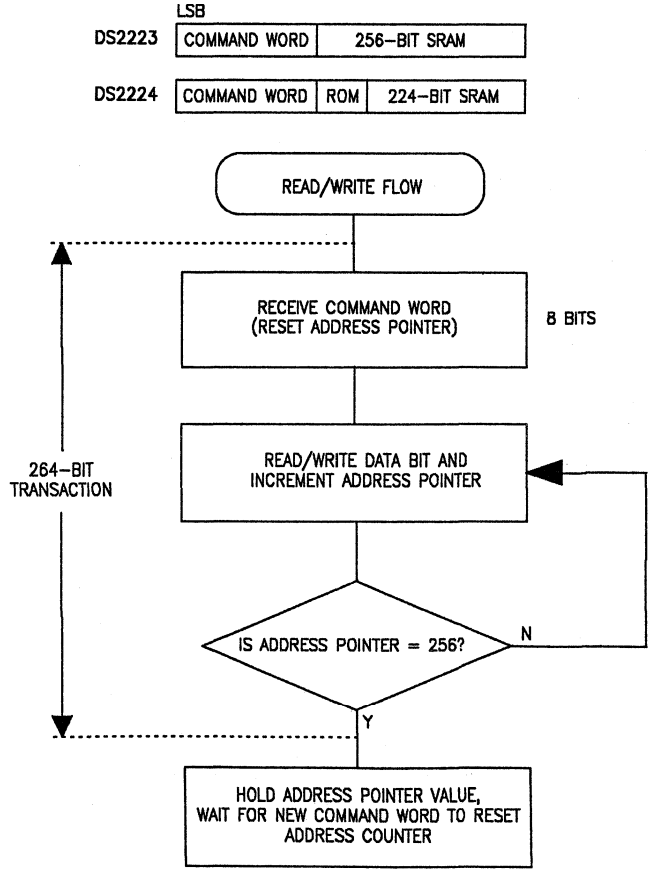
READ DATA TIME SLOTS Figure 3



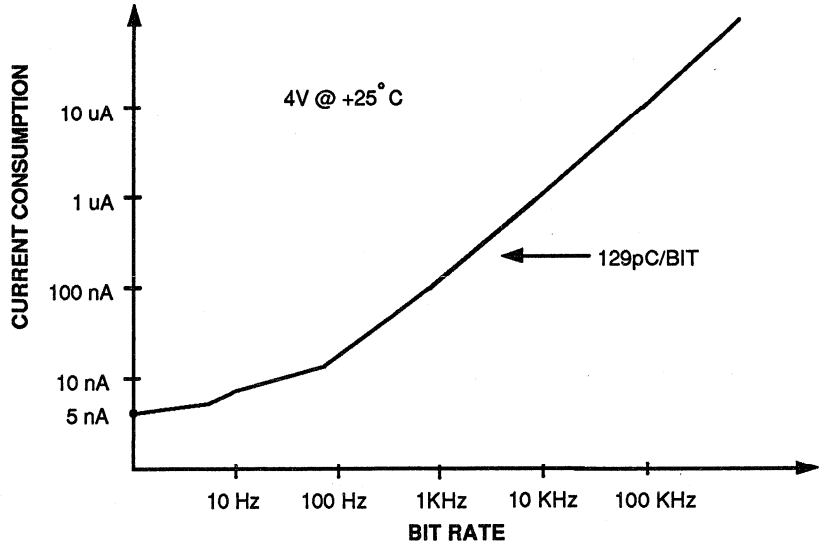
COMMAND WORD Figure 4



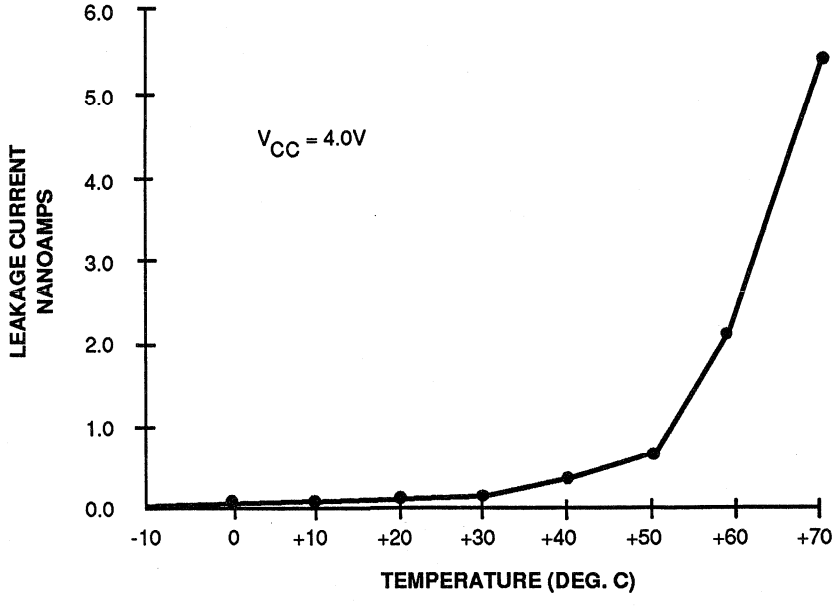
READ/WRITE TRANSACTION Figure 5



TYPICAL CURRENT CONSUMPTION VS. BIT RATE Figure 6



TYPICAL LEAKAGE CURRENT VS. TEMPERATURE Figure 7



ABSOLUTE MAXIMUM RATINGS

Voltage On Any Pin Relative to Ground	-0.5 to +6.5 Volts
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C

RECOMMENDED DC OPERATING CONDITIONS (DS2223/DS2224, 0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data Pin	DQ	-0.5		6.0	Volts	1
Supply Voltage	V_{CC}	1.2		5.5	Volts	1

DC ELECTRICAL CHARACTERISTICS (DS2223/DS2224 with V_{CC} = 2.0 - 5.5V, 0° to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5	0.4	0.8	Volts	1
Input Logic High	V_{IH}	V_{CC}-0.5		6.0	Volts	1
Sink Current	I_L	1	2		mA	4
Output Logic Low	V_{OL}			0.4	Volts	1
Output Logic High	V_{OH}	V_{PUP}			Volts	1,2
Input Resistance	I_R		500K		Ohms	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		0.2	15	nA	6

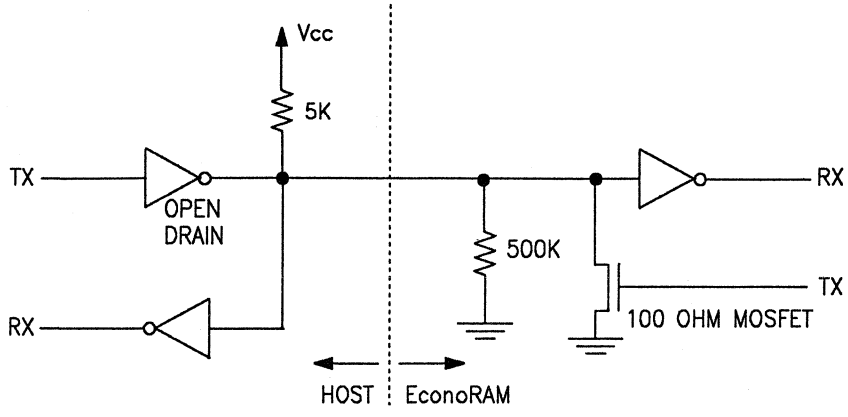
DC ELECTRICAL CHARACTERISTICS (DS2223/DS2224 with V_{CC} = 1.2V, 0° to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5		0.2	Volts	1
Input Logic High	V_{IH}	1.0		6.0	Volts	1
Sink Current	I_L	1	2		mA	7
Output Logic Low	V_{OL}			0.4	Volts	4
Output Logic High	V_{OH}	V_{PUP}			Volts	1,2
Input Resistance	I_R		500K		Ohms	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		0.2	15	nA	6

NOTES:

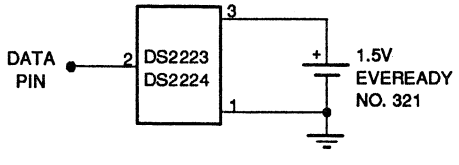
1. All voltages are referenced to ground.
2. V_{PUP} = external pullup voltage to system supply.
3. Input pulldown resistance to ground.
4. @ V_{OL} = 0.4V.
5. 36 nanocoulombs per 264 time slots @ 1.5V (see Figure 6).
6. See Figure 7 for typical values over temperature.
7. @ V_{OL}= 0.2 V.

HOST TO EconoRAM INTERFACE Figure 8

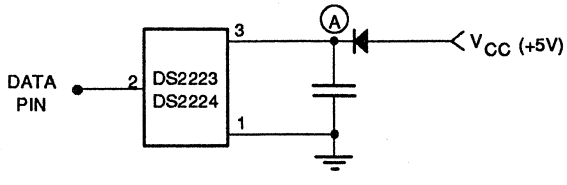


APPLICATION EXAMPLES

1. **Battery Backup Circuit**
   14mA-Hr => 144 million transactions



2. **Capacitor Backup Circuit**
   $A = V_{CC} - 0.7v$



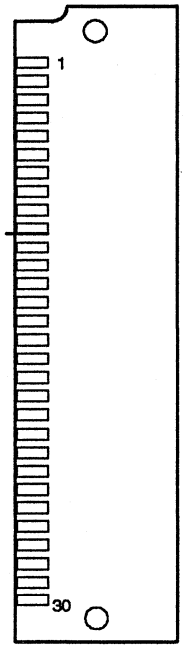
DALLAS SEMICONDUCTOR

DS2217
Nonvolatile SRAM Stik 128K x 9

FEATURES

- Data retention in the absence of V_{CC}
- Directly replaces volatile SRAM
- Employs popular JEDEC standard 30-position SIMM connection scheme
- Nonvolatile circuitry transparent to and independent from host system
- No additional components
- 10 years of data retention
- Organized as 128K bytes
- Available in 120ns, 150ns, and 200ns read access times
- Full ± 10% operating range
- Read cycle time equals write cycle time
- Unlimited write cycles
- Automatic write protection circuitry safeguards against data loss
- Wide operating temperature range of 0°C to 70°C

PIN DESCRIPTION



30-Pin SIP Stik

PIN NAMES (\ Denotes Condition Low)

V_{CC}	-+5 volt supply
GND	-Ground
A_0-A_{16}	-Address Inputs
DQ_0-DQ_7	-Data Input/Output
CE\	-Chip Enable
OE\	-Output Enable
WE\	-Write Enable

DESCRIPTION

The DS2217 Nonvolatile SRAM Stik 128K x 9 is a self-contained, 1,048,576-bit nonvolatile static RAM organized as 131,072 words by 8 bits. The nonvolatile memory contains all necessary control circuitry and energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2217 conforms to the popular 30-position SIMM pinout and requires no additional circuitry.

OPERATION

The DS2217 SRAM Stik is used like any standard static RAM. All the nonvolatile circuitry resides transparently to the user. Decoding from upper order address lines is also integrated into the nonvolatile controller and is transparent to SRAM operation. Connection to the DS2217 is made with an industry standard, 30-position SIMM socket (AMP part number 643930-1). These SIMM sockets are also available in double-row and low-profile angled variations.

READ MODE

The DS2217 is executing a read cycle whenever WE\ (write enable) is inactive (high) and CE\ (chip enable) is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that CE\ and OE\ (output enable) access times are satisfied. If OE\ and CE\ times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS2217 is in the write mode whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge. Write cycles can occur only when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The nonvolatile Stik provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2217 constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2217 checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2217, the battery is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. Therefore, the SRAM Stik provides battery redundancy. The DS2217 has an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground: -0.3V to +7.0V
Operating Temperature: 0°C to 70°C
Storage Temperature: -40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		V_{CC}	V
Input Low Voltage	V_{IL}	-0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-60		+60	uA
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}				uA
Output Current @ 2.4V	I_{OH}	-1.0	-2.0		mA
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA
Standby Current $\overline{CE}$=2.2V	I_{CC}		15	25	mA
Operating Current t_{CYC} = 250ns	I_{CC}		50	100	mA

DC TEST CONDTIONS

Outputs Open.
All Voltages are Referenced to Ground.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	50	pF	
Output Capacitance	C_{OUT}	50	pF	

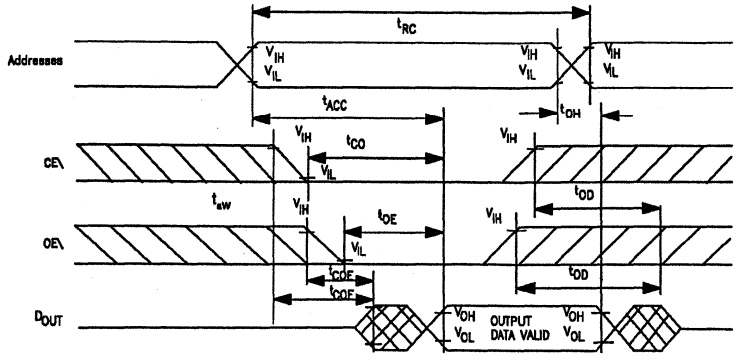
AC ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC}=5.0V ± 10%)

		DS2217-120		DS2217-150		DS2217-200			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	120		150		200		ns	
Access Time	t_{ACC}		120		150		200	ns	
CE\ to Output Valid	t_{OE}		60		70		100	ns	
OE\ to Output Valid	t_{CO}		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		ns	5
Output High Z from Deselection	t_{OD}		40		70		100	ns	
Output Hold from Address Change	t_{OH}	5		5		5		ns	5
Write Cycle Time	t_{WC}	120		150		200		ns	
Write Pulse Width	t_{WP}	90		100		150		ns	3
Address Setup Time	t_{aW}	0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		ns	
Output High Z from WE\	t_{ODW}		40		70		80	ns	5
Output Active from WE\	t_{OEW}	5		5		5		ns	5
Data Setup Time	t_{DS}	50		60		80		ns	4
Data Hold Time	t_{DH}	20		20		20		ns	4

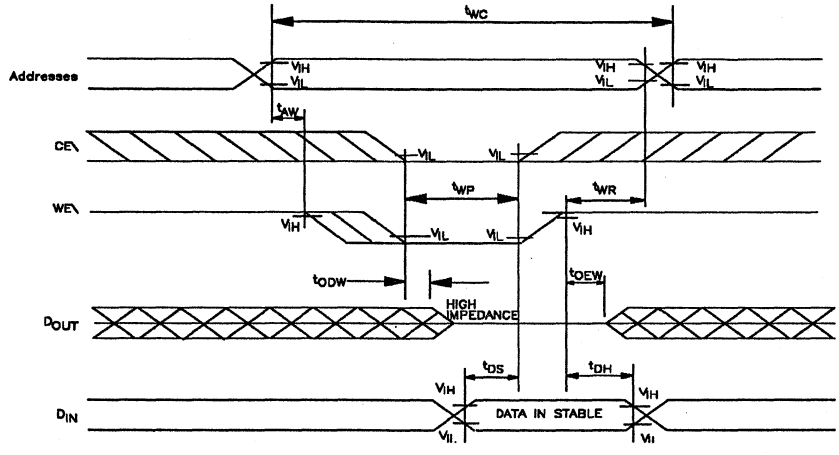
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0 V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

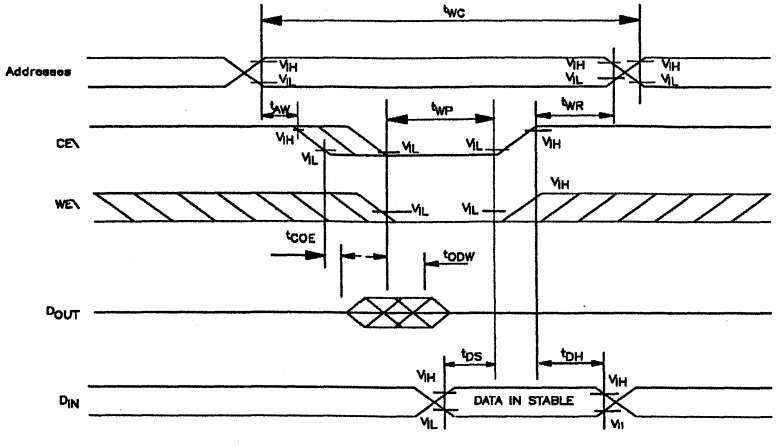
READ CYCLE(1)



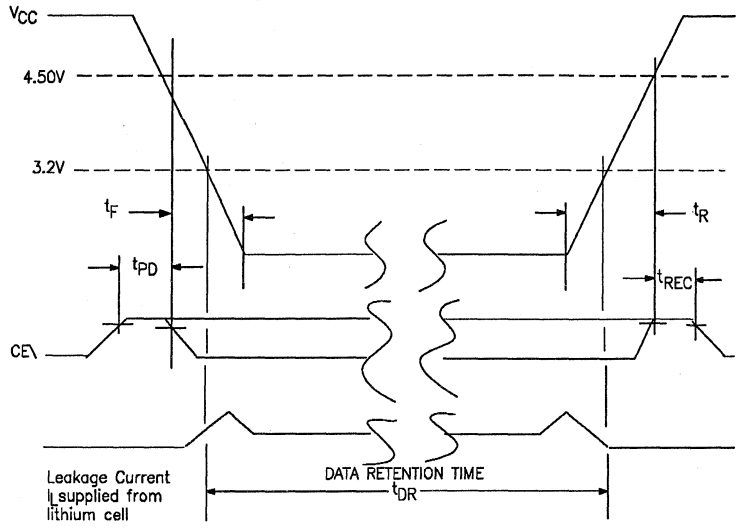
WRITE CYCLE 1(2),(6),(7)



WRITE CYCLE 2(2),(8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} slew from 4.5V to OV (CE\ at V_{IH})	100		us	
t_R	V_{CC} slew from OV to 4.5V (CE\ at V_{IH})	0		us	
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

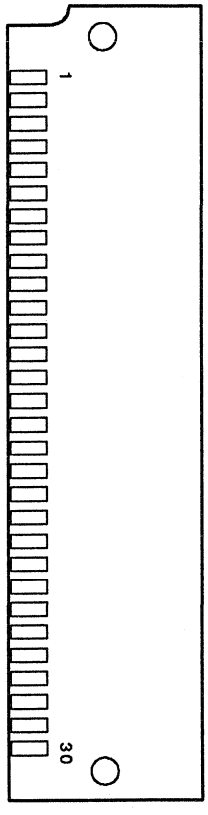
1. WE\ is high for a read cycle.
2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.
4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in a Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If the WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS2217 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

DALLAS SEMICONDUCTOR

DS2219
Nonvolatile DRAM Stik 1M x 9

FEATURES
- Maintains data in the absence of system power
- Compatible with existing DRAM SIMM applications
- Normal operating mode completely unaffected
- Nonvolatile circuitry transparent and independent from host system
- No additional components required
- Conforms to popular JEDEC standard 30-position SIMM DRAM module
- Accommodates any 6 volt to 10 volt primary energy cell or rechargeable energy source
- Memory array available as 1024K bytes with parity bit
- RAS\ access time of 120ns or 150ns
- Power-fail detection at 10% supply

PACKAGE DESCRIPTION



30-Pin SIP Stik

DESCRIPTION

The DS2219 Nonvolatile DRAM Stik 1M x 9 provides all necessary timing, refresh generation, and power-down/power-up sequencing necessary to maintain data integrity during system power failure. A primary or a rechargeable energy source can be used to support data retention. Available in 1,048,576 bytes, the memory module conforms to the standard 30-position SIMM pin configuration. The self-contained memory maintenance circuitry resides transparently to the host system, eliminating the need for any additional components. Normal 5 volt operation is completely unaffected as nonvolatile circuitry is transparent to DRAM.

OPERATION - NORMAL POWER CONDITIONS

Under normal 5 volt operating conditions, the DS2219 Nonvolatile DRAM Stik behaves exactly like a standard 1024K x 9 DRAM SIMM such as the Hitachi HB56A19B. The RAS\, CAS\, and WE\ inputs to the Stik are directed through the DS1237 directly to the individual DRAM circuits. The DS2219 will operate in this mode until the 5 volt supply at V_{CC} decays to 4.5 volts during loss of power. For detailed information on access timing, AC characteristics, and operating conditions for the Power Normal mode, please review the Hitachi HB56A19B DRAM Module data sheet.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5 volt V_{CC} power begins to drop, the DS1237 senses this change using a precision band gap comparator and isolates all control inputs to the Stik as V_{CC} falls below 4.5 volts. Power to the individual DRAM circuits is switched from the main 5 volt supply to a back-up supply connected at position 24 of the Stik. This backup supply is typically a chargeable capacitor or battery; however, any supply between 6 volts and 10 volts is suitable. Connection pins are provided for the back-up supply at other locations on the Stik PCB if location 24 is not convenient. All refreshing is accomplished internally within the Stik and is supported continuously until V_{CC}returns to normal levels and the system signals the Stik that it is ready to assume refresh duties.

OPERATION - RETURN TO NORMAL POWER CONDITIONS

When the system 5 volt supply returns and exceeds 4.5 volts, the system supply is reconnected to the DRAM circuits and the back-up supply is internally disconnected. At this time, a continuous CAS\ before RAS\ refresh is also generated internally at a cycle time of 350 ns maximum. Refreshing continues without interruption until the system signals the Stik that it is ready to assume refresh responsibility for the DRAMs. Refresh duties are shifted from the Stik to the system when a software-controlled switch is set by sending a specific pattern on address lines A5, A6, and A7 for 24 consecutive cycles. The address pattern which sets the software switch is shown in Figure 1. This address pattern is clocked into the DS1237 DRAM Nonvolatizer Chip resident on the Stik on the falling edge of CAS\ provided that set-up and hold times are met. When the 24th cycle is correctly entered, the system will have full access to RAM and must handle refresh requirements. RAM read and write cycles can then resume without restriction.

CONSERVATON OF BACKUP SUPPLY

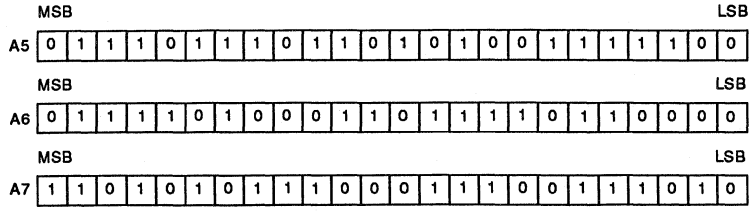
Another software-controlled switch allows conservation of the back-up supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. The bit patterns shown in Figure 2 turn on or off this switch which disconnects or connects the back-up supply.

BACK-UP CONDITION

The DS2219 contains two features which provide information about the condition of the back-up supply. The BC\ (Battery Condition) pin at location 19 of the Stik provides the output for the back-up supply information. If this feature is to be used, please review the "Back-up Condition" section of the DS1237 DRAM Nonvolatizer Chip data sheet.

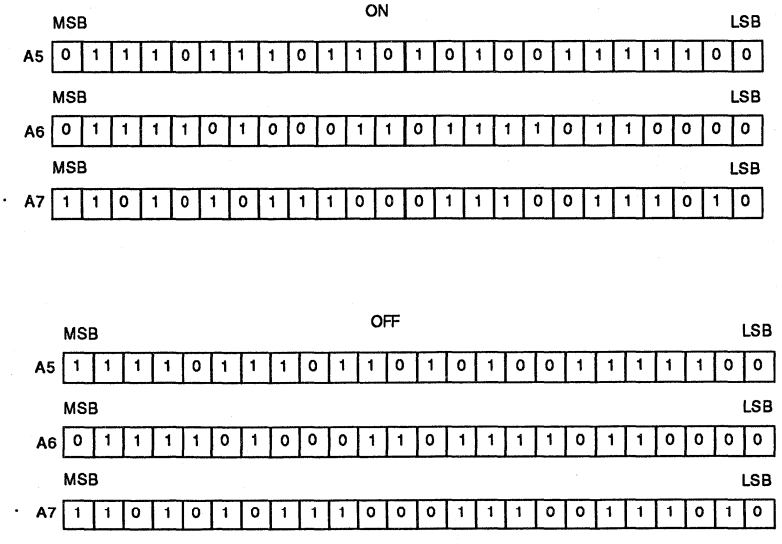
SOFTWARE SWITCH FOR PROCESSOR CONTROL POWER-UP

Figure 1



SOFTWARE CONTROLLED SWITCH FOR CONSERVATION OF BACK-UP SUPPLY

Figure 2



PIN DESCRIPTION Table 1 **(\Denotes Condition Low)**

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	V_{CC}	16	DQ4
2	CAS\	17	A8
3	DQ0	18	A9
4	A0	19	BC\
5	A1	20	DQ5
6	DQ1	21	WE\
7	A2	22	GND
8	A3	23	DQ6
9	GND	24	V_{BAT}
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	RAS\
13	DQ3	28	PCAS\
14	A6	29	V_{CC}
15	A7	30	PD

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Except Battery Inputs Relative to Ground	-0.3 to +7V
Voltage On the Battery Input Pins Relative to Ground	-0.3V to +12V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	VOLTS	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	VOLTS	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	VOLTS	1
Back-up Supply	BK_{UP}	6.0	8.0	10.0	VOLTS	2,3

DC ELECTRICAL CHARACTERISTICS (0°C to70°C V_{CC}=4.5 to 5.5 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			15	mA	4
Power-Fail Detect	V_{TP}	4.25	4.37	4.5	V	6
Input Leakage	I_{IL}	-1.0		1.0	uA	4

(0°C to 70°C,V_{CC} <V_{TP})

Data Retention Current	I_{DR}		7	15	mA	5

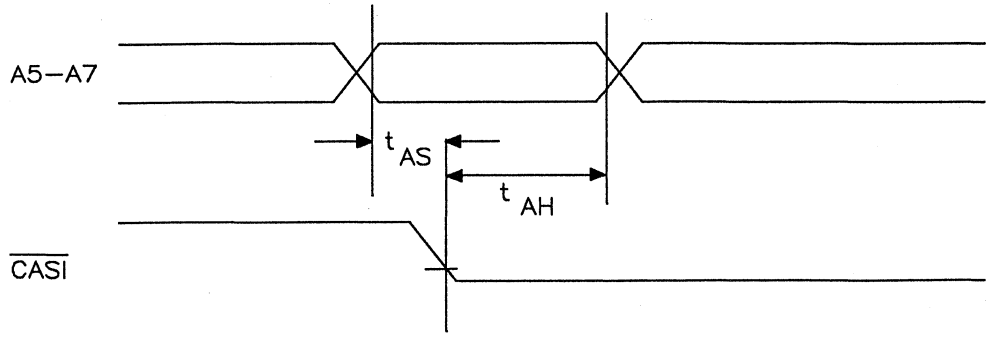
CAPACITANCE (t_A =25°)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input capacitance	C_{IN}		5	7	pF	4

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC}=4.5 to 5.5V)

Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	

SOFTWARE SEQUENCE ENTRY



NOTES:

1. All voltages are referenced to ground.
2. The BC\ pin will be driven active whenever V_{CC} is within nominal limits and the back-up supply is below V_{CC}.
3. Back-up input voltage is internally regulated within the DS2219 such that V_{CC} to the DRAMs is never below 4.5 volts, for a back-up input voltage of 6.0 volts minimum.
4. Additive to specification limit for the Hitachi HB56A19B Series DRAM SIMM.
5. This is the average current from the back-up supply to maintain memory for the Stik.
6. V_{TP} is the trip point where the internal switching circuit disconnects V_{CC} and connects the internally regulated back-up supply to the DRAMs. Rapid refresh is also initiated at this time.

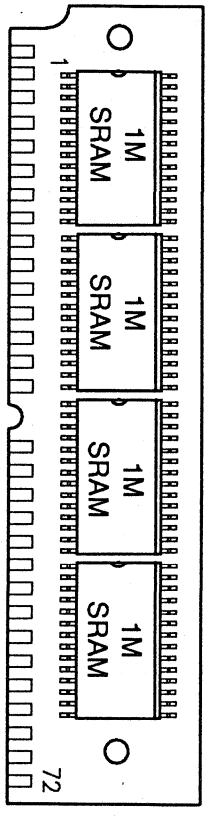
DALLAS SEMICONDUCTOR

DS2227
Flexible NV SRAM Stik™

FEATURES

- Flexibly organized as 128K x 32, 256K x 16, or 512K x 8 bits
- Data retention >10 years in the absence of V_{CC}
- Nonvolatile circuitry transparent to and independent from host system
- Automatic write protection circuitry safeguards against data loss
- Separate chip enables allow access by byte, word, or long word
- Fast access times: 55ns, 70ns, 100ns, or 120ns
- Unlimited write cycles
- Read cycle time equals write cycle time
- Employs popular JEDEC standard 72-position SIMM connection scheme
- Single 5-volt operating supply
- Full +/- 10% operating range
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

PIN DESCRIPTION



72-pin SIP Stik

DESCRIPTION

The DS2227 Flexible NV SRAM Stik™ is a self-contained 4,194,304-bit nonvolatile static RAM which can be flexibly organized as 128K x 32 bits, 256K x 16 bits, or 512K x 8 bits. The nonvolatile memory contains all necessary control circuitry and lithium energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2227 employs the popular JEDEC standard 72-position SIMM connection scheme requiring no additional circuitry.

OPERATION

The DS2227 Flexible NV SRAM Stik™ is used like any standard static RAM. All the nonvolatility circuitry resides transparently to the user. The flexibility of the part is achieved by providing separate read, write, and chip select pins for each of the four banks of onboard memories (see Figure 1). For operation as a 512K x 8 NV SRAM Stik, tie all data lines from each bank together (i.e., all D0s together, all D1s together, etc.). Read enables and write enables are also tied together. For operation as a 256K x 16 NV SRAM Stik, tie the data lines from two banks together. Chip enables, read enables, and write enables from these banks are also tied together. Connection to the DS2227 is made by using an industry-standard, 72-position SIMM socket (AMP part number 821824-3). These SIMM sockets are also available in perpendicular, inclined, or parallel mount, depending on the height available.

READ MODE

The DS2227 executes a read cycle whenever WE\ is inactive (high) and CE\ is active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that CE\ and OE\ access times are also satisfied. If OE\ and CE\ times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS2227 is in the write mode whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cyle. WE\ must return to the high state for a minimum recovery time (t_{WR}) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs to t_{ODW} from its falling edge. Write cycles can occur only when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The DS2227 provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2227 constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2227 checks lithium status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2227 the lithium is checked with a precision comparator. If the lithium supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications data integrity is paramount. The DS2227 provides lithium cell redundancy and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the lithium with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A lithium status warning will occur only if both lithium cell batteries are less than 2.0 volts.

PIN DESCRIPTION Table 1

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	Vcc Power	38	4-D0
2	1-D0	39	4-D1
3	1-D1	40	4-D2
4	1-D2	41	4-D3
5	1-D3	42	4-D4
6	1-D4	43	4-D5
7	1-D5	44	4-D6
8	1-D6	45	4-D7
9	1-D7	46	NC
10	NC	47	4-Chip Enable
11	1-Chip Enable	48	4-Output Enable
12	1-Output Enable	49	4-Write Enable
13	1-Write Enable	50	Ground
14	2-D0	51	Vcc Power
15	2-D1	52	A0
16	2-D2	53	A1
17	2-D3	54	A2
18	2-D4	55	A3
19	2-D5	56	A4
20	2-D6	57	A5
21	2-D7	58	A6
22	NC	59	A7
23	2-Chip Enable	60	A8
24	2-Output Enable	61	A9
25	2-Write Enable	62	A10
26	3-D0	63	A11
27	3-D1	64	A12
28	3-D2	65	A13
29	3-D3	66	A14
30	3-D4	67	A15
31	3-D5	68	A16
32	3-D6	69	NC
33	3-D7	70	Stik Serial Number
34	NC	71	NC
35	3-Chip Enable	72	Ground
36	3-Output Enable		
37	3-Write Enable		

NOTE: Leave all pins marked as NC unconnected.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40° to +85°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-1.0		+1.0	uA
I/O Leakage Current	I_{LO}	-5.0		+5.0	uA
Output Current @ 2.4V	I_{OH}	-1.0			mA
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA
Operating Current	I_{CC}		60	280	mA

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}		20	40	pF
Output Capacitance	C_{OUT}		5	10	pF

POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CE\ at V_{IH} Before Power-down	t_{PD}	0			us
V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	t_F	300			us
V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	t_R	0			us
CE\ at V_{IH} after Power-up	t_{REC}	2	80	125	ms

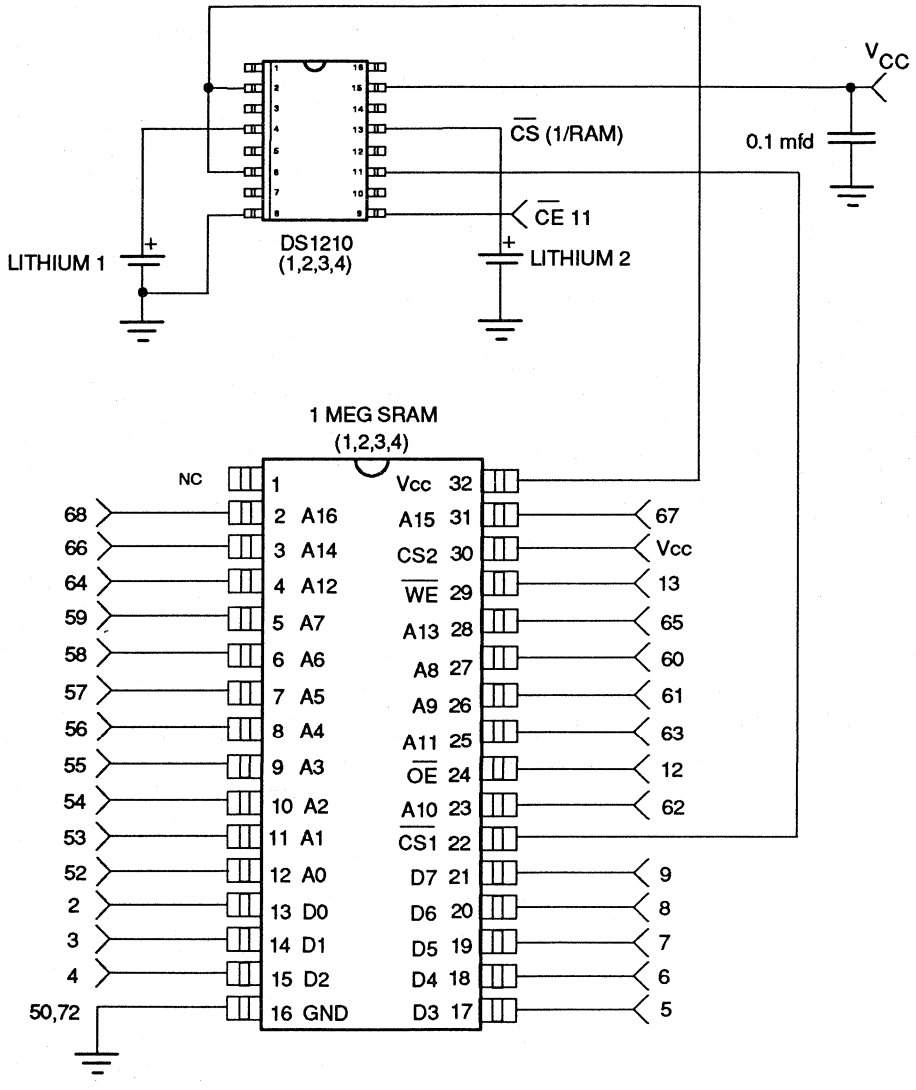
(t_A = 25°)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Expected Data Retention Time	t_{DR}	10			Years

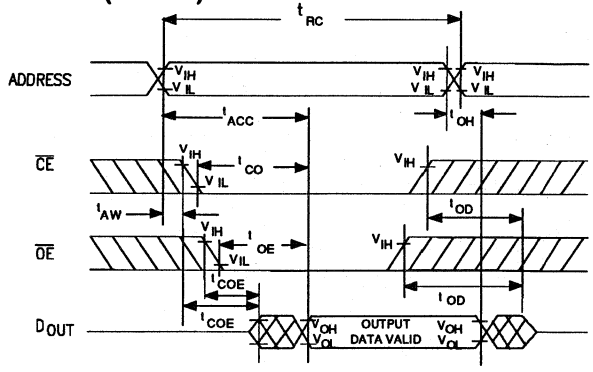
AC ELECTRICAL CHARACTERISTICS

		DS2227-55		DS2227-70		DS2227-100		DS2227-120		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**NOTE**
Read Cycle Time	t_{RC}	55ns		70ns		100ns		120ns		10
Access Time	t_{ACC}		55ns		70ns		100ns		120ns	10
OE\ to Output Valid	t_{OE}		30ns		35ns		50ns		60ns	10
CE\ to Output Valid	t_{CO}		55ns		70ns		100ns		120ns	10
OE\ or CE\ to Output Active	t_{COE}	5ns		5ns		5ns		5ns		10
Output High Z from Deselection	t_{OD}		20ns		25ns		35ns		40ns	10
Output Hold from Address Change	t_{OH}	5ns		5ns		5ns		5ns		10
Write Cycle Time	t_{WC}	55ns		70ns		100ns		120ns		10
Write Pulse Width	t_{WP}	45ns		55ns		75ns		90ns		3,10
Address Setup Time	t_{AW}	0ns		0ns		0ns		0ns		10
Write Recovery Time	t_{WR}	20ns		20ns		20ns		20ns		10
Output High Z from WE	t_{ODW}		20ns		25ns		35ns		40ns	10
Output Active from WE\	t_{OEW}	5ns		5ns		5ns		5ns		8,10
Data Setup Time	t_{DS}	25ns		30ns		40ns		50ns		4,10
Data Hold Time from WE\	t_{DH}	20ns		20ns		20ns		20ns		4,5 10

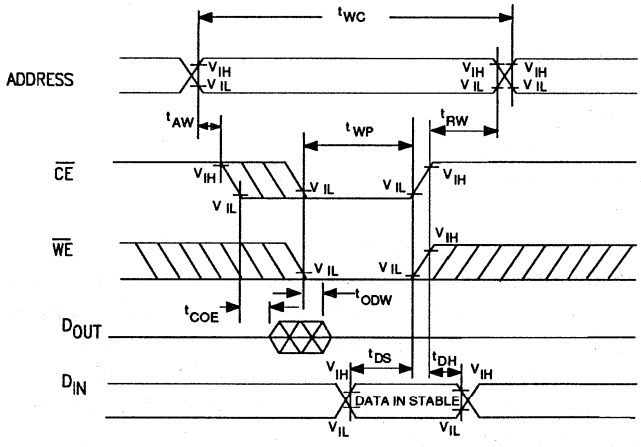
SCHEMATIC (1 CELL) Figure 1



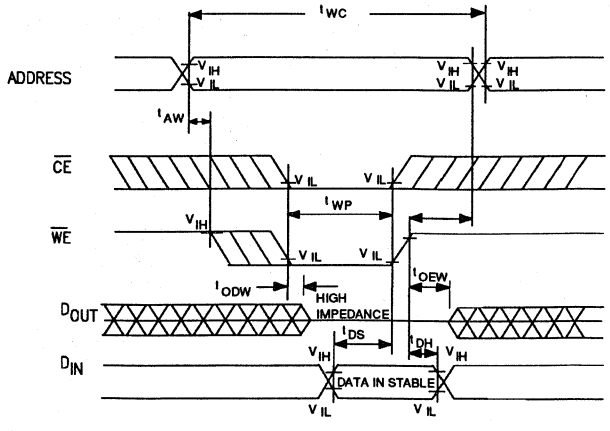
READ CYCLE (Note 1)



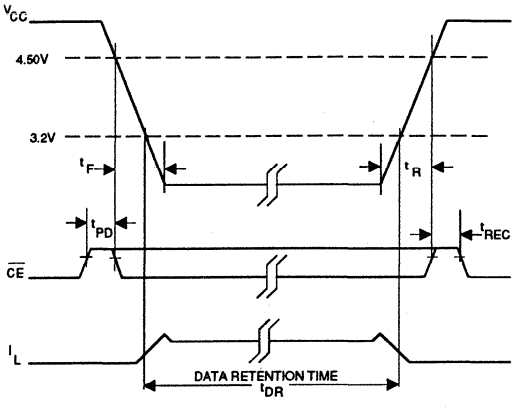
WRITE CYCLE 1 (Note 2, 6, 7)



WRITE CYCLE 2 (Note 2, 8)



POWER-UP/POWER-DOWN CONDITION



Leakage current
I_L supplied from lithium cell

NOTES:

1. WE\ is high for a read cycle.
2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE\ and WE\.
4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.
5. t_{DH} is measured from WE\ going high. If CE\ is used to terminate the write cycle then t_{DH} = 20 ns.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in write cycle 1, the output buffers remain in a high impedance state in this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in write cycle 1, the output buffers remain in a high impedance state in this period.
8. If the WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS2227 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The minimum expected t_{DR} is defined as starting at the date of manufacture.
10. Timings are valid only when CE\ is tied low.

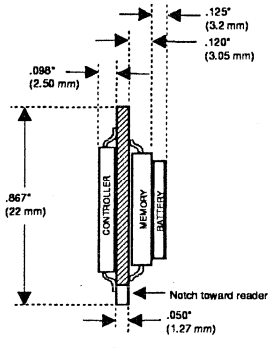
DC TEST CONDITIONS

Outputs Open
t cycle = 250 ns
All voltages are referenced to ground

AC TEST CONDITIONS

Output load: 100 pF + 1TTL gate
Input pulse levels: 0 - 3.0 V
Timing Measurements Reference levels:
Input - 1.5V
Output - 1.5V
Input Pulse Rise and Fall Times: 5ns

MECHANICAL SPECIFICATIONS (SIDE VIEW)



See 72-pin SIP Stik for other dimensions.

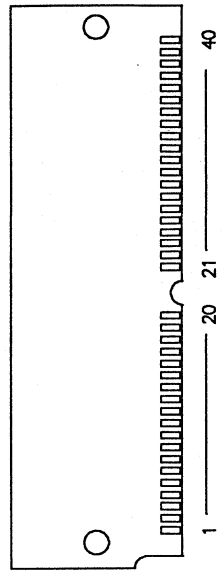
DALLAS SEMICONDUCTOR

DS2230
Dual Port NV SRAM Stik

FEATURES

- Provides 64 Kbytes of dual port nonvolatile SRAM
- NV SRAM accessible via JEDEC bytewide port and 3-wire serial port
- Provides arbitration mechanisms for dual port operation
- Permanently powered clock/calendar option keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Clock/calendar access is transparent to RAM operation
- Cyclic redundancy check monitors serial data transmission for error
- 40-pin SIMM connection scheme

PIN DESCRIPTION



40-Pin SIP Stik

DESCRIPTION

The DS2230 is a self-contained, 524,288-bit dual port nonvolatile static RAM organized as 65,536 words by 8 bits. Standard bytewide CMOS SRAMs are converted into nonvolatile storage by an onboard DS1221 Nonvolatile Controller x 4 Chip and an onboard lithium source. The nonvolatile memory contains all necessary control circuitry and energy sources to maintain data integrity in the absence of power for more than 10 years.

The NV SRAM is accessible from a processor's data bus via a JEDEC standard bytewide interface that incorporates 19 address lines, 8 data lines, a chip enable (CE\), output enable (OE\), and write enable (WE\). In addition, the memory is accessible via a 3-wire serial bus interface to a second processor. As a result, the two processors can share data within the RAM area. The DS1280 3-Wire to Bytewide Converter Chip provides the arbitration between the serial and bytewide ports.

The DS2230T version incorporates a DS1214 Time Chip as a permanently powered real time clock calendar. The Time Chip keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years.

The Dual Port NV SRAM Stik plugs into the industry-standard SIMM connector scheme that supports redundant contacts, simple insertion/ extraction, and low overall height profiles.

Throughout this document, when features are discussed that are common to both the time and non-time versions of the DS2230, both versions are generically referred to as the DS2230(T). When features are discussed which are specific to either the time or the non-time version, each version will be represented with its true designation, DS2230 and DS2230T, respectively.

PIN ASSIGNMENTS

Table 1 lists the pin assignment of the DS2230(T) 40-position SIP connector. Table 2 is a description of the pins.

DS2230(T) PIN ASSIGNMENT Table 1

1 - GND	21 - A1
2 - DQ	22 - A2
3 - V_{CC}	23 - A3
4 - OE\	24 - A4
5 - WE\	25 - A5
6 - CE\	26 - A6
7 - DQE	27 - A7
8 - CLK	28 - A8
9 - RST\	29 - A9
10 - D7	30 - A10
11 - D6	31 - A11
12 - D5	32 - A12
13 - D4	33 - A13
14 - D3	34 - A14
15 - D2	35 - A15
16 - D1	36 - A16
17 - D0	37 - A17
18 - NC	38 - A18
19 - GND	39 - NC
20 - A0	40 - GND

(\ Denotes Condition Low)

DS2230(T) PIN DESCRIPTION Table 2

NAME	DESCRIPTION
V_{CC}	+5V Power Supply input
GND	Ground
A18-A0	Address Bus inputs
D7-D0	Data Bus; bidirectional
CE\	Chip Enable input; active low
OE\	Output Enable input; active low
WE\	Write Enable input; active low
RST\	Reset for serial port; input; active low
DQ	Data Input/Output for serial port; bidirectional
CLK	Clock for serial port; input
DQE	Serial port active output

ARBITRATION

The DS1280 3-Wire to Bytewide Converter Chip provides the arbitration scheme between the 3-wire serial port and the bytewide parallel port. The 3-wire serial port has priority in accessing the RAM. Furthermore, the methods used to avoid collisions are primarily directed via the serial port. Arbitration can be accomplished by handshaking between the processors or by using a predictable idle time as an access window. The designer should consult the DS1280 data sheet for detailed information on arbitration operation between the bytewide and serial ports.

BYTEWIDE PORT ACCESS

If the RST\ signal for the 3-wire serial port is low (serial port disabled), the bytewide parallel port can access the RAM directly. In this mode the DS2230(T) is used like any standard static RAM. All the nonvolatile circuitry is transparent to the user.

READ MODE

The DS2230(T) will execute a read cycle whenever WE\ (write enable) is inactive (high) and CE\ (chip enable) is active low. The unique address specified by the 19 address inputs (A_0-A_{18}) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that CE\ and OE\ (output enable) access times are also satisfied. If OE\ and CE\ times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS2230(T) will execute a write cycle whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge. Write cycles can occur only when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION

The Dual Port NV SRAM Stik provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} at less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2230(T) constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2230(T) checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2230(T) the battery is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

SERIAL PORT ACCESS

If the RST\ signal for the 3-wire serial port is high (serial port enabled), the DS1280 uses the 3-wire port for communication with the RAM and disregards accesses performed on the bytewide port. The DS1280 uses a 56-bit protocol written serially using RST\, DQ, and CLK to determine the action required and also the starting location in the RAM to be used. Both single-byte transfers as well as burst read and writes to the RAM are supported. Cyclic Redundancy Check (CRC) circuitry can be enabled to monitor serial data transmission for error. The designer should consult the DS1280 data sheet for complete operational information and electrical specification information on RAM access via the serial port.

TIME CHIP

The DS2230T version incorporates a DS1214 Time Chip as a permanently powered real time clock calendar. The DS1214 is identical to the DS1215 Phantom Time Chip with one exception: it has no on-chip comparator circuitry for lithium backup. Instead, it is backed up by the onboard DS1221 Nonvolatile Controller x 4 Chip. Because the DS1214 is tied to the DS1221's CE0\ line, the clock is accessed by addressing the lower 32K byte memory (00000H - 07FFFH). The DS1214 is accessed using a protocol that is identical to that of the DS1215. Consult the DS1215 data sheet for a complete functional description of the read/write protocol to the Time Chip.

CONNECTOR

Connection to the DS2230(T) is made by using an industry standard, 40-position SIMM socket. AMP Inc. manufactures two sockets that will accept the DS2230(T): vertical mount (AMP part # 821918-2) or right angle mount (AMP part #4-382480-0). These connectors are also available from Dallas Semiconductor. The Dallas part numbers are DS9072-40V for the vertical mount version and DS9072-40R for the right angle mount version.

ORDERING INFORMATION

The following version of the DS2230 is available as a standard product from Dallas Semiconductor:

PART #	TIME-KEEPER	RAM	ACCESS TIME
DS2230T 64	Yes	64K x 8	200 ns

Please contact Dallas Semiconductor for ordering information on other configurations of the DS2230.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3 to +7.0V
Operating Temperature	0° to +70°C
Storage Temperature	-40°C to +85°C

*This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A = 0°C to 70°C)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3 V		1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	uA	2
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	+2.0			mA	
Standby Current	I_{STBY}		15	25	mA	3
Supply Current	I_{CC}		75	100	mA	4

CAPACITANCE

(t_A = 25° C)

PARAMETER	SYM.	TYP.	MAX.	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Output Capacitance	C_{OUT}	7	15	pF	

DC TEST CONDITIONS

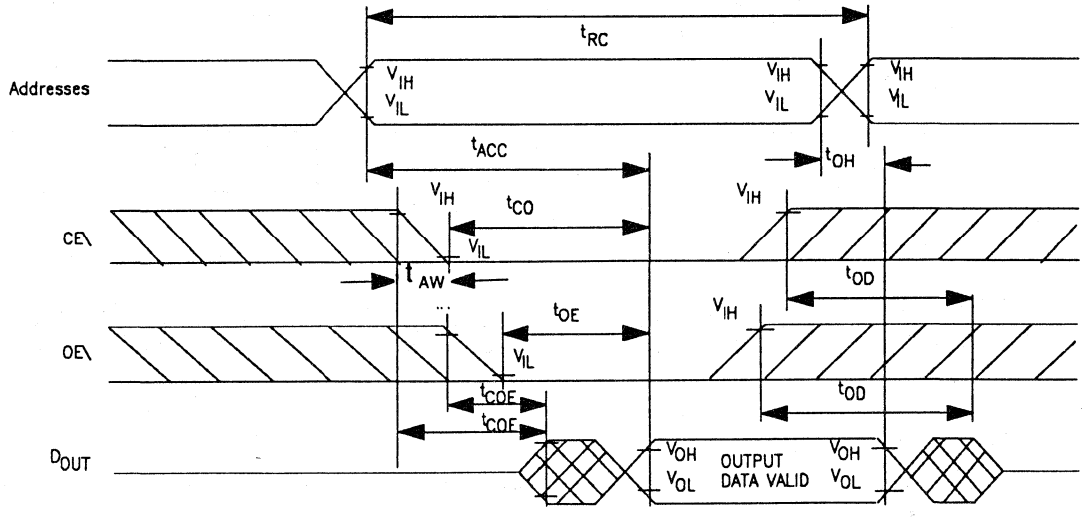
Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

AC ELECTRICAL CHARACTERISTICS

(0^{o} TO 70^{o}C; V_{CC} = 5V ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	200			ns	
Access Time	t_{ACC}			200	ns	
OE\ to Output Valid	t_{OE}			100	ns	
CE\ to Output Valid	t_{CO}			200	ns	
OE\ or CE\ to Output Active	t_{COE}	10			ns	
Output High Z from Deselection	t_{OD}			100	ns	
Output Hold From Address Change	t_{OH}	10			ns	
Write Cycle Time	t_{WC}	200			ns	
Write Pulse Width	t_{WP}	170			ns	7
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}			10	ns	
Output High Z from WE\	t_{ODW}			80	ns	
Output Active from WE\	t_{OEW}	10			ns	12
Data Setup Time	t_{DS}	80			ns	8
Data Hold Time	t_{DH}	0			ns	8, 9

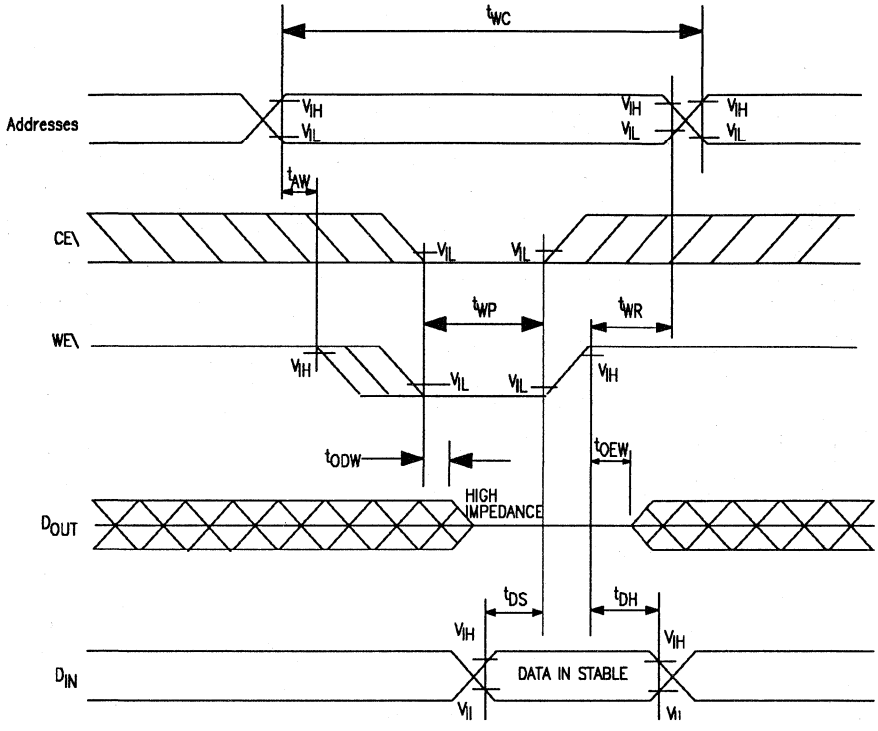
READ CYCLE (Note 5)



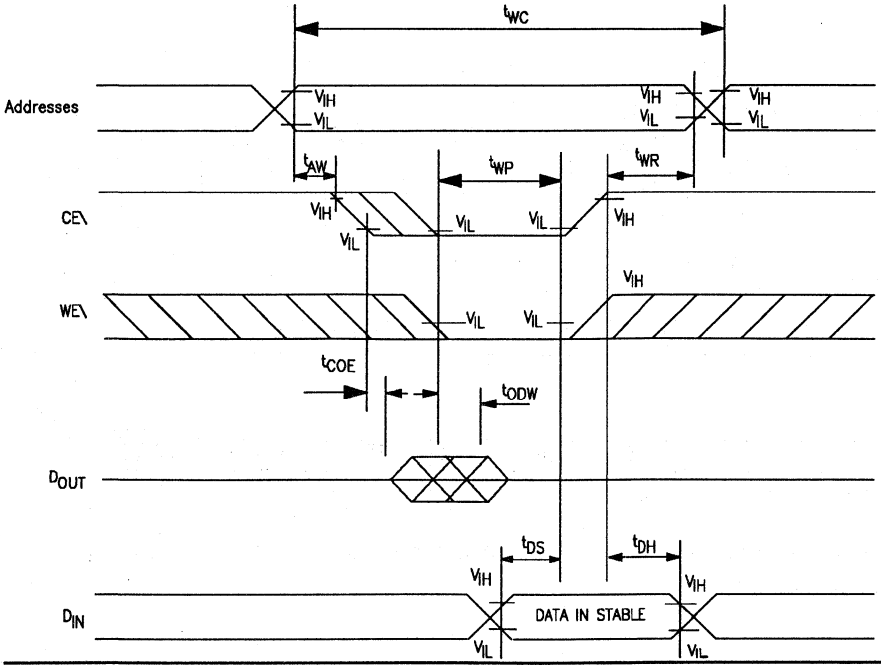
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

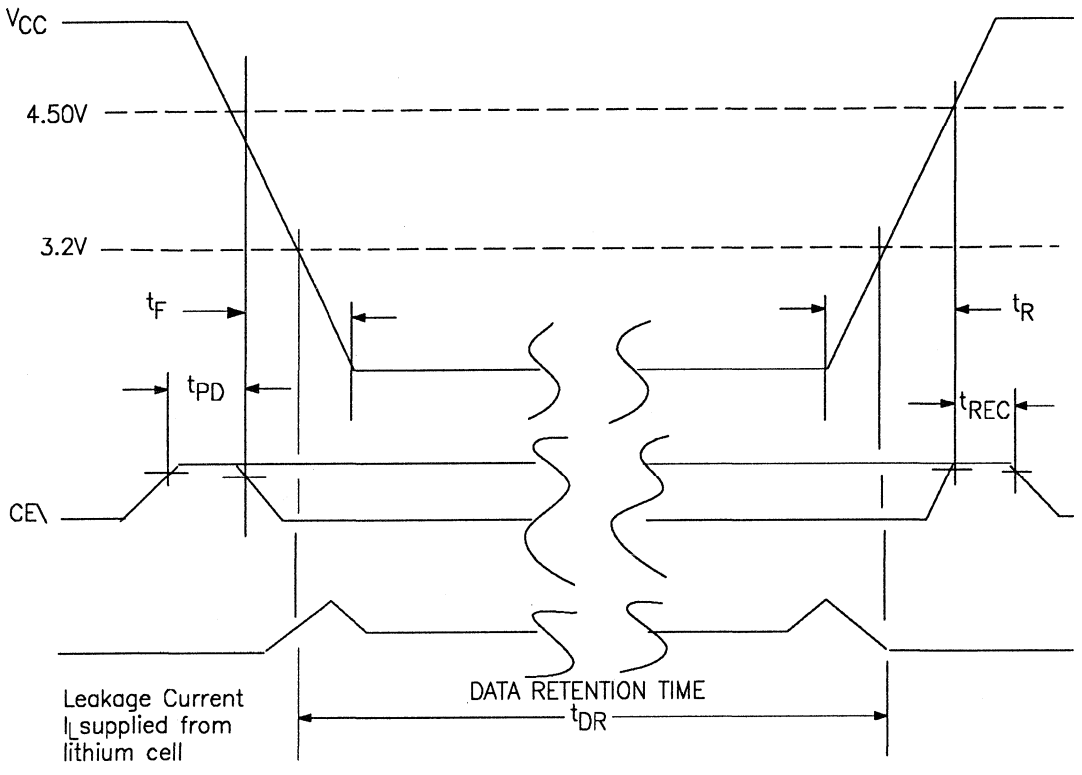
WRITE CYCLE 1 (Notes 6, 10, 11)



WRITE CYCLE 2 (Notes 6, 12)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
CE\ at V_{IH} before Powe- Down	t_{PD}	0			us	
V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	t_F	100			us	
V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	t_R	100			us	
CE\ at V_{IH} after Power-Up	t_{REC}	2		125	ms	

(t_A= 25°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	13

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in lithium backup mode.

AC ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C; V_{CC} = 5V ± 10%)

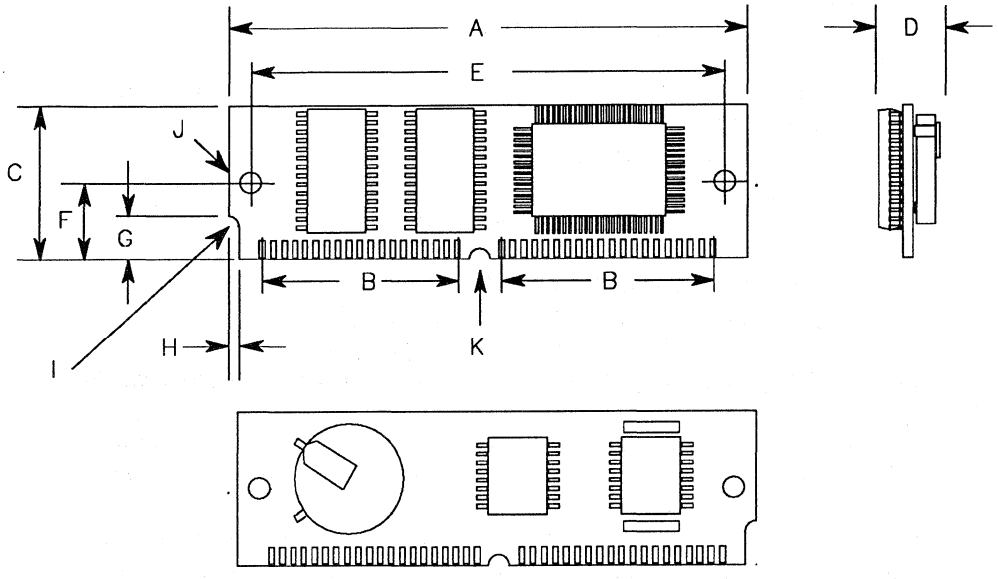
SERIAL PORT ACCESS

The AC electrical characteristics pertaining to access of the RAM via the 3-wire serial port are given in the DS1280 data sheet.

NOTES:

1. All voltages are referenced to ground.
2. Pins A0 thru A18, RST\, DQ, and CE\ have pull-down resistors on-chip that will leak approximately 50uA.
3. I_{STBY} is measured with CE\ = 2.2V, all outputs open, and both the 3-wire serial port and the bytewide port inactive.
4. I_{CC} is measured with all outputs open.
5. WE\ is high for a read cycle.
6. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
7. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.
8. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.
9. t_{DH} is measured from WE\ going high. If CE\ is used to terminate the write cycle the t_{DH} = 20 ns.
10. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
11. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
12. If the WE\ is low, or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.
13. Each DS2230(T) is marked with a 4-digit data code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

DS2230(T)
Dual Port NV SRAM Stik



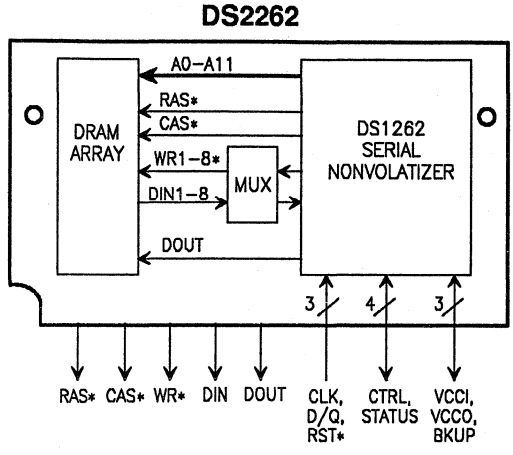
DIM.	INCHES	MM
A	2.650	67.31
B	0.950	24.13
C	0.850	21.59
D	0.350	8.89
E	2.384	60.55
F	0.400	10.16
G	0.250	6.35
H	0.080	2.03
I	R .062	R 1.57
J	D 0.125	D 3.18
K	R .062	R 1.57

DALLAS SEMICONDUCTOR

DS2262
MegaStore Stik™

FEATURES
- Solid-state mass storage subsystem using nonvolatile DRAM
- Versions with 4, 8, 16 and 32 megabits available
- DRAM timing and refresh control performed transparently to host
- Nonvolatile data retention using an external 6-9 volt backup supply
- Low-power data retention mode consumes less than 3 mA (4 megabit version)
- Backup supply can be switched off under host software control for conserving energy
- 3-wire serial port can access DRAM data at up to 1 Mbit/sec in burst mode
- Unique backup supply gas gauge continuously reports battery condition
- Power fail detect write-protects memory at either 5% or 10% of +5 volt main supply
- Mates with JEDEC-standard 30-pin SIMM edge connectors (right angle and vertical)

FUNCTIONAL DIAGRAM (*Denotes Condition Low)



DESCRIPTION

The DS2262 MegaStore Stik is an extremely compact solid-state mass storage device that provides up to 32 megabits of nonvolatile DRAM for data storage. The DRAM and internal control functions are accessed using a 3-wire serial interface (CLK, D/Q, RST*) which can hook directly to the serial port of popular microprocessor/microcontroller devices such as the DS5000T/2250T Time Microcontroller family. All necessary DRAM timing and refresh duties are performed automatically.

An external backup supply such as a 6-volt battery can be attached to enable DRAM data retention, creating in effect a solid-state disk drive. An internal circuit monitors the main +5V supply. Upon its failure, the DRAM is write-protected and the backup supply switched on. With an inexpensive1300 mA/Hr lithium battery, a DS2262 with 4 megabits can provide up to 3 weeks of continuous nonvolatile operation. If the failure of the main supply is relatively infrequent, the DS2262 can extend its nonvolatile operation for years, especially if the backup source is a rechargeable battery. A unique gas gauge circuit continuously monitors and reports the backup supply condition, warning the host of impending battery failure.

Intelligent Sockets

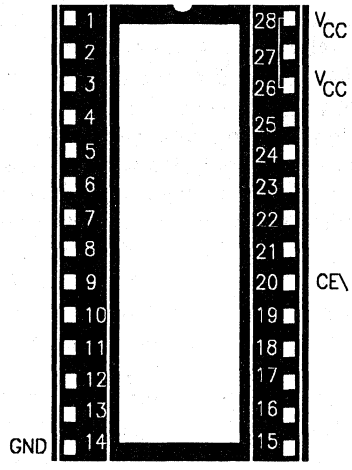
DALLAS SEMICONDUCTOR

DS1213B
SmartSocket 16/64K

FEATURES

- Accepts standard 2K x 8 and 8K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 2K x 8 to 8K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70° C

PIN DESCRIPTION



28-Pin Intelligent Socket

PIN NAMES (\ Denotes Condition Low)

All pins pass through except 20, 26, 28.

Pin 20	CE\	-Conditioned Chip Enable
Pin 26	V_{cc}	-Switched V_{cc} for 24-pin RAM
Pin 28	V_{cc}	-Switched V_{cc} for 28-pin RAM
Pin 14	GND	-Ground

DESCRIPTION

The DS1213B Smart Socket 16/64K is a 28-pin, 0.6 inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either 28-pin 8K x 8 or 24-pin 2K x 8 lower-justified JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{cc} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of the SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only pins 28, 26, 20, and 14 for RAM control. All other pins are passed straight through to the socket receptacle.

OPERATION

The DS1213B SmartSocket performs five circuit functions required to battery back-up a CMOS memory. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function is power-fail detection. Power-fail detection occurs between 4.75 and 4.5 volts. The DS1213B constantly monitors the V_{CC} supply. When V_{CC} falls below 4.75 volts, a precision comparator detects the condition and inhibits the RAM chip enable. The third function accomplishes write protection by holding the chip enable signal to the memory to within 0.2 volts of V_{CC} or battery supply. If the chip enable signal is active at the time power fail detection occurs, write protection is delayed until after the memory cycle is complete to avoid corruption of data. During nominal power supply conditions the memory chip enable signal will be passed through to the socket receptacle with a maximum propagation delay of 20 ns. The fourth function the DS1213B performs is to check battery status to warn of potential data loss. Each time that V_{CC} power is restored to the SmartSocket the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in the memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memory are questionable. The fifth function the SmartSocket provides is battery redundancy. In many applications, data integrity is paramount. In these applications it is desirable to use two batteries to ensure reliability. The DS1213B SmartSocket provides an internal isolation switch which provides for the connection of two batteries. During battery back-up the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. Each of the two lithium cells contains 35 mA/hr capacity, making the total 70 mA/hr.

NOTE: As shipped from Dallas Semiconductor, the lithium energy cell cannot be measured from the V_{CC} pin. In order to read the cell potential, apply V_{CC} and then remove power. The cell potential will then be available on pins 26, 28, and 20.

ABSOLUTE MAXIMUM RATINGS*

Voltage in Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec

*This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°c)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1,3
Logic 1 PIN 20 L	V_{IH}	2.2		V_{CC} + 0.3	V	1,3
Logic 0 PIN 20 L	V_{IL}	-0.3		+ 0.8	V	1,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26 L, PIN 28 L Supply Current	I_{CC}			5	mA	3, 4, 5
PIN 26 U, PIN 28 U Supply Voltage	V_{CCO}	V_{CC} -0.2			V	3, 8
PIN 26 U, PIN 28 U Supply Current	I_{CCO}			80	mA	3,8
PIN 20 L CE\ Input Leakage	I_{IL}	-1.0		+1.0	uA	3, 4
PIN 20 U CE\ Output @ 2.4 V	I_{OH}	-1.0			mA	2, 3
PIN 20 U CE\ Output @ .4V	I_{OL}			4.0	mA	2, 3

(0°C to 70°C, V_{cc} < 4.5V)

PIN 20 U Output	V_{OHL}	V_{CC} -0.2 V_{BAT}-0.2			V	3
PIN 26 U, PIN 28U Battery Current	I_{BAT}			1	uA	3,6
PIN 26 U, PIN 28 U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance PIN 20 L	C_{IN}	5	pF	3
Output Capacitance PIN 20 U	C_{OUT}	7	pF	3

AC ELECTRICAL CHARACTERISTICS

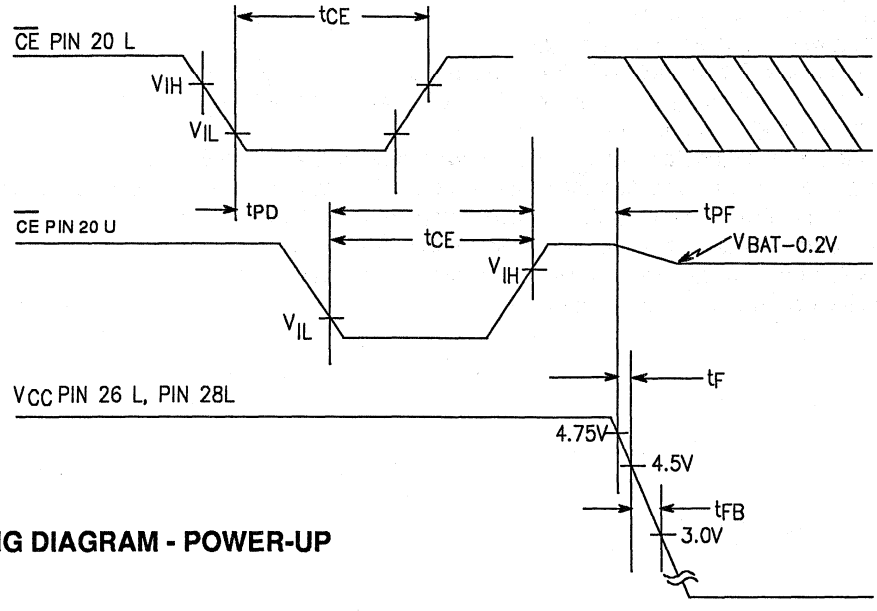
(0°C to 70°C, V_{CC}=4.75 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2,9
CE\ High to Power-Fail	t_{PF}			0	ns	

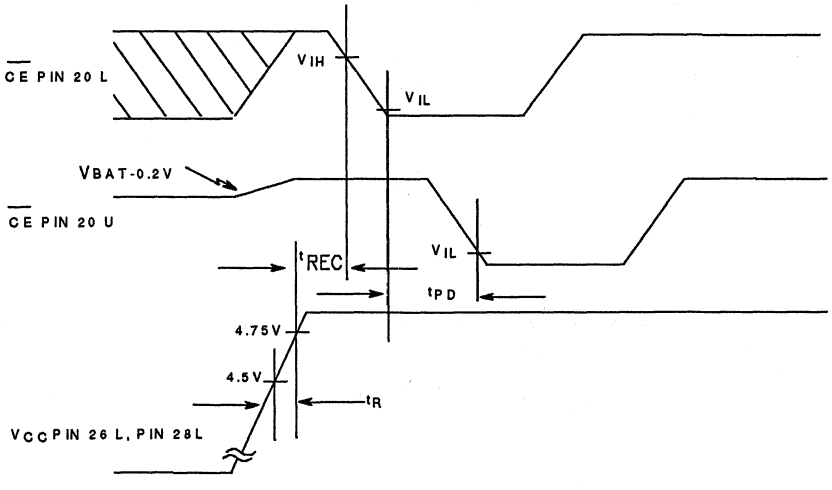
(0° to 70°C, V_{CCI} < 4.75 V)

Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate 4.75 - 4.5 V	t_F	300			us	
V_{CC} Slew Rate 4.5-3 V	t_{FB}	10			us	
V_{CC} Slew Rate 4.5 - 4.75 V	t_R	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7

TIMING DIAGRAM - POWER-DOWN



TIMING DIAGRAM - POWER-UP



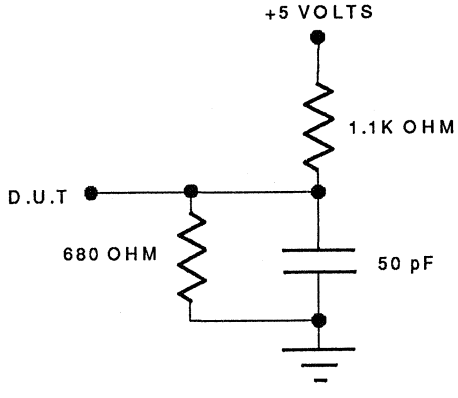
WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES:
1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26 L may be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum load current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. T_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.

OUTPUT LOAD Figure 1



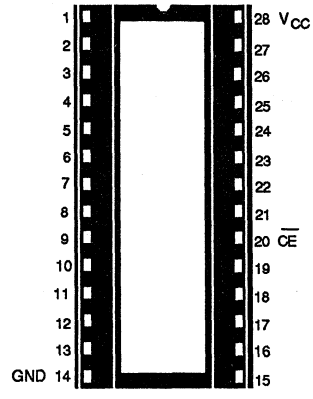
DALLAS SEMICONDUCTOR

DS1213C
SmartSocket 64/256K

FEATURES

- Accepts standard 8K x 8 and 32K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 8K x 8 to 32K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN DESCRIPTION



28-Pin Intelligent Socket

PIN DEFINITIONS

All pins pass thorugh except 20, 28.
Pin 20 Conditioned Chip Enable
Pin 28 Switched V_{CC}
Pin 14 Ground

DESCRIPTION

The DS1213C SmartSocket is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board space since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 28 and 20 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213B SmartSocket 16/64K data sheet for technical details.

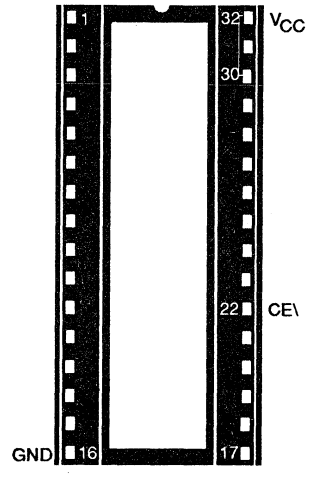
DALLAS SEMICONDUCTOR

DS1213D
SmartSocket 64/256K/1M

FEATURES

- Accepts standard 8K x 8, 32K x 8, 128K x 8, and 512K x 8 CMOS static RAMs
- Embedded lithium energy cell retains RAM data
- Self-contained circuitry safeguards data
- Data retention time is greater than 10 years with the proper RAM selection
- IC socket permits upgrading from 128K x 8 to 512K x 8 RAM
- Proven gas-tight socket contacts
- Operating temperature range 0°C to 70°C

PIN DESCRIPTION



32-Pin Socket (600 mil)

PIN NAMES (\ Denotes Condition Low)

All pins pass through except 22, 30 and 32.

Pin 22 CE\	- Conditioned Chip Enable
Pin 32 V_{CC}	- Switched V_{CC} for 32-pin RAM
Pin 30 V_{CC}	- Switched V_{CC} for 28-pin RAM
Pin 16 GND	- Ground

DESCRIPTION

The DS1213D SmartSocket is a 32-pin, 0.6-inch-wide DIP socket with a built-in CMOS controller circuit and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8 or 512K x 8 byte wide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility. The SmartSocket monitors incoming V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium source is automatically switched on and write protection is unconditionally enabled to prevent garbled data.

Using the SmartSocket saves printed circuit board spacing since the combination of SmartSocket and memory uses no more area than the memory alone. The SmartSocket uses only Pins 22, 30 and 32 for RAM control. All other pins are passed straight through to the socket receptacle.

See the DS1213B SmartSocket 16/64K data sheet for technical details.

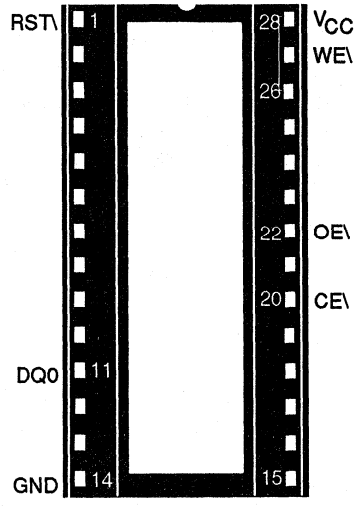
DALLAS SEMICONDUCTOR

DS1216B
SmartWatch/RAM 16/64K

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 2K x 8 and 8K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ± 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 min./month @25°C

PIN DESCRIPTION



28-Pin Intelligent Socket

PIN NAMES (\ Denotes Condition Low)
All Pins Pass Through Except 20, 26, 28
Pin 20 CE\ = Conditioned Chip Enable
Pin 26 V_{CC} = Switched V_{CC} for 24 Pin RAM
Pin 28 V_{CC} = Switched V_{CC} for 28 Pin RAM
Pin 1 RST\ = Reset
Pin 22 OE\ = Output Enable
Pin 27 WE\ = Write Enable
Pin 11 DQ0 = Data Input/Output 0
Pin 14 GND = Ground

DESCRIPTION

The DS1216B SmartWatch/RAM 16/64K is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either 24-pin 2K x 8 or 28-pin 8K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated RAM take up no more area than the memory alone. The SmartWatch uses pins 28, 27, 26, 22, 20, 11, and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

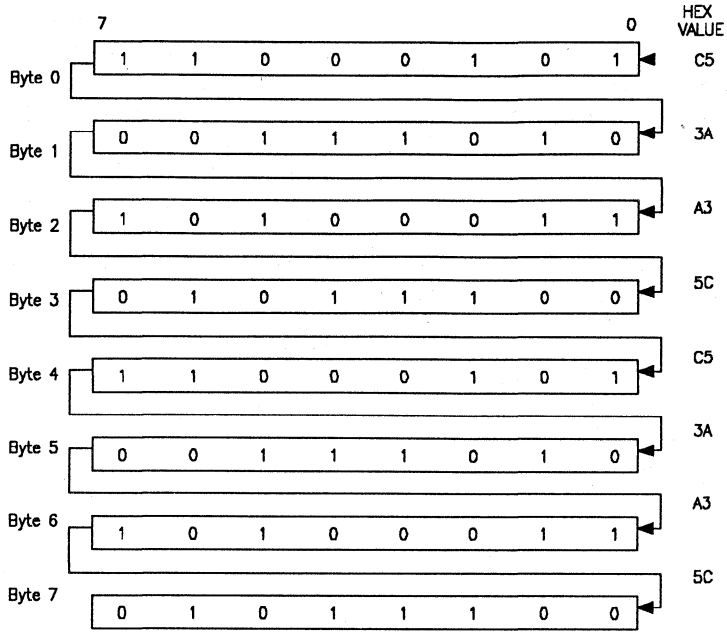
OPERATION

Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the SmartWatch, and memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of Chip Enable (CE\), Output Enable (OE\), and Write Enable (WE\). Initially, a read cycle to any memory location using the CE\ and OE\ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the CE\ and WE\ control of the SmartWatch. These 64 write cycles are used only to gain access to the SmartWatch. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the OE\ pin or the WE\ pin. Cycles to other locations outside the memory block can be interleaved with CE\ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}. This pattern is sent to the SmartWatch LSB to MSB.

NONVOLATILE CONTROLLER OPERATION

The DS1216B SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which the SmartWatch provides is power-fail detection. Power-fail detection occurs at typically 4.25 volts. The DS1216B constantly monitors the V_{CC} supply. When V_{CC} goes out of tolerance, a comparator outputs a power-fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of V_{CC} or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

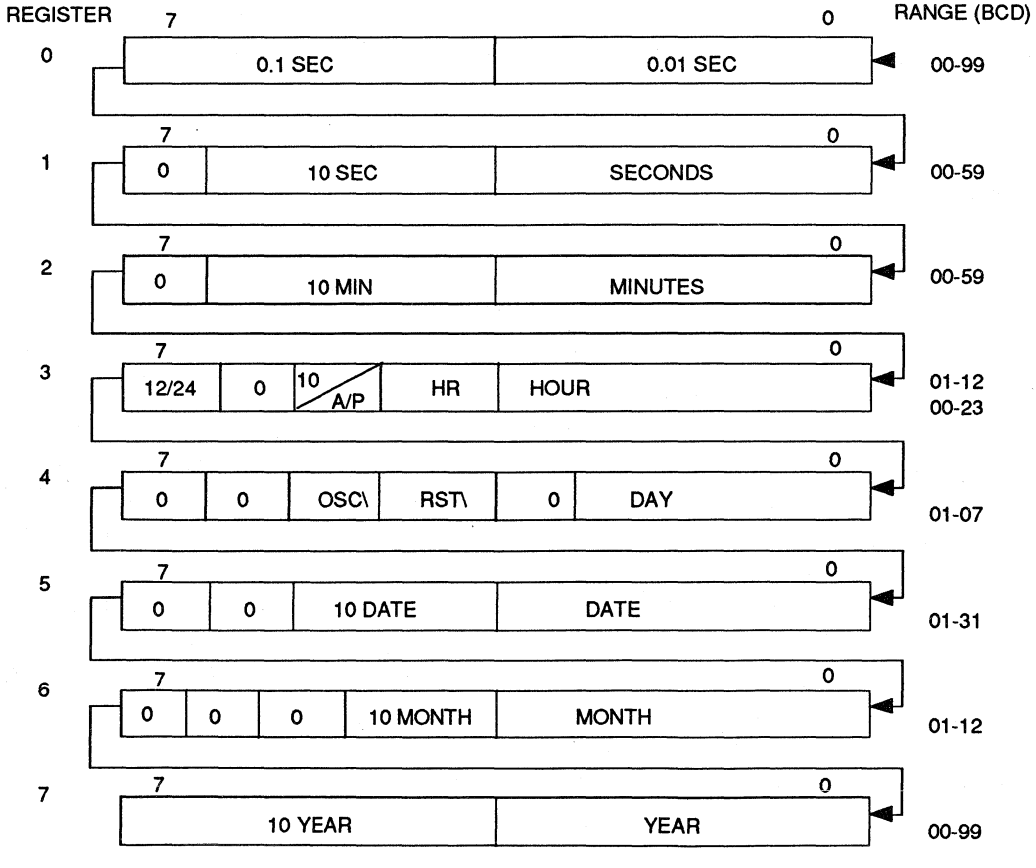
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the RESET\ and oscillator functions. Bit 4 controls the RESET\ (pin 1). When the RESET\ bit is set to logic 1, the RESET\ input pin is ignored. When the RESET\ bit is set to logic 0, a low input on the RESET\ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS *

Voltage on Any Pin Relative to Ground	-1.0V + 7V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 Sec

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, PIN 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1, 10

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC}=4.5 to 5.5V)

PIN 26L, PIN 28L Supply	I_{CCI}			5	mA	3,4,5
PIN 26U, PIN 28U Supply Voltage	V_{CCO}	V_{CC}-0.2			V	3, 8
PIN 26U, PIN 28U Supply Current	I_{CCO}			80	mA	3,8
Input Leakage	I_{IL}	-1.0		+1.0	uA	4,10,13
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°, V_{CC} <4.5V)

PIN 20U Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	3
PIN 26U, PIN 28U Battery Current	I_{BAT}			1	uA	3,6
PIN 26U, PIN 28U Battery Voltage	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

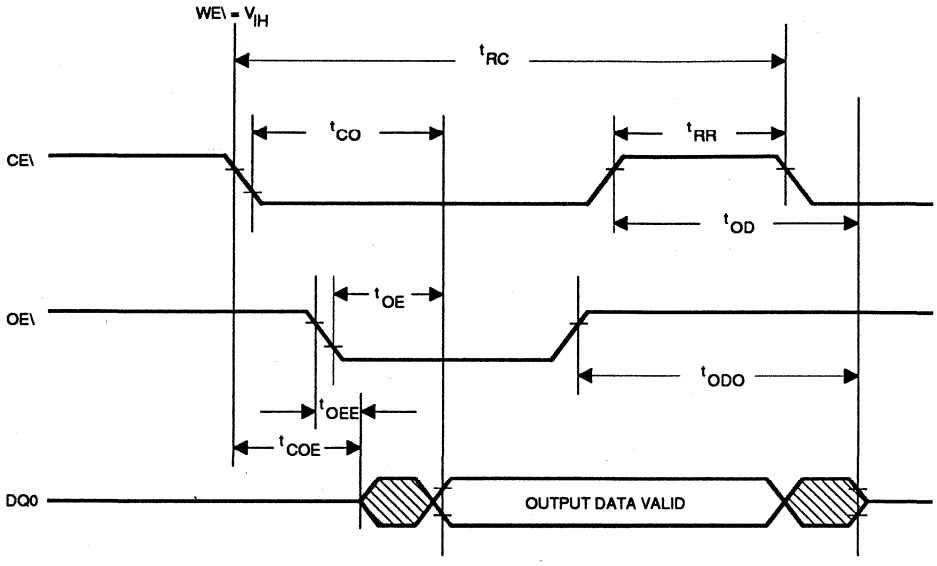
(0°C to 70°C, V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
OE\ Access Time	t_{OE}			100	ns	
CE\ To Output Low Z	t_{COE}	10			ns	
OE\ To Output Low Z	t_{OEE}	10			ns	
CE\ To Output High Z	t_{OD}			100	ns	
OE\ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	11
Data Setup Time	t_{DS}	100			ns	12
Data Hold Time	t_{DH}	0			ns	12
CE\ Pulse Width	t_{CW}	170			ns	
RESET\ Pulse Width	t_{RST}	200			ns	
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2, 9
CE\ High to Power-Fail	t_{PF}			0	ns	

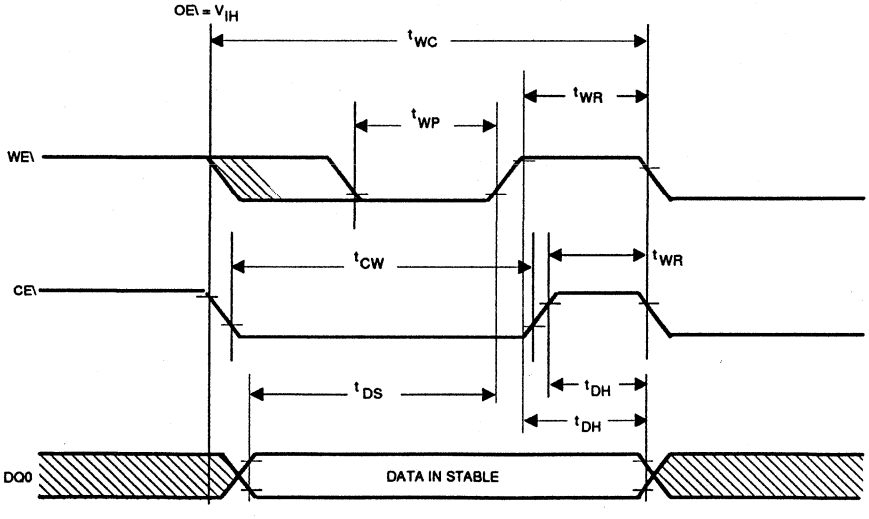
(0°C to 70°C, V_{CC} <4.5V)

Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3V	t_F	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7

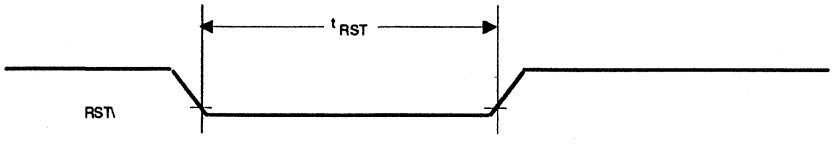
TIMING DIAGRAM—READ CYCLE TO SMARTWATCH



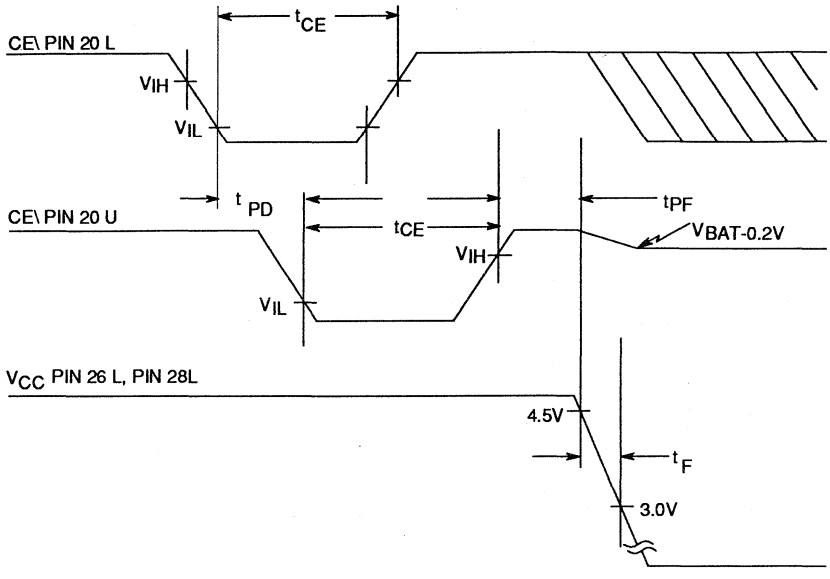
TIMING DIAGRAM—WRITE CYCLE TO SMARTWATCH



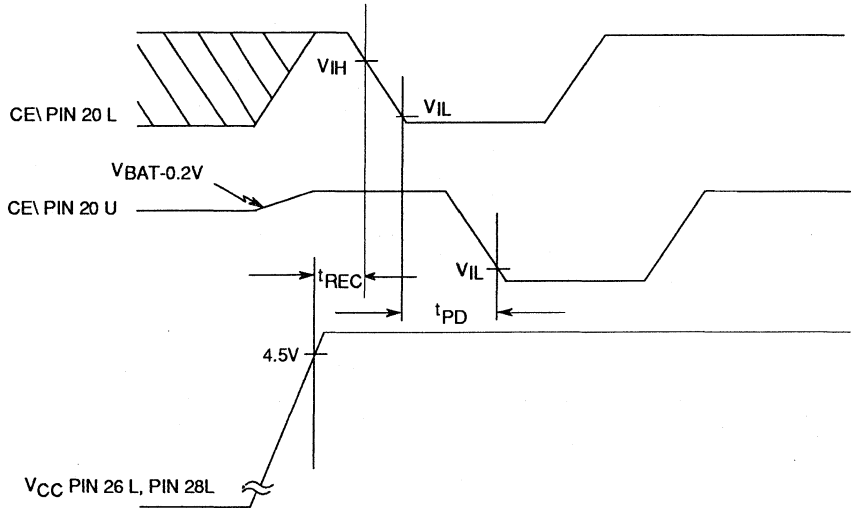
TIMING DIAGRAM—RESET FOR SMARTWATCH



TIMING DIAGRAM--POWER-DOWN



TIMING DIAGRAM--POWER-UP



WARNING

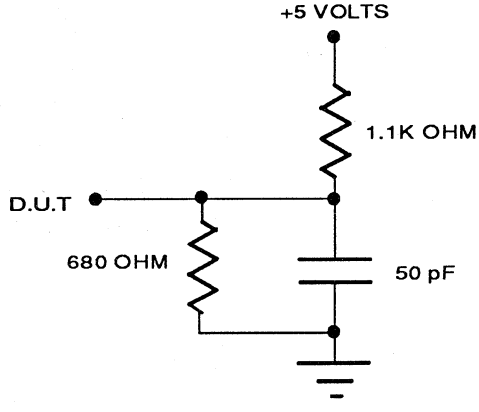
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Pin 26L can be connected to V_{CC} or left disconnected at the PC board.
6. I_{BAT} is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25°C.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. V_{CC} is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L, and 27 L.
11. t_{WR} is a function of the latter occurring edge of WE\ or CE\.
12. t_{DH} and t_{DS} are a function of the first occurring edge of WE\ or CE\.
13. RST\ (Pin 1) has an internal pull-up resistor.

OUTPUT LOAD Figure 3



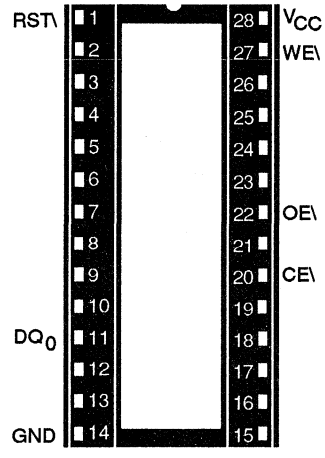
DALLAS SEMICONDUCTOR

DS1216C
SmartWatch/RAM 64/256K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Converts standard 8K x 8 and 32K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than +/- 1 min./month @ 25°C

PIN DESCRIPTION



28-Pin Intelligent Socket

PIN NAMES (\ Denotes Condition Low)

All pins pass through except 20, 28.

Pin 20	Conditioned Chip Enable
Pin 28	Switched V_{CC}
Pin 1	RESET\
Pin 22	Output Enable\
Pin 27	Write Enable\
Pin 11	Data Input/Output 0
Pin 14	Ground

DESCRIPTION

The DS1216C SmartWatch/RAM is a 28-pin, 0.6-inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8 or a 32K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

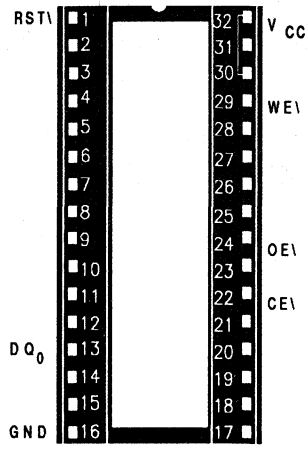
DALLAS SEMICONDUCTOR

DS1216D
SmartWatch/RAM 256K/1M

FEATURES

- Converts standard 8K x 8, 32K x 8, 128K x8, and 512K x 8 CMOS static RAMs into nonvolatile memory
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than +/- 1 min./month @ 25°C

PIN DESCRIPTION



32-Pin Intelligent Socket

PIN NAMES (\ Denotes Condition Low)

All pins pass through except 22, 30 and 32.

Pin 22 - Conditioned Chip Enable
Pin 32 - Switched V_{CC} for 32-pin RAM
Pin 1 - RESET\
Pin 24 - Output Enable
Pin 29 - Write Enable
Pin 13 - Data Input/Output 0
Pin 16 - Ground
Pin 30 - Switched V_{CC} for 28-pin RAM

DESCRIPTION

The DS1216D SmartWatch/RAM 256K/1M is a 32-pin, 0.6 inch-wide DIP socket with a built-in CMOS watch function, a nonvolatile RAM controller circuit, and an embedded lithium energy source. It accepts either an 8K x 8, 32K x 8, 128K x 8, or 512K x 8 JEDEC bytewide CMOS static RAM. When the socket is mated with a CMOS RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the RAM.

See the DS1216B SmartWatch/RAM 16/64K data sheet for technical details.

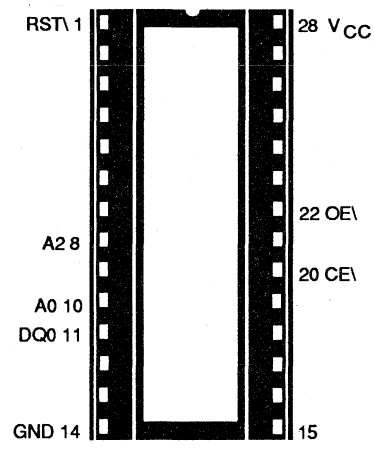
DALLAS SEMICONDUCTOR

DS1216E
SmartWatch/ROM 64/256K

FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ±10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accurate to within ±1 minute/month @25°C

PIN DESCRIPTION



28-Pin Intelligent Socket

PIN NAMES(\Denotes Condition Low)

Pin 1 RST\	Reset
Pin 8 A2	Address Bit 2(READ/ WRITE\)
Pin 10 A0	Address Bit 0(Data Input)
Pin 11 DQ0	I/O_0(Data Output)
Pin 14 GND	Ground
Pin 20 CE\	Conditioned Chip Enable
Pin 22 OE\	Output Enable
Pin 28 V_{CC}	+5 VDC to the Socket

All pins pass through to the socket except 20.

DESCRIPTION

The DS1216E SmartWatch/ROM 64/256K is a 28-pin, 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of the SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20, and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 (CE\), which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnects the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals OE\ and CE\, and data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit AO. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal (OE\ or CE\) must transition low to begin and high to end memory cycles that are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle.

Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch, ensuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of READ/WRITE\ (A2). Cycles to other locations outside the memory block can be interleaved with CE\ and OE\ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 (RESET\) low if enabled, or on power-up. The RESET\ can occur during pattern recognition or while accessing the SmartWatch registers. RESET\ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. The second function provides power-fail detection. Power-fail detection typically occurs at 4.25 volts. Finally, the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power-fail detection has occurred. Power-fail detection also has the same effect on data transfer as the RESET\ input.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

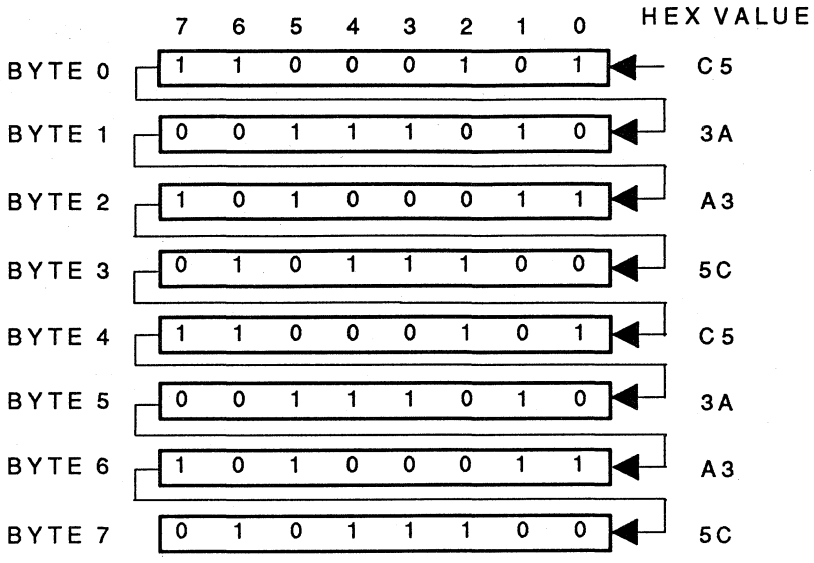
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the RESET\ and oscillator functions. Bit 4 controls the RESET\ (pin 1). When the RESET\ bit is set to logic 1, the RESET input pin is ignored. When the RESET\ bit is set to logic 0, a low input on the RESET\ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is turned off. When set to logic 0, the oscillator turns on and the watch becomes operational. Both bits are set to a logic 1 when shipped from the factory

ZERO BITS

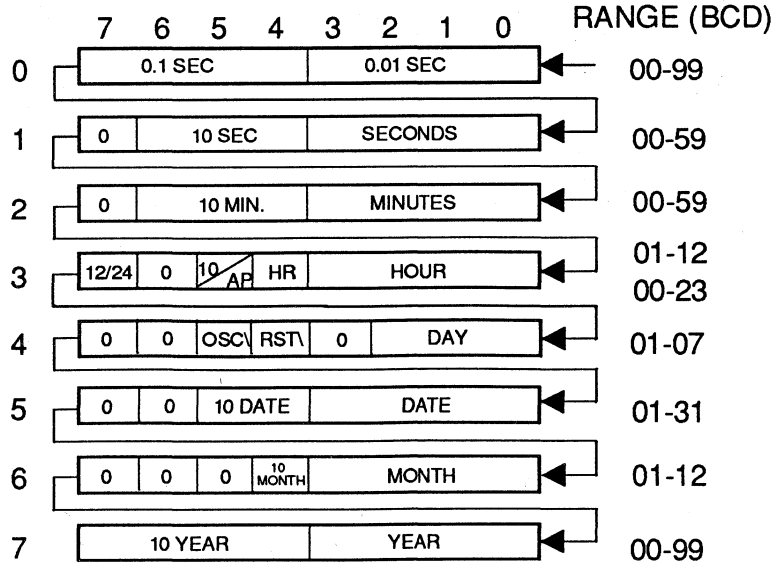
Registers 1,2,3,4,5,and 6 contain one or more bits which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE:
The pattern recognition sequence in Hex is C5, 3A, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch are less than 1 in 10^{19}.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1,3
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1,6
Logic 0	V_{IL}	-0.3		+0.8	V	1,6

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Current	I_{CC}			5	mA	3,4
Input Leakage	I_{IL}	-1.0		+1.0	uA	4,6,10
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

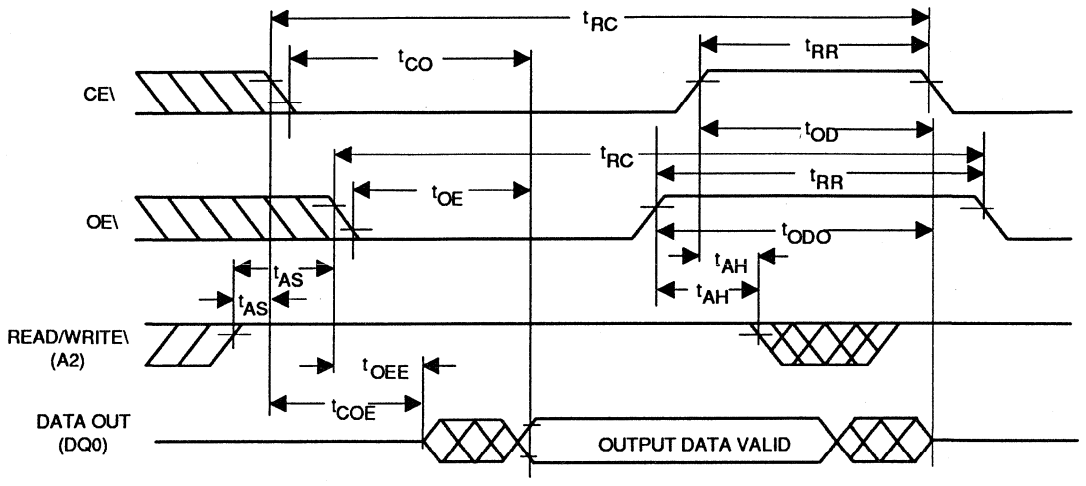
(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
OE\ Access Time	t_{OE}			200	ns	
CE\ to Output in Low Z	t_{COE}	10			ns	
OE\ to Output in Low Z	t_{OEE}	10			ns	
CE\ to Output in High Z	t_{OD}			100	ns	
OE\ to Output in High Z	t_{ODO}			100	ns	
Address Setup Time	t_{AS}	20			ns	9
Address Hold Time	t_{AH}			10	ns	8
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
CE\ Pulse Width	t_{CW}	170			ns	
OE\ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	7
Data Setup Time	t_{DS}	100			ns	8
Data Hold Time	t_{DH}	10			ns	8
RST\ Pulse Width	t_{RST}	200			ns	
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2,5
CE\ High to Power-Fail	t_{PF}			0	ns	

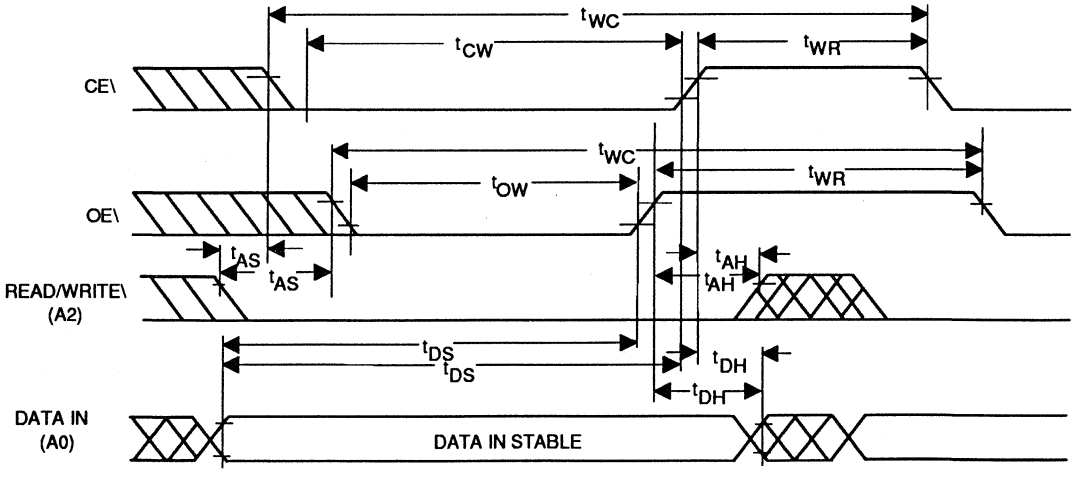
(0°C to 70°C, V_{CC} <4.5V)

Recovery at Power-Up	t_{REC}			2	ms
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms

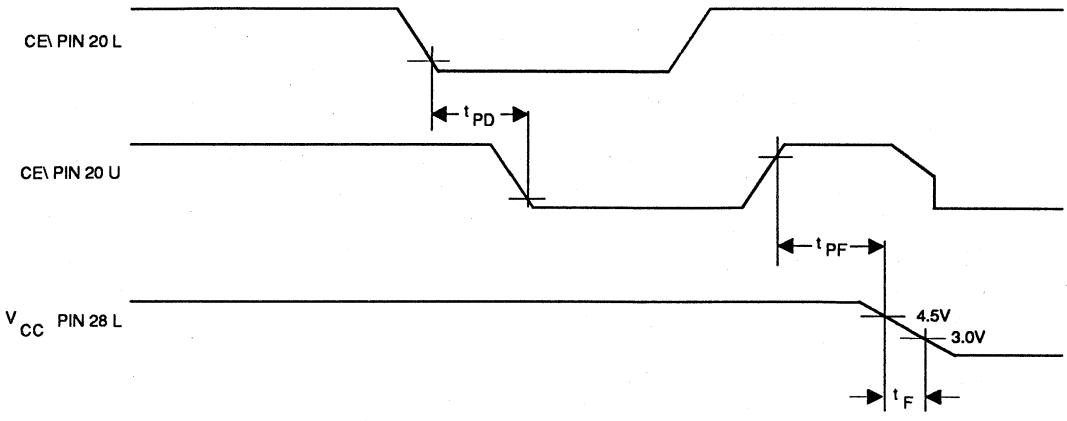
TIMING DIAGRAM - READ CYCLE



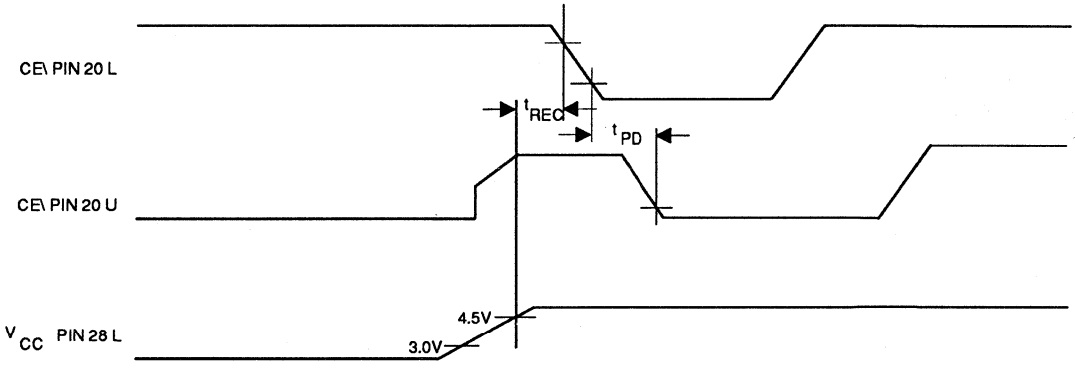
TIMING DIAGRAM - WRITE CYCLE



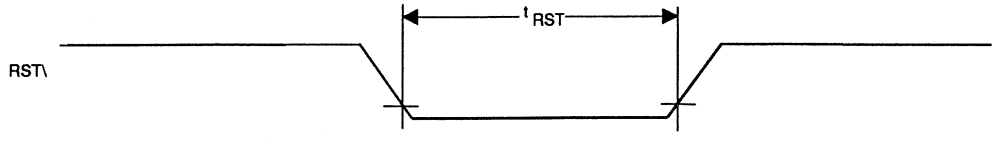
TIMING DIAGRAM - POWER-DOWN



TIMING DIAGRAM - POWER-UP



TIMING DIAGRAM - RESET FOR SMARTWATCH

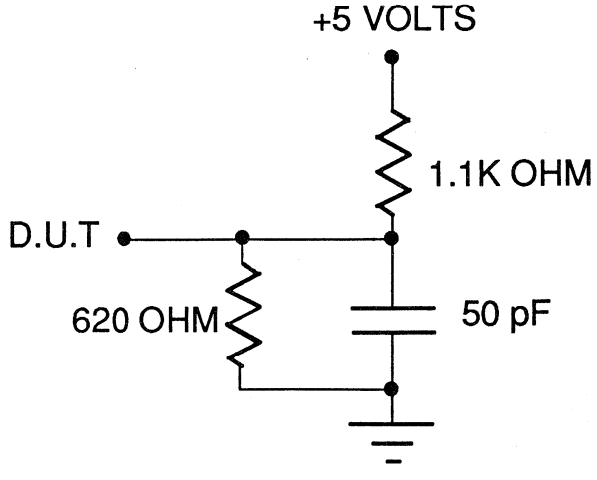


WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode. Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES:

1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. t_{WR} and t_{RR} are functions of the first occurring edge of OE\ or CE\.
8. t_{AH}, t_{DS}, and t_{DH} are functions of the first occurring edge of OE\ or CE\.
9. t_{AS} is a function of the latter occurring edge of OE\ or CE\.
10. RST\ (Pin 1) has an internal pull-up resistor.

OUTPUT LOAD Figure 3



DALLAS SEMICONDUCTOR

DS1216F
SmartWatch/ROM 64/256K/1M

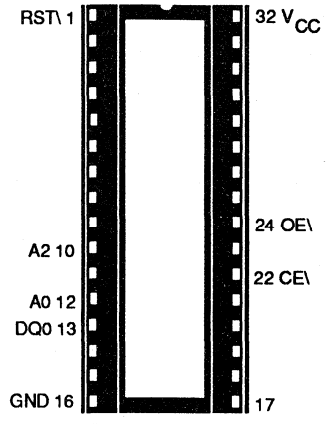
FEATURES

- Adds timekeeping to any 32-pin JEDEC bytewide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full ± 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ± 1 minute/month @ 25°C

DESCRIPTION

The DS1216F SmartWatch/ROM is a 32-pin, 600 mil-wide DIP socket with a built-in CMOS timekeeper and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeping function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source automatically switches on to prevent loss of time and calendar data.

PIN DESCRIPTION



32-Pin Intelligent Socket

PIN NAMES (\Denotes Condition Low)

Pin 1 RST\	- RESET
Pin 10 A2	- Address Bit 2 (READ/ WRITE\)
Pin 12 A0	- Address Bit 0 (Data Input)
Pin 13 DQ0	- I/O0 (Data Output)
Pin 16 GND	- Ground
Pin 22 CE\	- Conditioned Chip Enable
Pin 24 OE\	- Output Enable
Pin 32 V_{CC}	- +5 VDC to the Socket

All pins pass through to the socket except 22.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device takes up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22, and 24 for timekeeper control. All pins pass through to the socket receptacle except for pin 22 (CE\), which is inhibited during the transfer of time information.

See the DS1216E SmartWatch/ROM/64/256K data sheet for technical details.

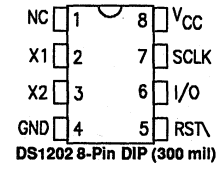
Timekeeping

DALLAS SEMICONDUCTOR

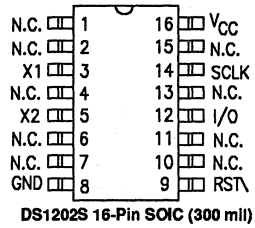
DS1202
Serial Timekeeper Chip

FEATURES
- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation
- 24 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0-5.5 volt clock operation
- Uses less than 300na at 2 volts
- Single- byte or multiple-byte (burst mode) data transfer for read or write of clock or RAM data
- 8-pin DIP or optional 16-pin SOIC for surface mount
- Simple 3-wire interface
- TTL-compatible (V_{CC} = 5V)
- Optional industrial temperature range -40°C to +85°C

PIN CONNECTIONS



DS1202 8-Pin DIP (300 mil)



DS1202S 16-Pin SOIC (300 mil)

PIN NAMES (\ Indicates Condition Low)

N.C.	-No Connection
X1, X2	-32.768 KHz Crystal Input
GND	-Ground
RST\	- Reset
I/O	-Data Input/Output
SCLK	-Serial Clock
V_{CC}	-Power Supply Pin

DESCRIPTION
The DS1202 Serial Timekeeper Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/ calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12- hour format with an AM/PM indicator. Interfacing the DS1202 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock /RAM: (1) RST\ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

OPERATION

The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM. To initiate any transfer of data, RST\ is taken high and eight bits are loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first eight bits specify which of 32 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have occurred which load the command word into the shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals eight plus eight for byte mode or eight plus up to 192 for burst mode.

COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logical one. If it is zero, further action will be terminated. Bit 6 specifies clock/calendar data if logic zero or RAM data if logic one. Bits one through five specify the designated registers to be input or output, and the LSB (Bit 0) specifies a write operation (input) if logic zero or read operation (output) if logic one. The command byte is always input starting with the LSB (bit 0).

BURST MODE

Burst mode can be specified for either the clock/calendar or the RAM registers by initiating a burst mode command. Bit six specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity in the clock/calendar or in the RAM for command bytes. Data I/O starts with the LSB (Bit 0) of address 0.

WRITE PROTECT COMMAND BYTE

Before any write operation to the clock/calendar or RAM, the write protect bit must be zero. This operation requires driving RST\ high and loading the write protection command byte 8Eh, followed by data byte 00h. RST\ must be driven low before any other command can be initiated. To restore write protect, drive RST\ high followed by the WRITE PROTECT command byte, 8Eh, and data byte 80h. Sixteen clock cycles are required for this operation. Complete the operation by driving RST\ low.The write protect bit cannot be written to in the burst mode.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RST\ input high. The RST\ input serves two functions. First, RST\ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the RST\ signal provides a method of terminating either single byte or multiple byte data transfer. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. All data transfer terminates if the RST\ input is low and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

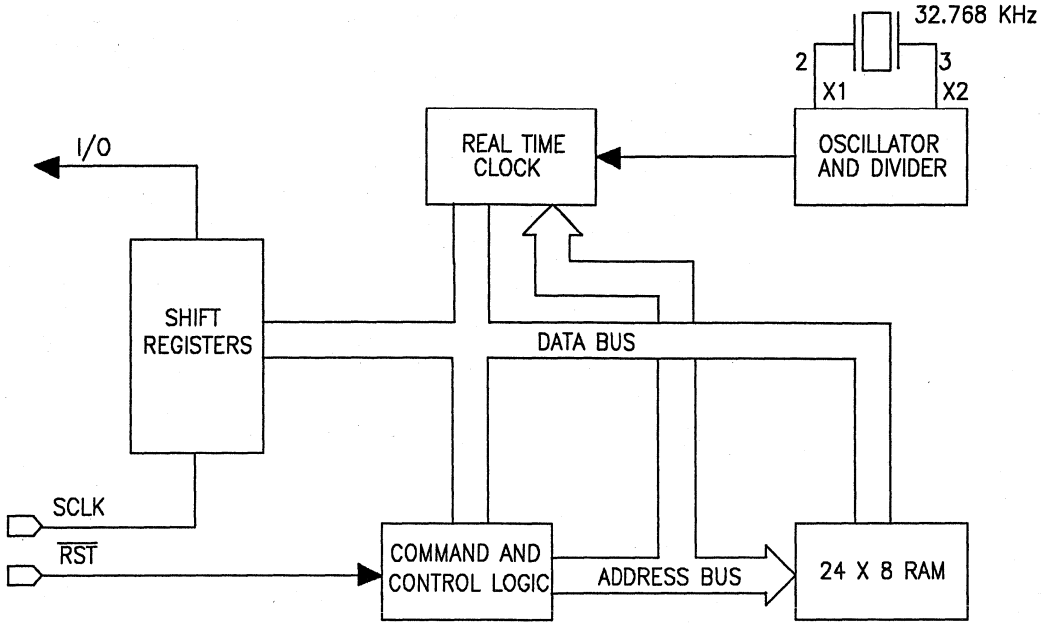
DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

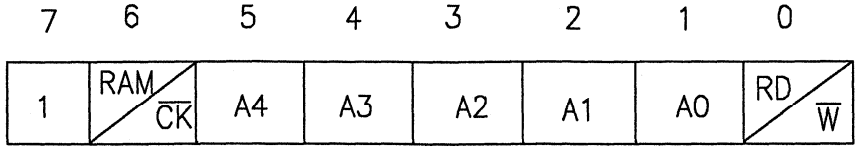
DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as RST\ remains high. This operation permits continuous burst mode read capability. Data is output starting with bit 0.

DS1202 BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND BYTE Figure 2



CLOCK/CALENDAR

The clock/calendar is contained in eight write/read registers as shown in Figure 4. Data contained in the clock/calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic one, the clock oscillator is stopped and the DS1202 is placed into a low-power standby mode with a current drain of not more than 100 nanoamps. When this bit is written to logic zero, the clock will start.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10 hour bit (20-23 hours).

WRITE PROTECT REGISTER

Bit 7 of write protect register is the write protect bit. The first seven bits (bits 0-6) are forced to zero and will always read a zero when read. Before any write operation to the clock or RAM, bit 7 must be zero. When high, the write protect bit prevents a write operation to any other register.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

RAM

The static RAM is 24 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 24 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

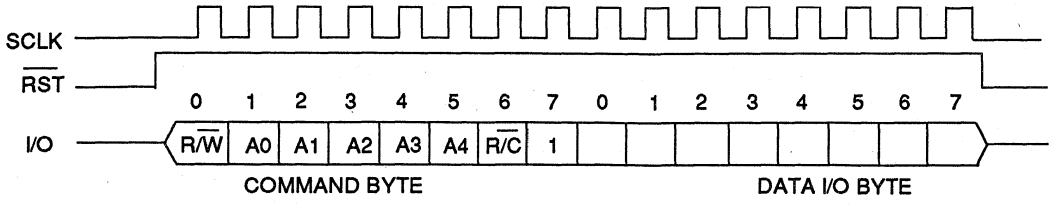
A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

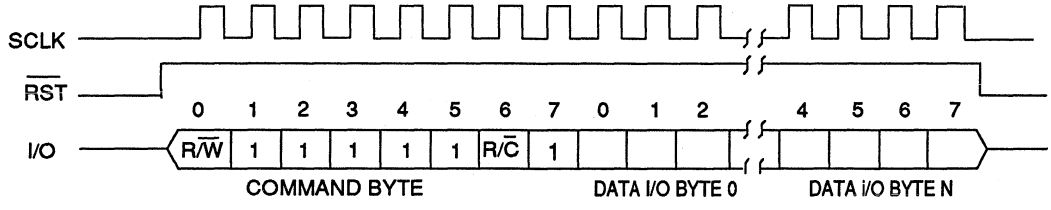
A 32.768 KHz crystal, Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, can be directly connected to the DS1202 via pins 2 and 3 (x1, x2). The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER



BURST FUNCTION	DATA (BYTES)	SCLK
CLOCK	8	72
RAM	24	200

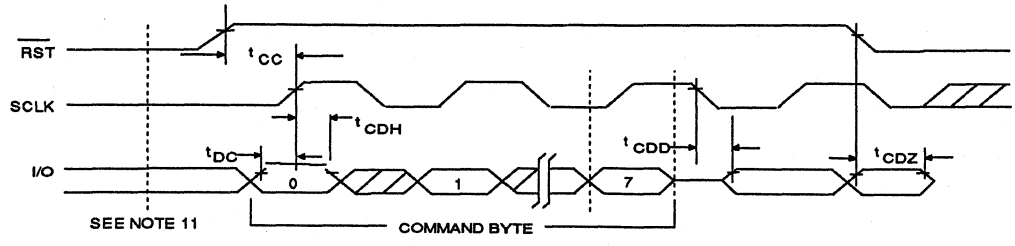
COMMAND BYTES/DEFINITION Figure 4

REGISTER	FUNCTION	COMMAND ADDRESS (HEX)	WRITE=W READ=R	RANGE DATA (BCD)	REGISTER DEFINITION 7	6	5	4	3	2	1	0
0	SECONDS	80 81	W R	00-59	CH	10 SEC			SEC			
1	MINUTES	82 83	W R	00-59	0	10 MIN			MIN			
2	12HRS 24 HRS	84 85	W R	01-12 00-23	12\ 24	0 0	AP 10	HR HR	HOUR			
3	DATE	86 87	W R	01-31	0	0	10DATE		DATE			
4	MONTH	88 89	W R	01-12	0	0	0	10M	MONTH			
5	DAY	8A 8B	W R	01-07	0	0	0	0	DAY			
6	YEAR	8C 8D	W R	00-99	10 YEAR				YEAR			
7	WRITE PROTECT	8E 8F	W R	00-80	WP	ALWAYS ZERO						

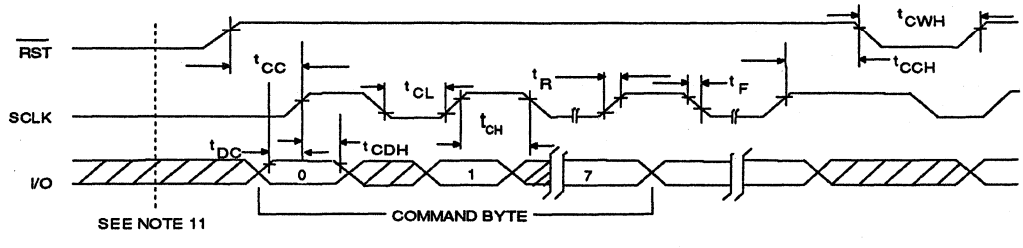
31	CLOCK BURST	BE	W
		BF	R
0	RAM 0	C0	W
		C1	R
•	•	•	•
•	•	•	•
23	RAM 23	EE	W
31	RAM BURST	FE	W
		FF	R

TIMING DIAGRAM - READ/WRITE DATA TRANSFER Figure 5

READ DATA TRANSFER



WRITE DATA TRANSFER



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0° to +70°C)

PARAMETER	SYMBOL		MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		2.0	5.5	VOLTS	1
Logic 1 Input	V_{IH}		2.0	V_{CC}+0.3	VOLTS	1
Logic 0 Input	V_{IL}	V_{CC}=2.0V	-0.3	+0.3	VOLTS	1
		V_{CC}=5V	-0.3	+0.8		

DC ELECTRICAL CHARACTERISTICS

(0° to +70°C, V_{CC} = 2.0 to 5.5V*)

PARAMETER	SYMBOL		MIN	MAX	UNITS	NOTES
Input Leakage	I_{LI}			+500	uA	6
I/O Leakage	I_{LO}			+500	uA	6
Logic 1 Output	V_{CC}=2V	V_{OH}	1.6		VOLTS	2
	V_{CC}=5V		2.4			
Logic 0 Output	V_{CC}=2V	V_{OL}		0.4	VOLTS	3
	V_{CC}=5V			0.4		
Active Supply Current	V_{CC}=2V	I_{CC}		.4	mA	4
	V_{CC}=5V			1.2		
Timekeeping Current	V_{CC}=2V	I_{CC1}		0.3	uA	5
	V_{CC}=5V			1		
Leakage Current	V_{CC}=2V	I_{CC2}		100	nA	10
	V_{CC}=5V			100		

*Unless otherwise noted.

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	
Crystal Capacitance	C_X		6		pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=+5V +/- 10%*)

PARAMETER	SYMBOL		MIN	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	V_{CC}=2V	200		ns	7
		V_{CC}=5V	50			
CLK To Data Hold	t_{CDH}	V_{CC}=2V	280		ns	7
		V_{CC}=5V	70			
CLK To Data Delay	t_{CDD}	V_{CC}=2V		800	ns	7,8,9
		V_{CC}=5V		200		
CLK Low Time	t_{CL}	V_{CC}=2V	1000		ns	7
		V_{CC}=5V	250			
CLK High Time	t_{CH}	V_{CC}=2V	1000		ns	7,12
		V_{CC}=5V	250			
CLK Frequency	f_{CLK}	V_{CC}=2V		0.5	MHz	7,12
		V_{CC}=5V	D.C.	2.0		
CLK Rise &Fall	t_R, t_F	V_{CC}=2V		2000	ns	
		V_{CC}=5V		500		
RST\ To CLK Setup	t_{CC}	V_{CC}=2V	4		us	7
		V_{CC}=5V	1			
CLK To RST\ Hold	t_{CCH}	V_{CC}=2V	240		ns	7
		V_{CC}=5V	60			
RST\ Inactive Time	t_{CWH}	V_{CC}=2V	4		us	7
		V_{CC}=5V	1			
RST\ To I/O High Z	t_{CDZ}	V_{CC}=2V		280	ns	7
		V_{CC}=5V		70		

*Unless otherwise noted.

NOTES

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at V_{CC} = 5V and .4 mA at V_{CC} = 2V.
3. Logic zero voltages are specified at a sink current of 4 mA at V_{CC} = 5V and 1.5 mA at V_{CC} = 2V.
4. I_{CC} is specified with the I/O pin open.
5. I_{CC1} is specified with the I/O pin open, RST\ High, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500KHz, V_{CC} = 2V and Clock Halt Flag = 0 (Oscillator enabled).
6. RST\, SCLK, and I/O all have 40 K ohm pulldown resistors to ground.
7. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10 ms maximum rise and fall time.
8. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
9. Load capacitance = 50 pF.
10. I_{CC2} is specified with RST\, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
11. At power-up, RST\ must be at a logic 0 until $V_{CC} \geq$ 2 volts. Also SCLK must be at a logic 0 when RST\ is driven to a logic one state.
12. If t_{CH} exceeds 100 ms with RST\ in a logic one state, then I_{CC} may briefly exceed I_{CC} specification.

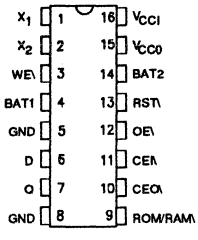
DALLAS SEMICONDUCTOR

DS1215/S
Phantom Time Chip

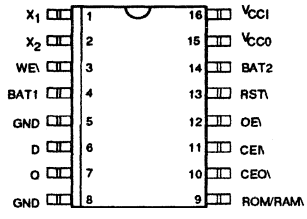
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected
- No address space required
- Provides nonvolatile controller functions for battery backup of RAM
- Supports redundant batteries for high-rel applications
- Uses a 32.768 KHz watch crystal
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Space-saving, 16-pin DIP package and SOIC

PIN DESCRIPTION



16 Pin DIP (300 mil)



16 Pin SOIC (300 mil)

PIN NAMES (\ Denotes Condition Low)

Pins 1&2	- X_1, X_2	- 32.768 KHz Crystal Connections
Pin 3	- WE\	- Write Enable
Pin 4	- BAT_1	- Battery 1 Input
Pins 5&8	- GND	- Ground
Pin 6	- D	- Data In
Pin 7	- Q	- Data Out
Pin 9	- ROM/ RAM\	- ROM-RAM Select
Pin 10	- CEO\	- Chip Enable Out
Pin 11	- CEI\	- Chip Enable Input
Pin 12	- OE\	- Output Enable
Pin 13	- RST\	- Reset
Pin 14	- BAT_2	- Battery 2 Input
Pin 15	- V_{CCO}	-Switched Supply Output
Pin 16	- V_{CCI}	- +5V DC Input

NOTE: Both pins 5 and 8 must be grounded.

DESCRIPTION

The DS1215 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information, while the nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24-hour mode.

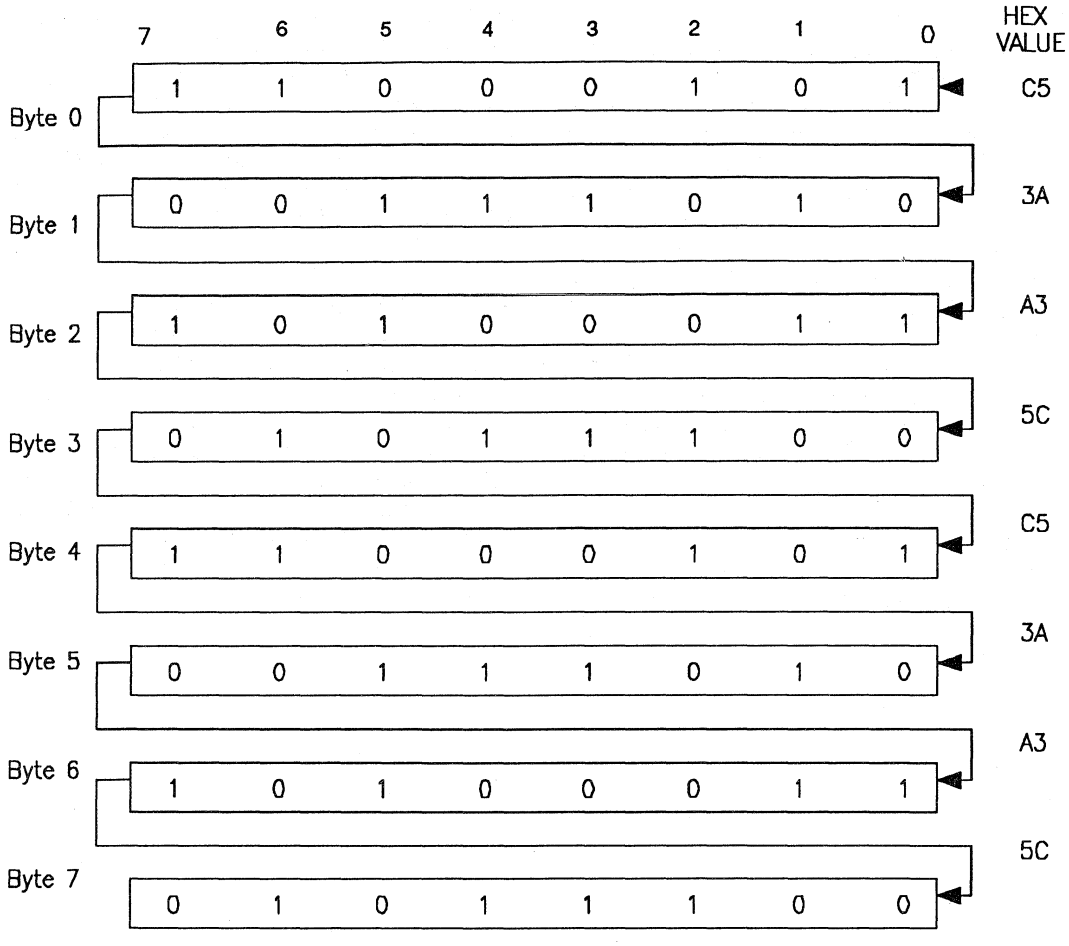
NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/RAM\ select pin. When ROM/RAM\ is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or V_{CCI} to V_{CCO} with a maximum voltage drop of 0.3 volts. The V_{CCO} output pin is used to supply uninterrupted power to CMOS SRAM. The DS1215 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to V_{CCO}. If only one battery is used in the system, the unused battery input should be connected to ground.

The DS1215 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when V_{CCI} falls below VTP, which is equal to 1.26 x V_{BAT}. The DS1215 constantly monitors the V_{CCI} supply pin. When V_{CCI} is less than VTP, a comparator outputs a power-fail signal to the control logic. The power-fail signal forces the chip enable output (CEO\) to V_{CCI} or V_{BAT}-0.2 volts for external RAM write protection. During nominal supply conditions, CEO\ will track CE\ with a maximum propagation delay of 20ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until V_{CCI} exceeds VTP. A typical RAM/Time Chip interface is illustrated in Figure 4.

When the ROM/RAM\ pin is connected to V_{CCO}, the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will not force CEO\ high when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power-fail as V_{CCI} falls below the level of V_{BAT}. A typical ROM/Time Chip interface is illustrated in Figure 5.

TIME CHIP COMPARISON REGISTER DEFINITION Figure 1



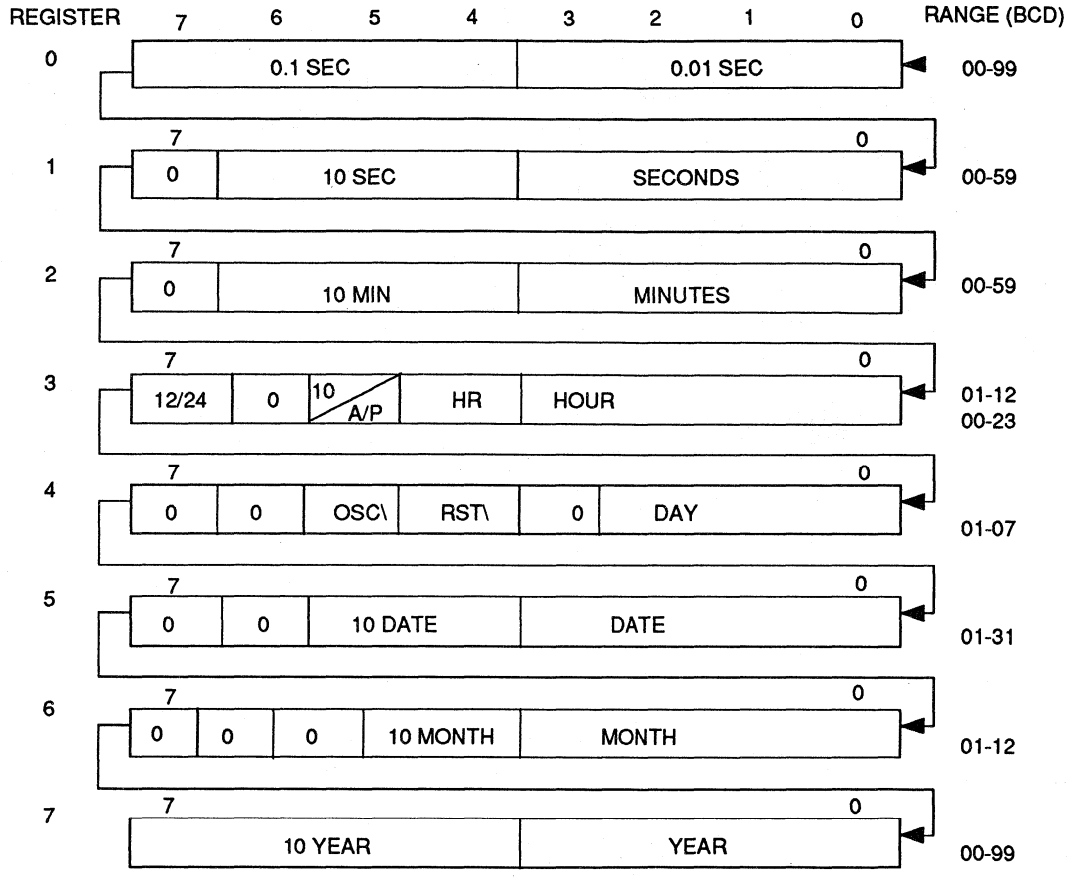
NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in 10^{19}.

TIME CHIP REGISTER INFORMATION

Time Chip information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the Time Chip registers is not binary coded decimal format (BCD) in the12-hour mode. Reading and writing the registers is always accomplished by stepping though all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

TIME CHIP REGISTER DEFINITION Figure 2



AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

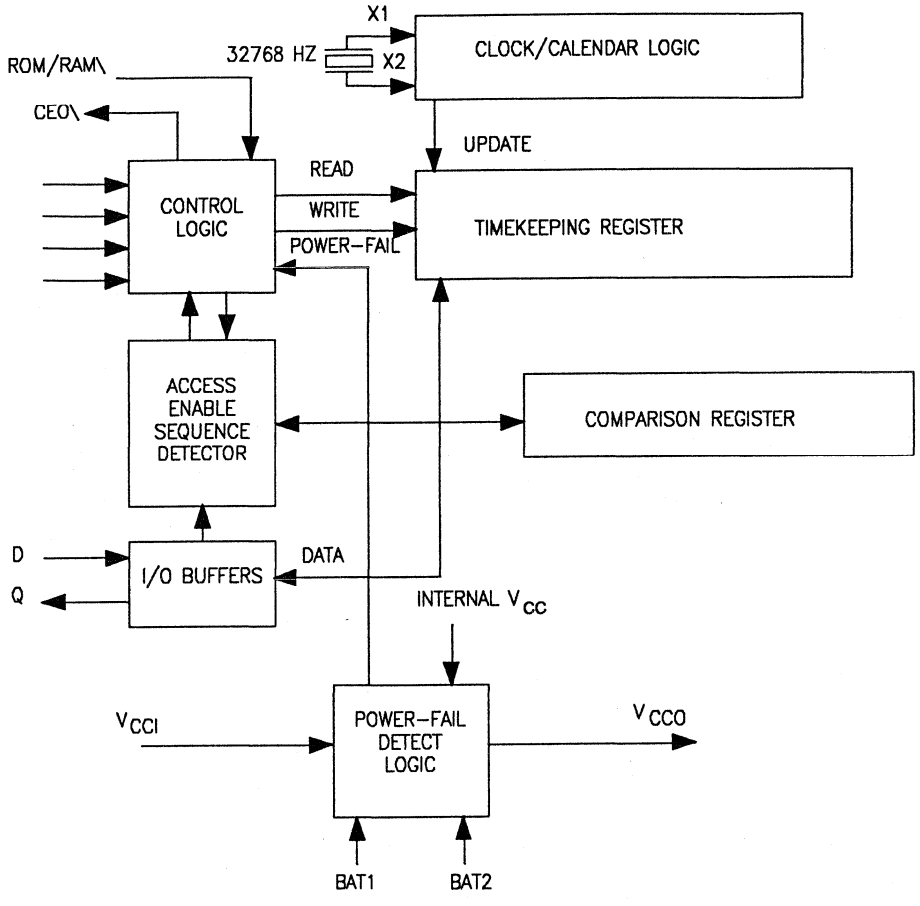
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the time-keeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the watch becomes operational.

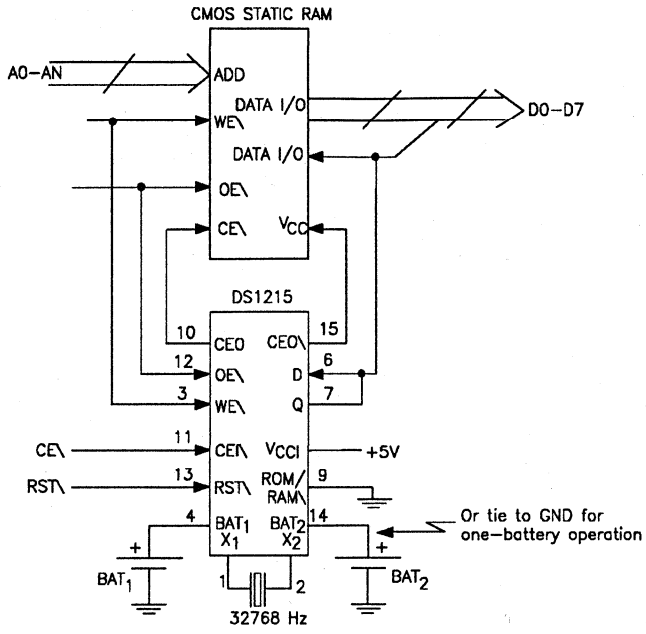
ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

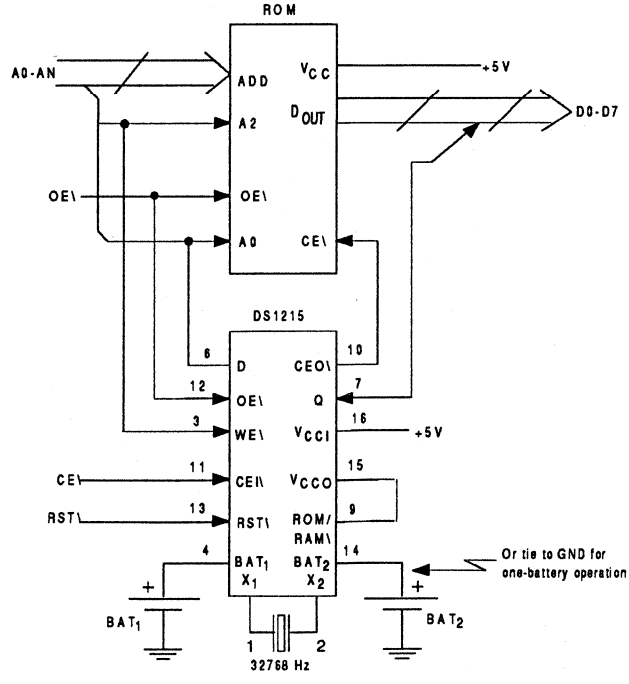
TIMING BLOCK DIAGRAM Figure 3



RAM/TIME CHIP INTERFACE Figure 4



ROM/TIME CHIP INTERFACE Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3 V		1
Logic 0	V_{IL}	-0.3		+0.8	V	1
V_{BAT1} or V_{BAT2} Battery Voltage	V_{BAT}	2.5		3.7	V	7

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	6
Supply Current $V_{CCO}=V_{CCI}$-0.3	I_{CCO1}			80	mA	8
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Output @ 2.4V	I_{OH}	-1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°C, V_{CC} < 4.5V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
CEO\ Output	V_{OH1}	V_{CCI} or V_{BAT}-0.2		V	9
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}		1	uA	6
Battery Backup Current @ $V_{CCO}=V_{BAT}$-0.2V	I_{CCO2}		10	uA	10

AC ELECTRICAL CHARACTERISTICS ROM/RAM\=GND(0^oC to 70^oC, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
OE\ Access Time	t_{OE}			100	ns	
CE\ to Output Low Z	t_{COE}	10			ns	
OE\ to Output Low Z	t_{OEE}	10			ns	
CE\ to Output High Z	t_{OD}			100	ns	
OE\ to Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Setup	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
CE\ Pulse Width	t_{CW}	170			ns	
RST\ Pulse Width	t_{RST}	200			ns	
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
CE\ High to Power-Fail	t_{PF}			0	ns	

(0^oC to 70^oC, V_{CC} < 4.5V)

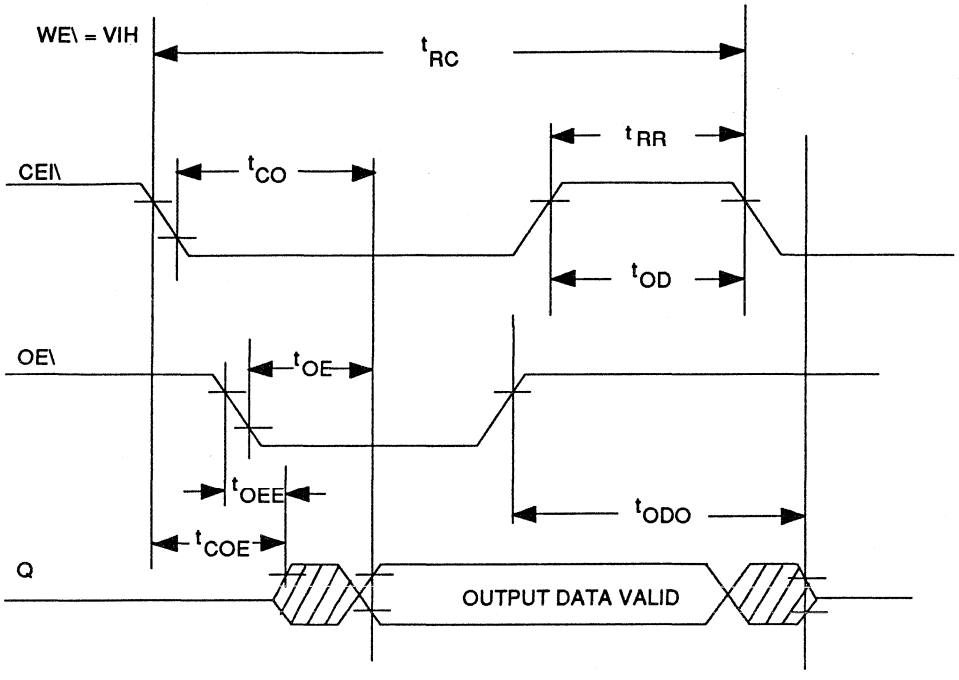
Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

CAPACITANCE

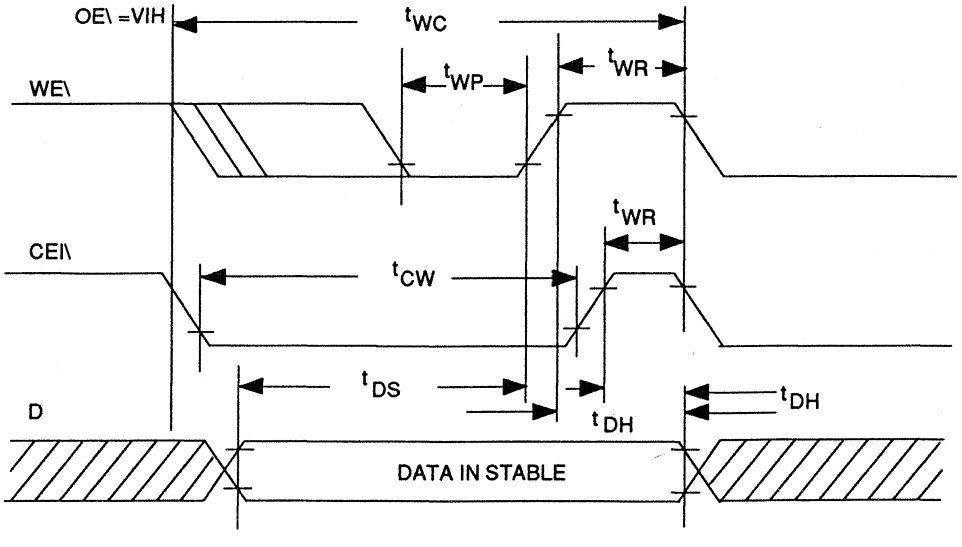
(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5			pF	
Output Capacitance	C_{OUT}	7			pF	

TIMING DIAGRAM-READ CYCLE TO TIME CHIP ROM/RAM\=GND



TIMING DIAGRAM-WRITE CYCLE TO TIME CHIP ROM/RAM\=GND



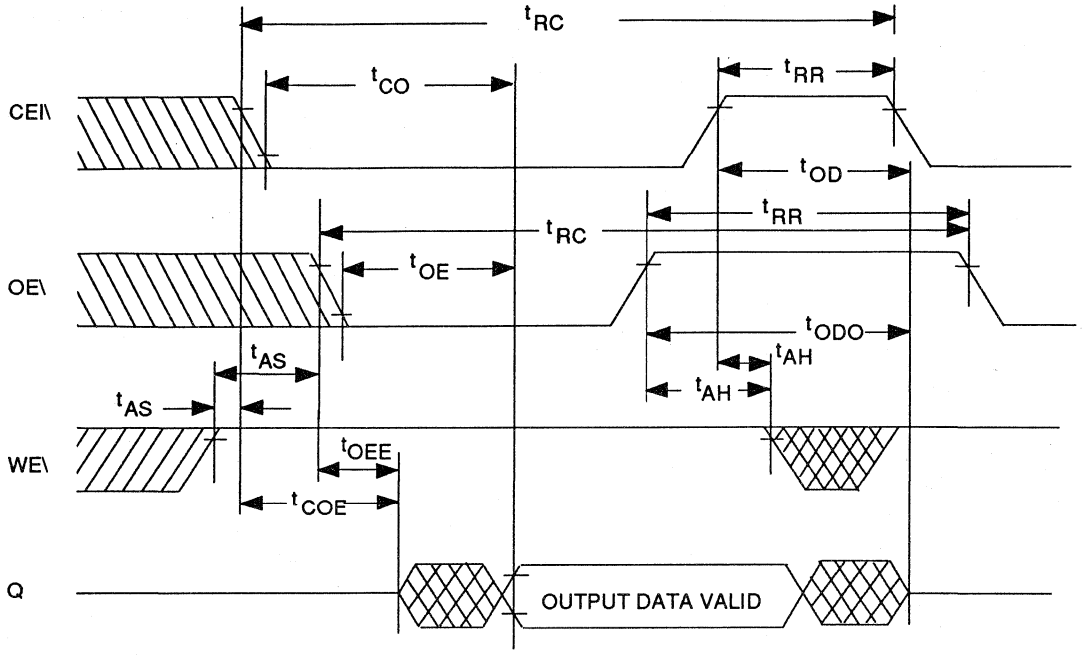
AC ELECTRICAL CHARACTERISTICS ROM/RAM\=V_{CCO} (0°C to 70°C; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
OE\ Access Time	t_{OE}			200	ns	
CE\ to Output in Low Z	t_{COE}	10			ns	
OE\ to Output in Low Z	t_{OEE}	10			ns	
CE\ to Output in High Z	t_{OD}			100	ns	
OE\ to Output in High Z	t_{ODO}			100	ns	
Address Setup Time	t_{AS}	20			ns	
Address Hold Time	t_{AH}			10	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
CE\ Pulse Width	t_{CW}	170			ns	
OE\ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	4
Data Setup Time	t_{DS}	100			ns	5
Data Hold Time	t_{DH}	10			ns	5
RST\ Pulse Width	t_{RST}	200			ns	
CE\ Propagation Delay	t_{PD}	5	10	20	ns	2, 3
CE\ High to Power Fail	t_{PF}			0	ns	

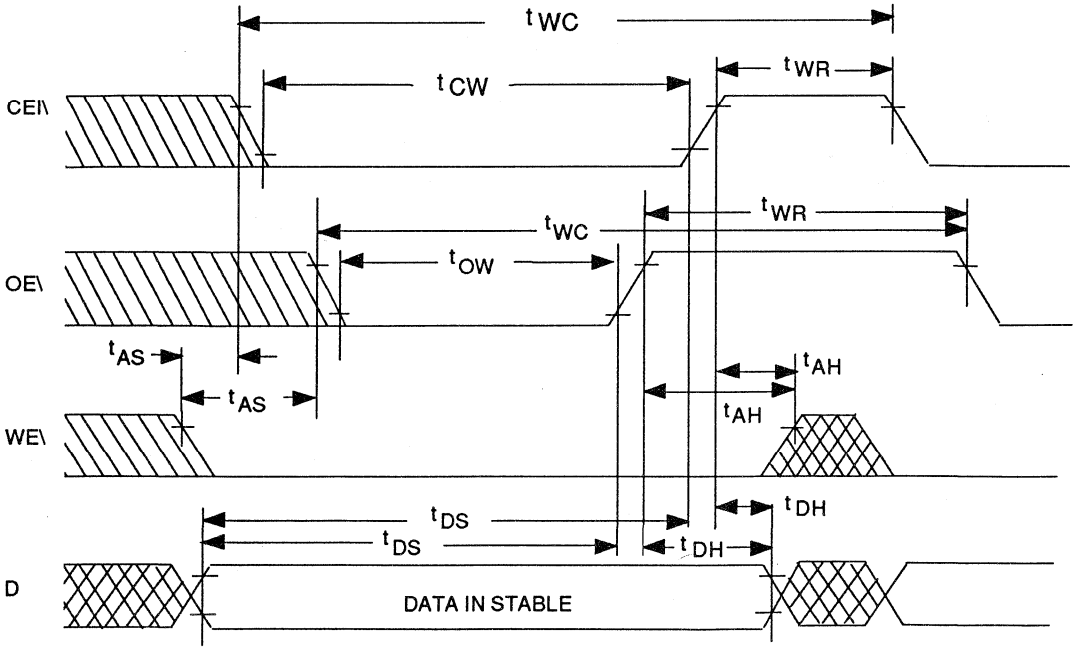
(0°C to 70°C, V_{CC} < 4.5V)

Recovery at Power-Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 - 3.0V	t_F	0			ms	

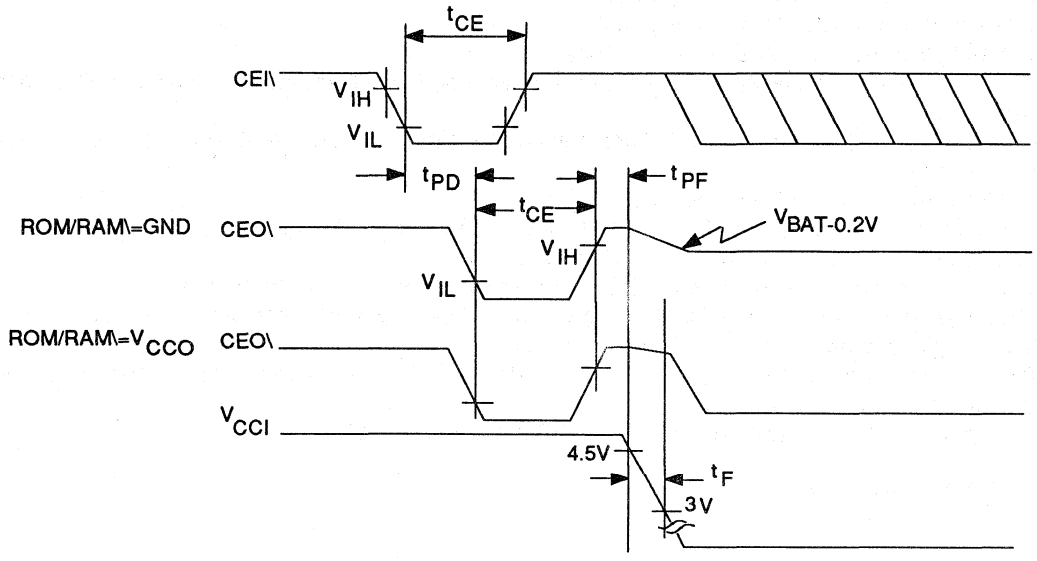
TIMING DIAGRAM-READ CYCLE ROM/RAM\=V_{cco}



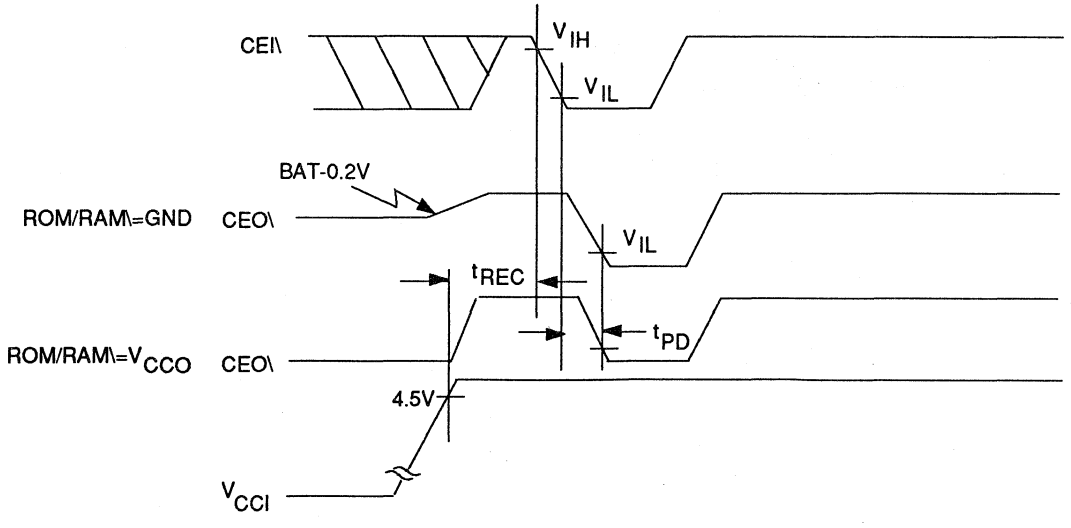
TIMING DIAGRAM-WRITE CYCLE ROM/RAM\=V_{cco}



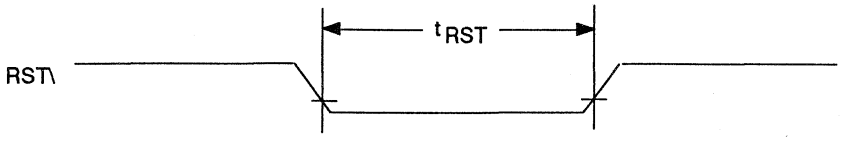
TIMING DIAGRAM--POWER-DOWN



TIMING DIAGRAM--POWER-UP



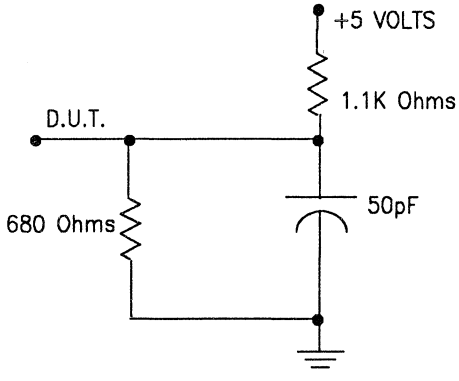
TIMING DIAGRAM--RESET FOR TIME CHIP



NOTES

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10ns.
4. t_{WR} is a function of the latter occurring edge of WE\ or CE\ in RAM mode, or OE\ or CE\ in ROM mode.
5. t_{DH} and t_{DS} are functions of the first occurring edge of WE\ or CE\ in RAM mode, or OE\ or CE\ in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power-fail detect. $V_{TP} = 1.26 \times V_{BAT}$. For 10% V_{CC}= 5V ± 10% operation V_{BAT} = 3.5V max.; for 5% operation V_{BAT} = 3.7V max.
8. I_{CCO1} is the maximum average load current the DS1215 can supply to memory.
9. Applies to CEO\ with the ROM/RAM\ pin grounded. When the ROM/RAM\ pin is connected to V_{CCO}, CEO\ will go to a low level as V_{CCI} falls below V_{BAT}.
10. I_{CCO2} is the maximum average load current that the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except RST\. RST\ is pulled internally to V_{CCI}.

OUTPUT LOAD Figure 6



DALLAS SEMICONDUCTOR

DS1243Y
64K NV SRAM with Phantom Clock

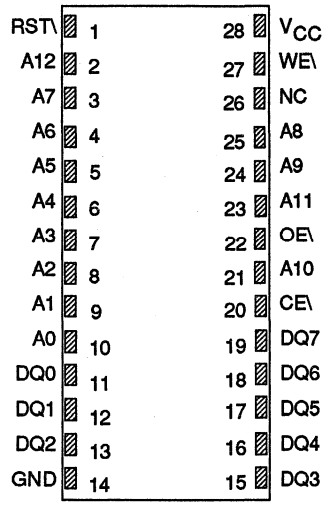
FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 8K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Timekeeping function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full ±10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than ±1 minute/month @ 25°C
- Over 10 years of data retention in the absence of power
- Unlimited write cycles

DESCRIPTION

The DS1243Y 64K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 8192 words by 8 bits) with a built-in real time clock. The DS1243Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock. For complete information and operation, electrical characteristics, and timing as it relates to the 8K x 8 nonvolatile memory, please reference the DS1225Y 64K Nonvolatile SRAM data sheet. For complete information on operation, access control, electrical characteristics, and timing of the real time clock, reference the DS1216B SmartWatch/RAM 16/64K data sheet.

PIN DESCRIPTION



28-Pin Encapsulated Package
(720 Mil Extended)

PIN NAMES (\ Denotes Condition Low)

A_0-A_{12}	-Address Inputs
CE\	-Chip Enable
GND	-Ground
DQ_0-DQ_7	-Data In/Data Out
V_{CC}	-Power (+5V)
WE\	-Write Enable
OE\	-Output Enable
NC	-No Connect
RST\	-Reset

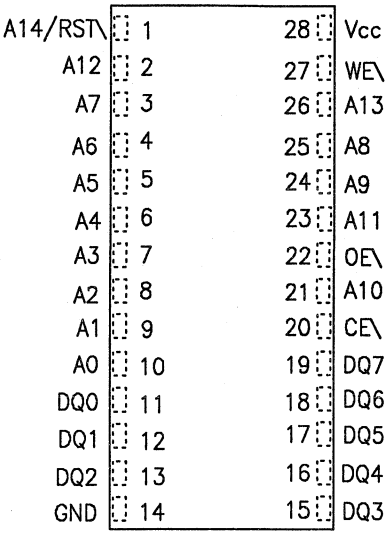
DALLAS SEMICONDUCTOR

DS1244Y
256K NV SRAM with Phantom Clock

FEATURES

- Real time clock keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years
- 32K x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains watch information and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month
- Standard 28-pin JEDEC pinout
- Full 10% operating range
- Operating temperature range 0°C to 70°C
- Accuracy is better than +/- 1 min/month @ 25°C
- Over 10 years of data retention in the absence of power
- Available in 200 ns access time

PIN DESCRIPTION



28-Pin Encapsulated Package (740 mil)

PIN NAMES (\ Denotes condition low)

A_0-A_{14}	Address Inputs
CE\	Chip Enable
GND	Ground
DQ_0-DQ_7	Data In/Data Out
V_{CC}	Power (+5V)
WE\	Write Enable
OE\	Output Enable
NC	No Connect
RST\	RESET (Clock)

DESCRIPTION

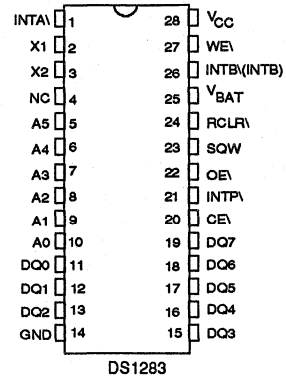
The DS1244Y 256K NV SRAM with Phantom Clock is a fully static nonvolatile RAM (organized as 32,768 words by 8 bits) with a built-in real time clock. The DS1244Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real time clock. For complete information and operation, electrical characteristics, and timing as it relates to the 32K x 8 nonvolatile memory, please reference the DS1235Y 256K Nonvolatile SRAM data sheet. For complete information on operation, access control, electrical characteristics, and timing of the real time clock, reference the DS1216B SmartWatch/RAM data sheet.

DALLAS SEMICONDUCTOR

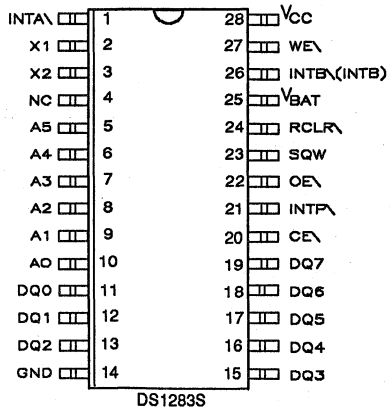
DS1283/S
Watchdog Timekeeper Chip

FEATURES
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function provides notice of real time related occurrences
- Designed for battery operation
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±2 minutes/month at 25° C
- 50 bytes of user nonvolatile RAM
- Optional 28-pin SOIC surface mount package
- Low-power CMOS circuitry is maintained on less than 1 uA in standby mode

PIN DESCRIPTION
(\ Denotes Condition Low)



DS1283
28-Pin DIP (600 mil)



DS1283S
28-Pin SOIC (330 mil)

NOTE: Pin 4 must be left disconnected.

DESCRIPTION
The DS1283 Watchdog Timekeeper Chip is a self- contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP or 28-pin SOIC surface mount package. The DS1283 is specifically designed to maintain internal operations from a single low voltage supply. In fact, the only two external components required by the DS1283 are a battery and crystal. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, V_{CC}, and RCLR\, see the DS1286 Watchdog Timekeeper data sheet.

PIN DESCRIPTION DETAIL

PIN #	NAME	I/O	DESCRIPTION
1	INTA\	O	**Interrupt Output A**
2-3	X1,X2	I	**32.768 KHz Crystal**
4	NC	-	**No Connection**
5-10	A0-A5	I	**Address Inputs: A5=Pin 5; A0=Pin 10**
11	DQ0	I/O	**Data Input/Output**
12	DQ1	I/O	**Data Input/Output**
13	DQ2	I/O	**Data Input/Output**
14	GND	-	**Ground**
15	DQ3	I/O	**Data Input/Output**
16	DQ4	I/O	**Data Input/Output**
17	DQ5	I/O	**Data Input/Output**
18	DQ6	I/O	**Data Input/Output**
19	DQ7	I/O	**Data Input/Output**
20	CE\	I	**Chip Enable**
21	INTP\	O	**Interrupt Output P**
22	OE\	O	**Output Enable**
23	SQW	O	**Square Wave Output**
24	RCLR\	I	**RAM Clear**
25	V_{BAT}	I	**+3 Volt Battery Input**
26	INTB\ (INTB)	O	**Interrupt Output B**
27	WE\	I	**Write Enable**
28	V_{CC}	I	**+3 Volt Battery**

PIN DESCRIPTIONS

X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a load capacitance (C_L) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency. Crystals can be ordered from Dallas Semiconductor Part # DS9032.

V_{BAT} - Battery input for a battery or power supply between 5.5 volts and 2.5 volts. When the DS1283 is powered by the V_{BAT} pin alone, V_{CC} and V_{BAT} must be connected together. When a single supply is used, input and output levels and timing are only guaranteed between the ranges of 4.5 volts and 5.5 volts. In this mode, the active current drain is 2 mA (CE\ = V_{IL}), the standby current is 0.5 mA (CE\ = V_{IH}), and the data retention mode is less than 1 uA typical and 1.5 uA maximum at 5.5 volts (CE\ = V_{BAT} - 0.2 volts). These current drain specifications are stated with all outputs unloaded.

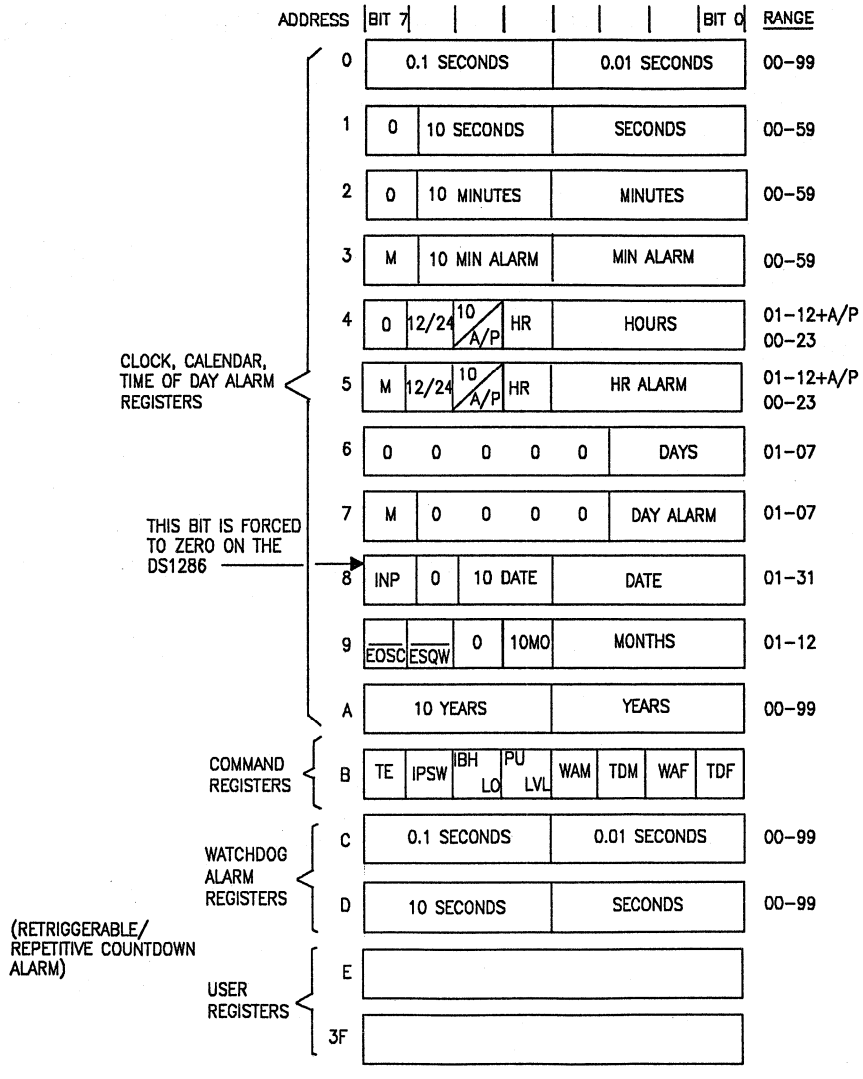
V_{CC} - +5 volt input for connection to the V_{CC} supply. This supply input is used for inputs and outputs only as the internal functions of the device are powered by the V_{BAT} pin. The V_{CC} voltage range should never exceed V_{BAT} by more than 0.3 volts and V_{BAT} is normally connected to V_{CC}. In order to guarantee timing and input/output levels, both V_{CC} and V_{BAT} must be between 4.5 and 5.5 volts. However, the DS1283 maintains internal functions with V_{CC} input as low as 2.5 volts.

RCLR - The RCLR\ pin is used to clear (set to logic 1) all 50 bytes of user nonvolatile RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, RCLR\ must be forced to an input logic 0 (-0.3 to +0.8 volts). The RCLR\ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

INTB - Interrupt B on the DS1283 operates identical to interrupt B on the DS1286 except that the sink and source current is limited to 500 uA. This pin should be pushed up or pulled down if not used.

INTP - Interrupt P on the DS1283 was a missing or no connection pin on the DS1286. This interrupt works in the same manner as INTA\ as programmed by the IPSW bit. However, INTP\ is also logically ORed with the MSB of the date register (see Figure 1). This bit is called the INP bit on the DS1283 and is forced to zero on the DS1286. When the INP bit (interrupt P bit) is set to logical one, interrupt P will be held active low. When INP is set to logical zero, INTP\ is always at the same logic state as INTA\. This pin is an open drain capable of sinking 4 mA.

DS1283 WATCHDOG TIMEKEEPER REGISTERS Figure 1



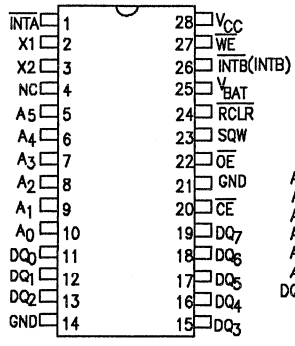
DALLAS SEMICONDUCTOR

DS1284/Q
Watchdog Timekeeper Chip

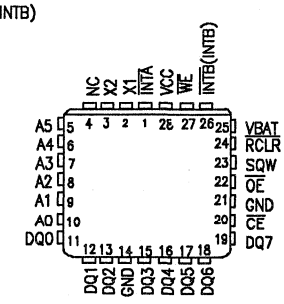
FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25° C
- 50 bytes of user NV RAM
- Optional 28-pin PLCC surface mount package
- Low-power CMOS circuitry is maintained on less than 0.5 uA when power is supplied from battery input

PIN DESCRIPTION



DS1284
28-Pin Dip (600 mil)



DS1284Q
28-Pin PLCC

PIN NAMES (\Denotes Condition Low)

INTA\	- Interrupt Output A
INTB\(INTB)	- Interrupt Output B
A0-A5	- Address Inputs
DQ0-DQ7	- Data Input/Output
CE\	- Chip Enable
OE\	- Output Enable
WE\	- Write Enable
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
SQW	- Square Wave Output
X1,X2	- 32.768 KHz Crystal Connections
V_{BAT}	- +3 Volt Battery Input
RCLR\	- RAM Clear

DESCRIPTION

The DS1284 Watchdog Timekeeper Chip is a self-contained real-time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package or a 28-pin PLCC surface mount package. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1, X2, V_{BAT}, and RCLR\, see the DS1286 Watchdog Timekeeper data sheet.

PIN DESCRIPTION

X1, X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part part no. DT-26S, Seiko part no. DS-VT-200, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6 pF. A trimming capacitor can be used to trim in the oscillator frequency. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

V_{BAT} - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.4 and 4 volts for proper operation. The nominal write protect trip point voltage at which access to registers containing time, watchdog, alarm, and RAM information is denied is set by internal circuitry as 1.26 x V_{BAT}. A maximum load of 0.5 uA at 25°C in the absence of power should be used to size the external energy source. An optional ground pin is provided for connection to battery negative. This pin should be grounded but can be left floating.

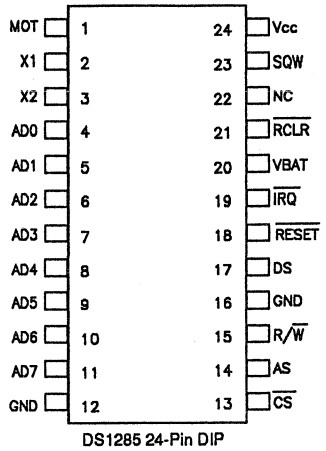
RCLR - The RCLR\ pin is used to clear (set to logic 1) all 50 bytes of user NV RAM but does not affect the registers involved with time, alarm, and watchdog functions. In order to clear the RAM, RCLR\ must be forced to an input logic zero (-0.3 to +0.8 volts) during battery backup mode when V_{CC} is not applied. The RCLR\ function is designed to be used via human interface (shorting to ground or by switch) and not be driven with external buffers. This pin is internally pulled up and should be left floating when not in use.

DALLAS SEMICONDUCTOR

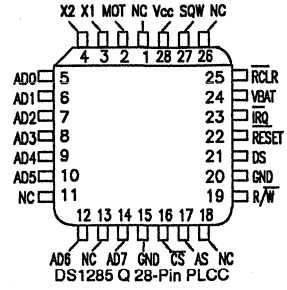
DS1285/Q
Real Time Chip

FEATURES
- Drop-in replacement for IBM AT computer clock/calendar
- Pin configuration closely matches MC146818A
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus compatible interrupt signals (IRQ\)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122us to 500ms
  - End of clock update cycle
- Optional 28-pin PLCC surface mount package

PIN CONNECTIONS



DS1285 24-Pin DIP



DS1285 Q 28-Pin PLCC

PIN NAMES (\ Denotes Condition Low)
AD0-AD7- Multiplexed Address/Data Bus
NC - No Connection
MOT - Bus Type Selection
CS\ - Chip Select
AS - Address Strobe
R/W\ - Read/Write Input
DS - Data Strobe
RESET\ - Reset Input
IRQ\ - Interrupt Request Output
SQW - Square Wave Output
V_{CC} - +5 Volt Supply
GND - Ground
X1,X2 - 32.768 KHz Crystal Connections
V_{BAT} - +3 Volt Battery Input
RCLR\ - RAM Clear

DESCRIPTION
The DS1285 Real Time Chip is a direct replacement for the MC146818A in IBM AT computer clock/calendar and other applications. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. For a complete description of operating conditions, electrical characteristics, bus timing, and pin descriptions other than X1,X2, V_{BAT}, and RCLR\, see the DS1287 data sheet.

PIN DESCRIPTION

X1,X2 - Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S, or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. A variable triming capacitor may be required for extremely high precision timekeeping applications. Crystals can be ordered from Dallas Semiconductor. Order part number DS9032.

V_{BAT} - Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2.5 and 4 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.26 x V_{BAT}. A maximum load of .5uA at 25°C in the absence of power should be used to size the external energy source.

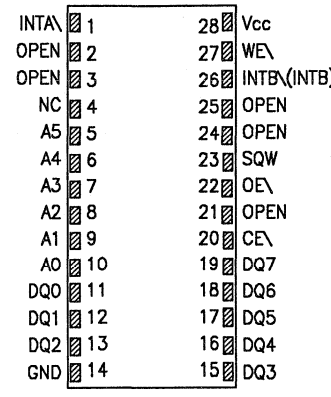
RCLR - The RCLR\ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, RCLR\ must be forced to an input logic 0 (-0.3 to +0.8 volts) during battery back-up mode when V_{CC} is not applied. The RCLR\ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. This pin is internally pulled up.

DALLAS SEMICONDUCTOR

DS1286
Watchdog Timekeeper

FEATURES
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real time-related activities
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs maintain 28-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ± 1 minute/month at 25° C
- Greater than 10 years of timekeeping in the absence of Vcc
- 50 bytes of user NV RAM

PIN DESCRIPTION



28-Pin Encapsulated Package (740 Mil Flush)

PIN NAMES (\ Indicates Condition Low)

INTA\	- Interrupt Output A
INTB\(INTB)	- Interrupt Output B
A0-A5	- Address Inputs
DQ0-DQ7	- Data Input/Output
CE\	- Chip Enable
OE\	- Output Enable
WE\	- Write Enable
Vcc	- +5 Volts
GND	- Ground
NC	- No Connection
OPEN	- Pin Missing
SQW	- Square Wave Output

DESCRIPTION

The DS1286 Watchdog Timekeeper is a self-contained real time clock, alarm, watchdog timer, and interval timer in a 28-pin JEDEC DIP package. The DS1286 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 64 eight-bit registers can be read or written in the same manner as byte-wide static RAM. Data is maintained in the Watchdog Timekeeper by intelligent control circuitry which detects the status of Vcc and write protects memory when Vcc is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of Vcc. Watchdog Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The Watchdog Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

OPERATION - READ REGISTERS

The DS1286 executes a read cycle whenever WE\ (Write Enable) is inactive (High) and CE\ (Chip Enable) and OE\ (Output Enable) are active (Low). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within t_{Acc} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the latter occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

OPERATION - WRITE REGISTERS

The DS1286 is in the write mode whenever the WE\ (Write Enable) and CE\ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of CE\ or WE\. The OE\ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active), then WE\ will disable the outputs in t_{ODW} from its falling edge.

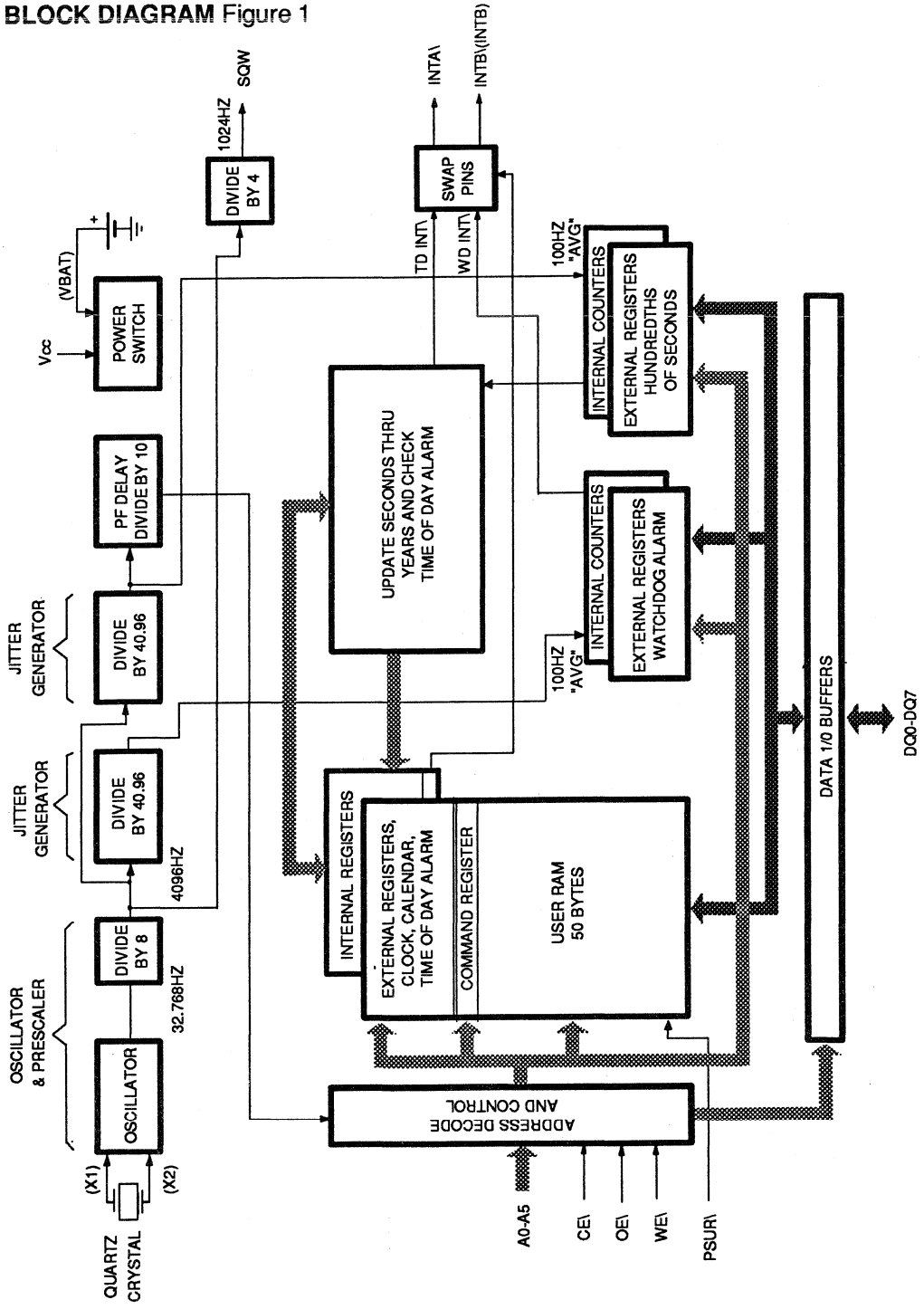
DATA RETENTION

The Watchdog Timekeeper provides full functional capability when Vcc is greater than 4.5 volts and write protects the register contents at 4.25 volts typical. Data is maintained in the absence of Vcc without any additional support circuitry. The DS1286 constantly monitors V_{CC}. Should the supply voltage decay, the Watchdog TimeKeeper will automatically write protect itself and all inputs to the registers become Don't Care. The two interrupts INTA\ and INTB\ (INTB) and the internal clock and timers continue to run regardless of the level of Vcc. As Vcc falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc and disconnects the internal lithium energy source. Normal operation can resume after Vcc exceeds 4.5 volts for a period of 150 ms.

WATCHDOG TIMEKEEPER REGISTERS

The Watchdog Timekeeper has 64 registers which are eight bits wide that contain all of the Timekeeping, Alarm, Watchdog, Control, and Data information. The Clock, Calendar, Alarm, and Watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 50 bytes of RAM registers can only be accessed from the external address and data bus. Registers 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of Day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm registers and information which is stored in these two registers is in BCD. Registers E through 3F are user bytes and can be used to contain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, EOSC\ (bit 7) enables the Real Time Clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (Pin 23). When set to logic zero, the Square Wave Output pin will output a 1024 Hz Square Wave Signal. When set to logic one the Square Wave Output pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12- or 24- Hour Select Bit. When set to logic one, the 12 Hour Format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic one being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours). The Time of Day registers are updated every .01 seconds from the real time clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the Watchdog Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable) to a logic zero. This will freeze the External Time of Day registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day registers back to being updated every .01 second. No time is lost in the real time clock because the internal copy of the Time of Day register buffers is continually incremented while the external memory registers are frozen.

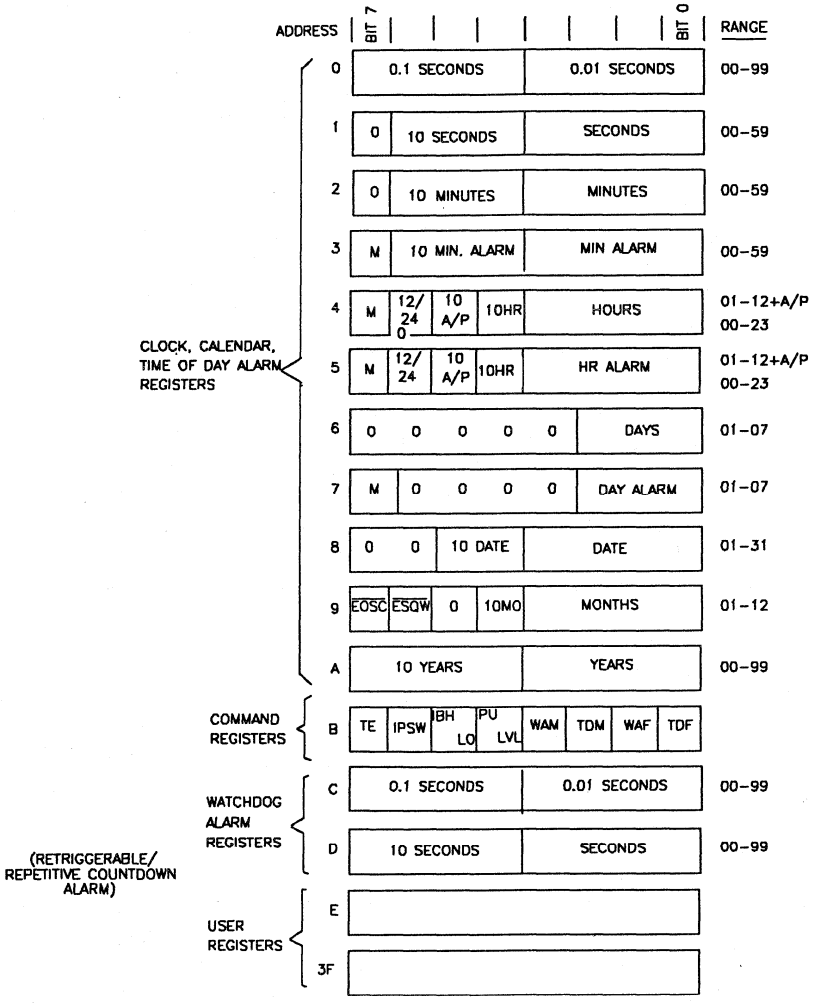
An alternate method of reading and writing the Time of Day registers is to ignore synchronization. However, any single read may give erroneous data as the real time clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented and Time of Day Alarm is checked during the period that hundreds of seconds read 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the Watchdog Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm registers are written and read in the same format as the Time of Day registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm registers are read or written.

DS1286 WATCHDOG TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

MINUTES	HOURS	DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Registers C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer countdown is interrupted and reinitialized back to the entered value every time either of the registers is accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm registers always read the entered value. The actual countdown register is internal and is not readable. Writing Registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logic one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm registers. However, if the transfer enable bit is set to logic zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logic one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Watchdog Alarm registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logic one, the Time of Day Alarm Interrupt Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logic zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask bit (WAM). When this bit is written to a logic one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm registers. When WAM\ is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins INTA\ and INTB\ (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If Bit 4 is set to logic one, the pulse mode is selected and INTA\ will sink current for a minimum of 3 ms and then release. Output INTB\ (INTB) will either sink or source current for a minimum of 3 ms depending on the level of bit 5. When bit 5 is set to logic one, the B interrupt will source current. When bit 5 is set to logic zero, the B interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins INTA\ or INTB\(INTB). When set to logic one, INTA\ becomes the Time of Day Alarm Interrupt pin and INTB\(INTB) becomes the Watchdog Interrupt pin. When bit 6 is set to logic zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on INTB\(INTB) and the Watchdog Interrupt will be output on INTA\. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day registers.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +125°C
Soldering Temperature 260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0° C to 70° C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{CC}	4.5	5.0	5.5	V	10
INPUT LOGIC 1	V_{IH}	2.2		V_{CC} + 0.3	V	10
INPUT LOGIC 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS (0° C to 70° C, Vcc =5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT	I_{IL}	-1.0		+1.0	uA	
OUTPUT LEAKAGE CURRENT	I_{LO}	-1.0		+1.0	uA	
I/O LEAKAGE CURRENT	I_{LIO}	-1.0		+1.0	uA	
OUTPUT CURRENT @ 2.4V	I_{OH}	-1.0			mA	
OUTPUT CURRENT @ 0.4V	I_{OL}	2.0			mA	13
STANDBY CURRENT CE\ = 2.2V	I_{CCS1}		3.0	7.0	mA	
STANDBY CURRENT CE\ > Vcc -0.5	I_{CCS2}			4.0	mA	
ACTIVE CURRENT	I_{CC}			15	mA	
WRITE PROTECTION VOLTAGE	V_{TP}		4.25		V	

CAPACITANCE

(t_A=25° C)

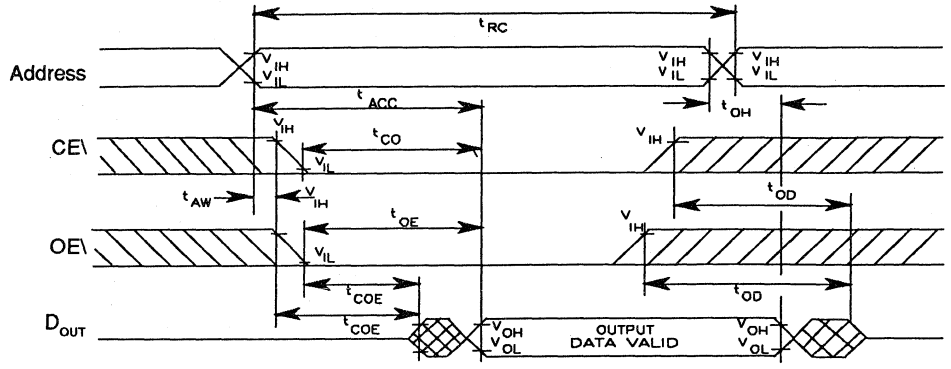
PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
INPUT CAPACITANCE	C_{IN}	7	10	pF	
OUTPUT CAPACITANCE	C_{OUT}	7	10	pF	
INPUT/OUTPUT CAPACITANCE	$C_{I/O}$	7	10	pF	

AC ELECTRICAL CHARACTERISTICS

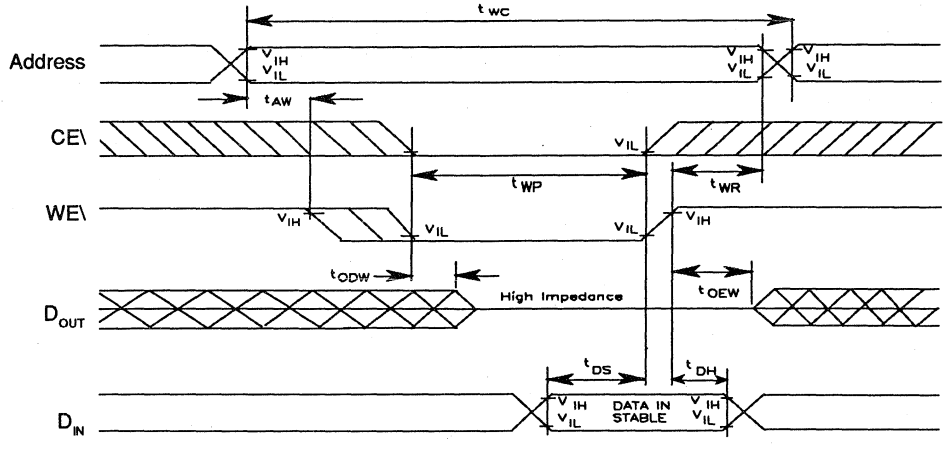
(0° C to 70° C, Vcc = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
READ CYCLE TIME	t_{RC}	150			ns	1
ADDRESS ACCESS TIME	t_{ACC}			150	ns	
CE\ ACCESS TIME	t_{CO}			150	ns	
OE\ ACCESS TIME	t_{OE}			60	ns	
OE\ OR CE\ TO OUTPUT ACTIVE	t_{COE}	10			ns	
OUTPUT HIGH Z FROM DESELECT	t_{OD}			60	ns	
OUTPUT HOLD FROM ADDRESS CHANGE	t_{OH}	10			ns	
WRITE CYCLE TIME	t_{WC}	150			ns	
WRITE PULSE WIDTH	t_{WP}	140			ns	3
ADDRESS SETUP TIME	t_{AW}	0			ns	
WRITE RECOVERY TIME	t_{WR}	10			ns	
OUTPUT HIGH Z FROM WE\	t_{ODW}			50	ns	
OUTPUT ACTIVE FROM WE\	t_{OEW}	10			ns	
DATA SETUP TIME	t_{DS}	45			ns	4
DATA HOLD TIME	t_{DH}	0			ns	4,5
INTA\, INTB\ PULSE WIDTH	t_{IPW}	3			ms	11,12

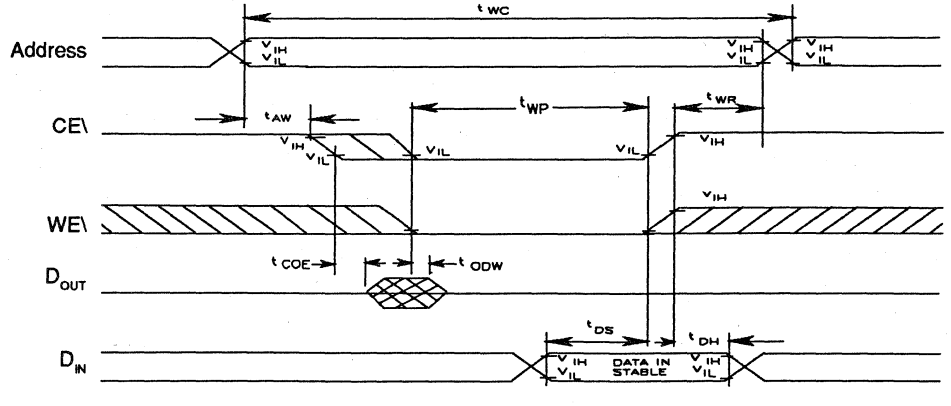
READ CYCLE (Note1)



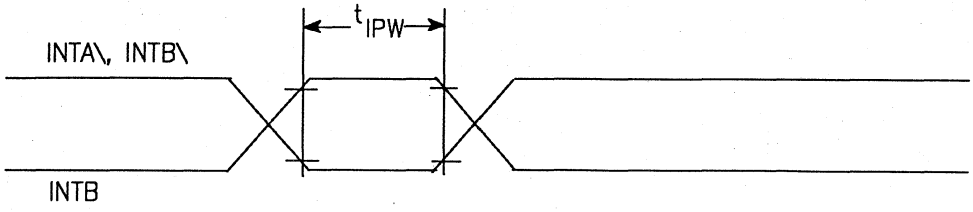
WRITE CYCLE 1 (Notes 2, 6, 7)



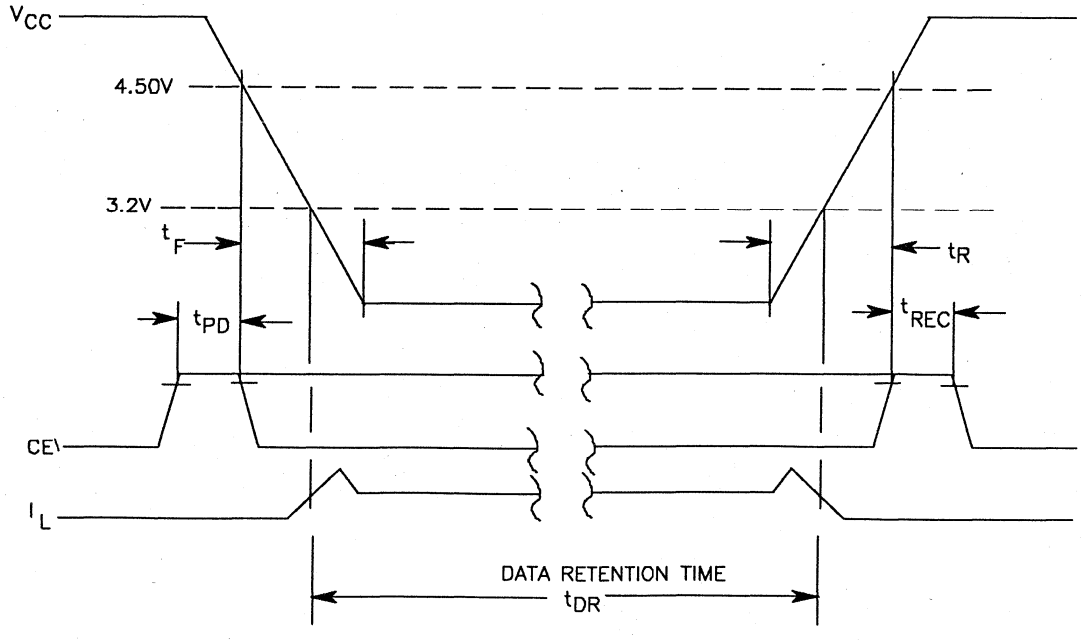
WRITE CYCLE 2 (Notes 2, 8)



TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-DOWN/POWER-UP CONDITION



CURRENT, I_L SUPPLIED FROM LITHIUM CELL

POWER-UP/POWER-DOWN CONDITION

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	350		us	
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	100		us	
t_{REC}	CE\ at V_{IH} after Power Up		150	ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. WE\ is high for a read cycle.
2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.
4. t_{DS} or t_{DH} are measured from the earlier of CE\ or WE\ going high.
5. t_{DH} is measured from WE\ going high. If CE\ is used to terminate the write cycle, then t_{DH} = 20 ns.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.
8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1286 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both INTA\ and INTB\(INTB) are open drain outputs.

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

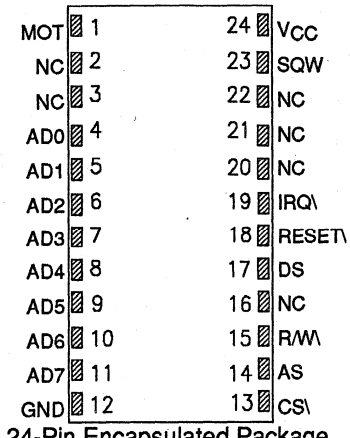
DALLAS SEMICONDUCTOR

DS1287
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - -14 bytes of clock and control registers
  - -50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ\)
- Three interrupts are separately software-maskable and testable
  - -Time-of-day alarm once/second to once/day
  - -Periodic rates from 122 us to 500 ms
  - -End of clock update cycle

PIN DESCRIPTION



24-Pin Encapsulated Package
(740 Mil Flush)

PIN NAMES(\Denotes Condition Low)

AD0 - AD7	-Multiplexed Address/ Data Bus
NC	- No Connection
MOT	- Bus Type Selection
CS\	- Chip Select
AS	- Address Strobe
R/W\	- Read/Write Input
DS	- Data Strobe
RESET\	- Reset Input
IRQ\	- Interrupt Request Output
SQW	- Square Wave Output
V_{CC}	- +5 Volt Supply
GND	- Ground

DESCRIPTION

The DS1287 Real Time Clock is designed to be a direct replacement for the MC146818A. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1287. The following paragraphs describe the function of each pin.

POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar ,and alarm memory locations remain nonvolatile regardless of the level of the V_{CC} input. When V_{CC} is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When V_{CC} falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of CS\ at the input pin. The DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When V_{CC} falls below a level of approximately 3 volts, the external V_{CC} supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

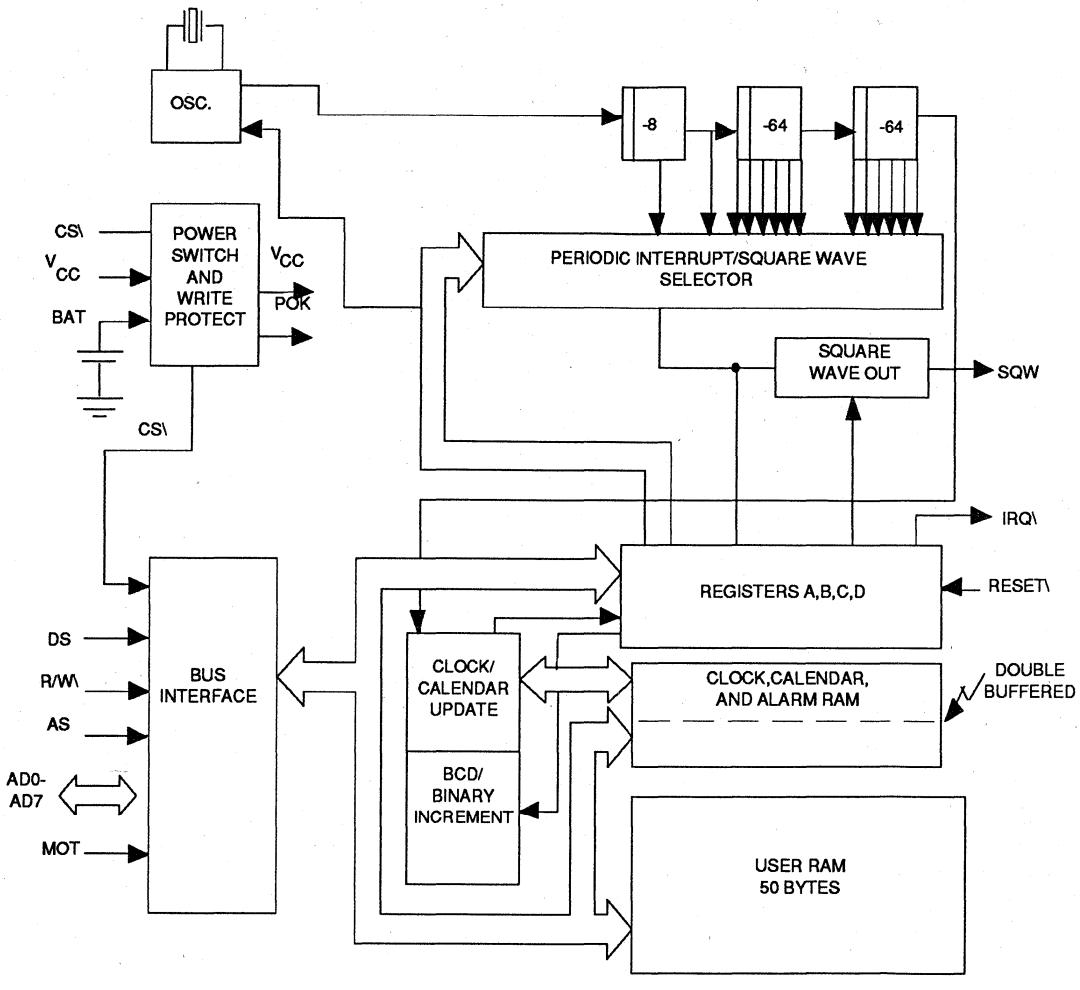
SIGNAL DESCRIPTIONS

GND, V_{CC} - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts are applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below 4.25 volts typical, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below 3 volts typical, the RAM and timekeeper are switched over to an internal lithium energy source. The timekeeping function maintains an accuracy of ±1 minute per month at 25°C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 Kohms.

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin can be changed by programming Register A as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than 4.25 volts typical.

BLOCK DIAGRAM DS1287 Figure 1



PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 1

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 us	8.192 KHz
0	1	0	0	244.141 us	4.096 KHz
0	1	0	1	488.281 us	2.048 KHz
0	1	1	0	976.5625 us	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bidirectional Address/Data Bus) - Multiplexed buses save pins because address information and data information time share the same signal paths. The addresses are present during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the DS1287 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the DS1287 latches the address from AD0 to AD5. Valid write data must be present and held stable during the latter portion of the DS or WR\ pulses. In a read cycle the DS1287 outputs 8 bits of data during the latter portion of the DS or RD\ pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD\ transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the DS1287.

DS (Data Strobe or Read Input) - The DS/RD\ pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the DS1287 is to drive the bidirectional bus. In write cycles the trailing edge of DS causes the DS1287 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read(RD\). RD\ identifies the time period when the DS1287 drives the bus with read data. The RD\ signal is the same definition as the Output Enable (OE\) signal on a typical memory.

R/W\ (Read/Write Input)-The R/W\ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/W\ is at a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/W\ while DS is high. A write cycle is indicated when R/W\ is low during DS.

When the MOT pin is connected to GND for Intel timing, the R/W\ signal is an active low signal called WR\. In this mode the R/W\ pin has the same meaning as the Write Enable signal (WE\) on generic RAMs.

CS\ (Chip Select Input) - The Chip Select signal must be asserted low for a bus cycle in the DS1287 to be accessed. CS\ must be kept in the active state during DS and AS for Motorola timing and during RD\ and WR\ for Intel timing. Bus cycles which take place without asserting CS\ will latch addresses but no access will occur. When V_{CC} is below 4.25 volts, the DS1287 internally inhibits access cycles by internally disabling the CS\ input. This action protects both the real time clock data and RAM data during power outages.

IRQ\ (Interrupt Request Output) - The IRQ\ pin is an active low output of the DS1287 that can be used as an interrupt input to a processor. The IRQ\ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the IRQ\ pin the processor program normally reads the C register. The RESET\ pin also clears pending interrupts.

When no interrupt conditions are present, the IRQ\ level is in the high impedance state. Multiple interrupting devices can be connected to an IRQ\ bus. The IRQ\ bus is an open drain output and requires an external pull-up resistor.

RESET\ (Reset Input) - The RESET\ pin has no effect on the clock, calendar, or RAM. On power-up the RESET\ pin can be held low for a time in order to allow the power supply to stabilize. The amount of time that RESET\ is held low is dependent on the application. However, if RESET\ is used on power-up, the time RESET\ is low should exceed 200 ms to make sure that the internal timer that controls the DS1287 on power-up has timed out. When RESET\ is low and V_{CC} is above 4.25 volts, the following occurs:

A. Periodic Interrupt Enable (PEI) bit is cleared to zero.
B. Alarm Interrupt Enable (AIE) bit is cleared to zero.
C. Update Ended Interrupt Flag (UF) bit is cleared to zero.
D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.
E. Periodic Interrupt Flag (PF) bit is cleared to zero.
F. The device is not accessible until RESET\ is returned high.
G. Alarm Interrupt Flag (AF) bit is cleared to zero.
H. IRQ\ pin is in the high impedanc state.
I. Square Wave Output Enable (SQWE\) bit is cleared to zero.
J. Update Ended Interrupt Enable (UIE) is cleared to zero.

In a typical application RESET\ can be connected to V_{CC}. This connection will allow the DS1287 to go in and out of power fail without affecting any of the control registers.

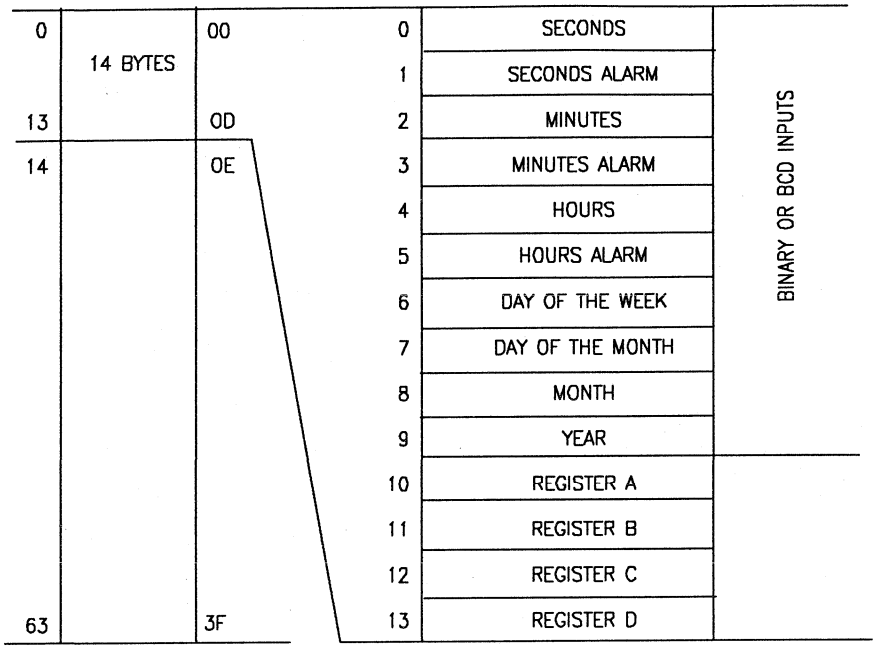
ADDRESS MAP

The address map of the DS1287 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar, and alarm data, and four bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

1. Registers C and D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds byte is read-only.

The contents of four registers (A,B,C, and D) are described in the "Registers" section.

ADDRESS MAP DS1287 Figure 2



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a logic one to prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar, and alarm bytes must use the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

TIME, CALENDAR AND ALARM DATA MODES Table 2

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours-12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours-24-hr Mode	0-23	00-17	00-23
5	Hours Alarm-12-hr	1-12	01-0C AM, 81-8C PM	01-12AM,81-92PM
	Hours Alarm-24-hr	0-23	00-17	00-23
6	Day of the Week Sunday = 1	1-7	01-07	01-07
7	Date of the Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the DS1287. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500 ms to 122 us. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A zero in an interrupt-enable bit prohibits the IRQ\ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, IRQ\ is immediately set at an active level, although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the IRQ\ pin is asserted low. IRQ\ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a one whenever the IRQ\ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS1287. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the DS1287 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the IRQ\ pin to go to an active state from once every 500 ms to once every 122 us. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

The DS1287 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a

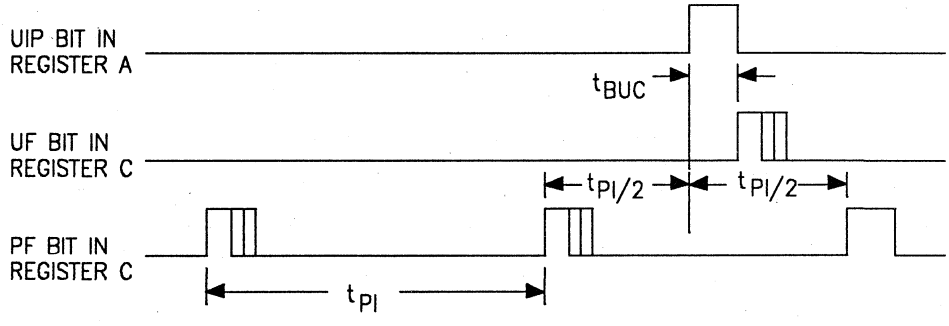
"don't care" code is present in all three positions.

There are three methods that can handle access of the real time clock that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates that over 999 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 us later. If a low is read on the UIP bit, the user has at least 244 us before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 us.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($TPI/2+t_{BUC}$) to ensure that data is not read during the update cycle.

UPDATE-ENDED AND PERIODIC INTERRUPT RELATIONSHIP Figure 3



t_{PI} = Periodic interrupt time interval per Table 1.
t_{BUC} = Delay time before update cycle = 244 us.

REGISTERS

The DS1287 has four control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP
The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a one, the update transfer will soon occur. When UIP is a zero, the update transfer will not occur for at least 244 us. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RESET\. Writing the SET bit in Register B to a one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2
These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of 010 is written to DV0, DV1, and DV2.

RS3, RS2, RS1, RS0
These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/ or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;

2. Enable the SQW output pin with the SQWE bit;

3. Enable both at the same time and the same rate; or

4. Enable neither.

Table 1 lists the periodic interrupt rates and the square wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by RESET\.

REGISTER B

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET
When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit that is not modified by RESET\ or internal functions of the DS1287.

PIE
The periodic interrupt enable PIE bit is a read/ write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to drive the IRQ\ pin low. When the PIE bit is set to one, periodic interrupts are generated by driving the IRQ\ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the IRQ\ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal DS1287 functions, but is cleared to zero on RESET\.

AIE
The Alarm Interrupt Enable (AIE) bit is a read/ write bit which, when set to a one, permits the Alarm Flag (AF) bit in register C to assert IRQ\. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ\ signal. The RESET\ pin clears AIE to zero. The internal functions of the DS1287 do not affect the AIE bit.

UIE
The Update Ended Interrupt Enable (UIE) bit is a read/write that enables the Update End Flag (UF) bit in Register C to assert IRQ\. The RESET\ pin going low or the SET bit going high clears to UIE bit.

SQWE
When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on a SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the RESET\ pin. SQWE is a read/write bit.

DM
The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET\. A one in DM signifies binary data while a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12
The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions of RESET\.

DSE
The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 am to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET\.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF
The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PFxPIE + AFxAIE + UFxUIE.

Any time the IRQF bit is a one, the IRQ\ pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET\ pin is low.

PF
The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are ones, the IRQ\ signal is active and will set the IRQF bit. The PF bit is cleared by a RESET\ or a software read of Register C.

AF
A one in the Alarm Interrupt Flag (AF) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ\ pin will go low and a one will appear in the IRQF bit. A RESET\ or a read of Register C will clear AF.

UF
The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in UF causes the IRQF bit to be a one which will assert the IRQ\ pin. UF is cleared by reading Register C or a RESET\.

BIT 0 THROUGH BIT 3
These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
VRT	0	0	0	0	0	0	0

VRT
The Valid RAM and Time (VRT) bit is set to the one state by Dallas Semiconductor prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by RESET\.

BIT 6 THROUGH BIT 0
The remaining bits of Register D are not usable. They cannot be written and, when read, they will always read zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	I_{CC1}		7	15	mA	2
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
I/O Leakage	I_{LO}	-1.0		+1.0	uA	4
Input Current	I_{MOT}	-1.0		+500	uA	3
Output @ 2.4V	I_{OH}	-1.0			mA	1,5
Output @ 0.4V	I_{OL}			4.0	mA	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

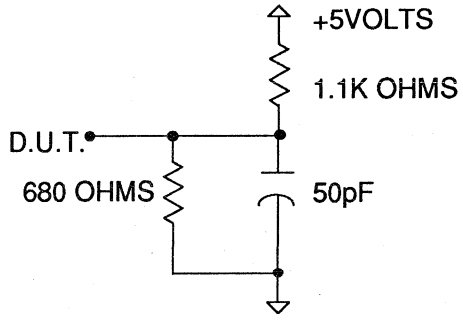
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

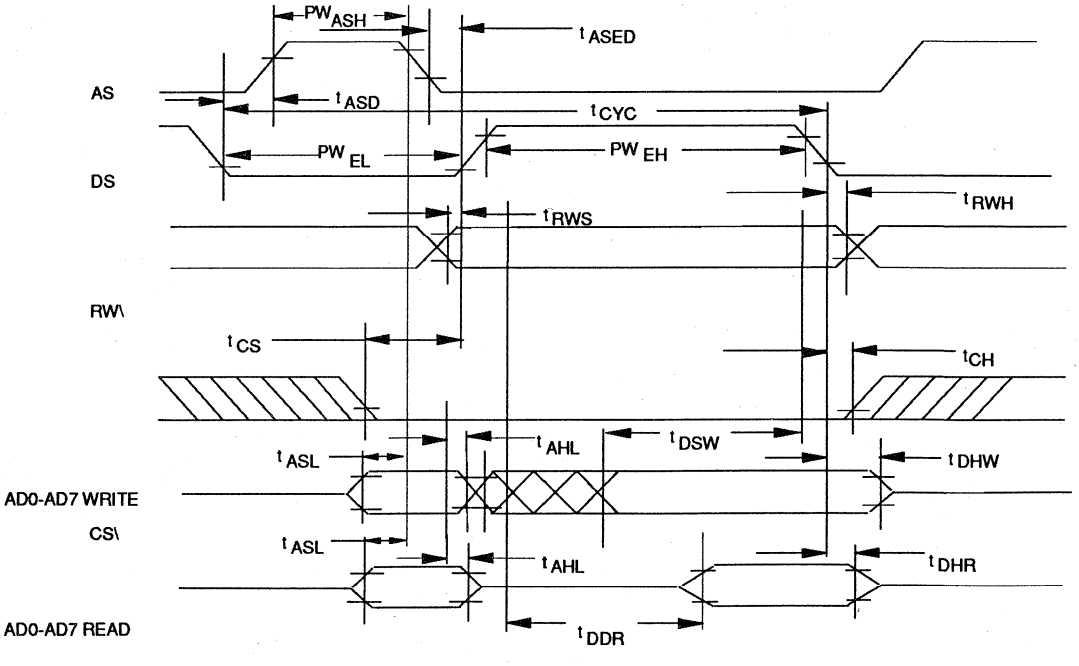
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	385		DC	ns	
Pulse Width, DS/E Low or RD/WR High	PW_{EL}	150			ns	
Pulse Width, DS/E High or RD/WR Low	PW_{EH}	125			ns	
Input Rise and Fall Time	t_R,t_F			30	ns	
R/W Hold Time	t_{RWH}	10			ns	
R/W Setup Time Before DS/E	t_{RWS}	50			ns	
Chip Select Setup Time Before DS, WR, or RD	t_{CS}	20			ns	
Chip Select Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		80	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	30			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS/E to AS/ALE Rise	t_{ASD}	25			ns	
Pulse Width AS/ALE High	PW_{ASH}	60			ns	
Delay Time, AS/ALE to DS/E Rise	t_{ASED}	40			ns	
Output Data Delay Time From DS/E or RD	t_{DDR}	20		120	ns	6
Data Setup Time	t_{DSW}	100			ns	
Reset Pulse Width	t_{RWL}	5			us	
IRQ\ Release from DS	t_{IRDS}			2	us	
IRQ\ Release from RESET\	t_{IRR}			2	us	

NOTES:
1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pulldown of 20K ohms.
4. Applies to the AD0-AD7 pins, the IRQ\ pin,and the SQW pin when each is in the high impedance state.
5. The IRQ\ pin is open drain.
6. Measured with a load as shown in Figure 4.

OUTPUT LOAD Figure 4

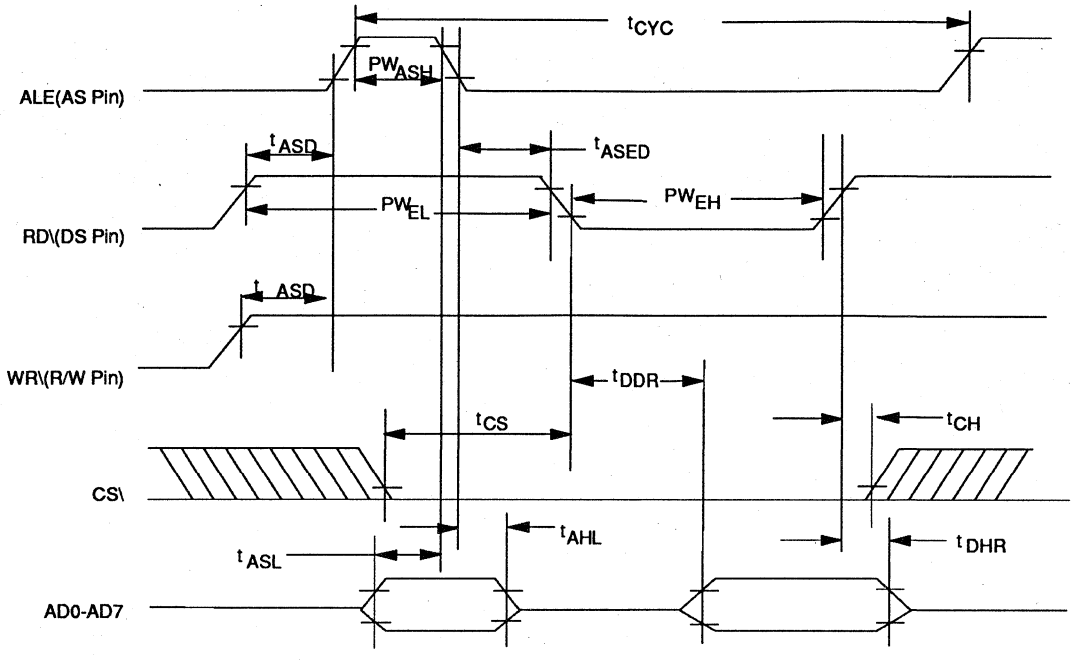


DS1287 BUS TIMING FOR MOTOROLA INTERFACE



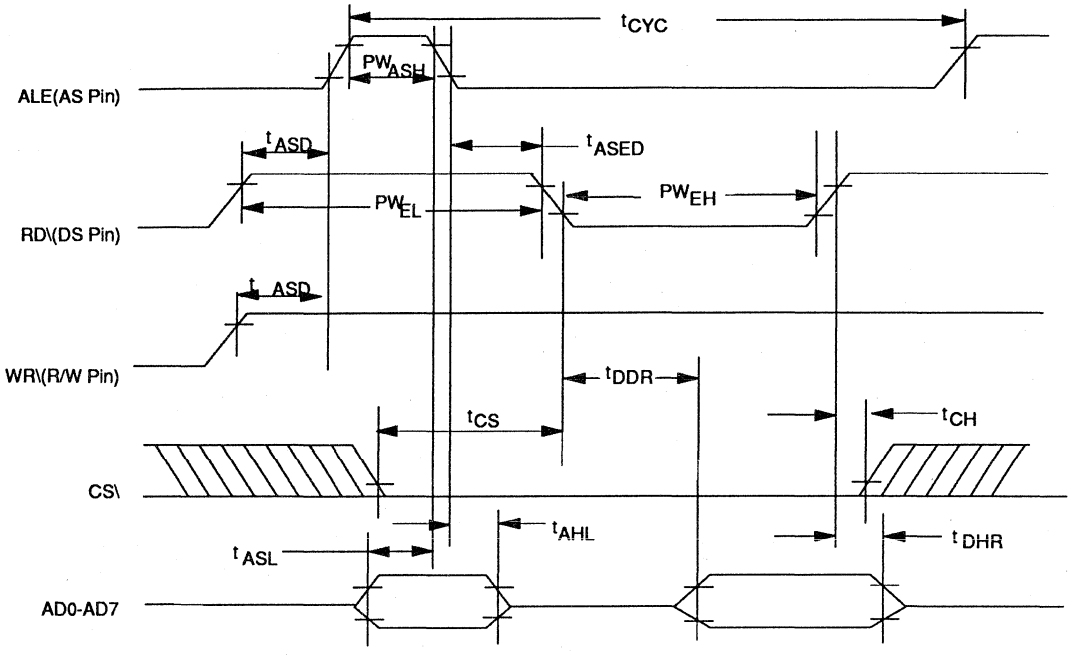
NOTE:
Input Levels = 0.8 volts and 2.2 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 BUS TIMING FOR INTEL INTERFACE WRITE CYCLE



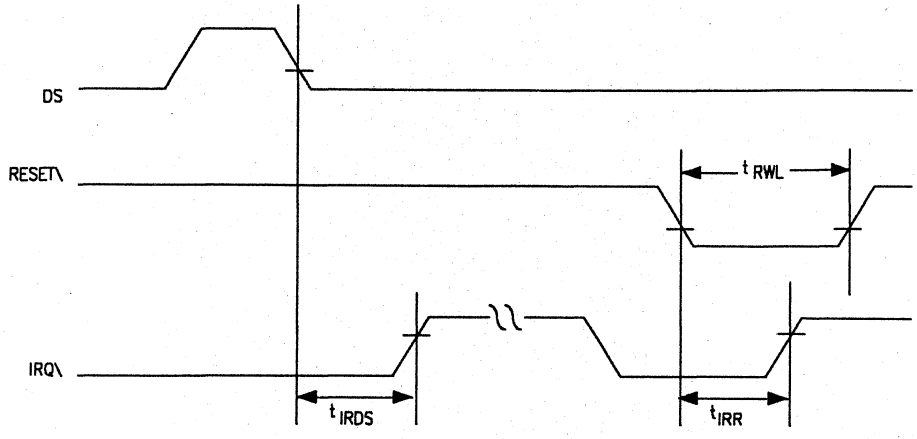
NOTE:
Input Levels = 0.8 volts and 2.2 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 BUS TIMING FOR INTEL INTERFACE READ CYCLE



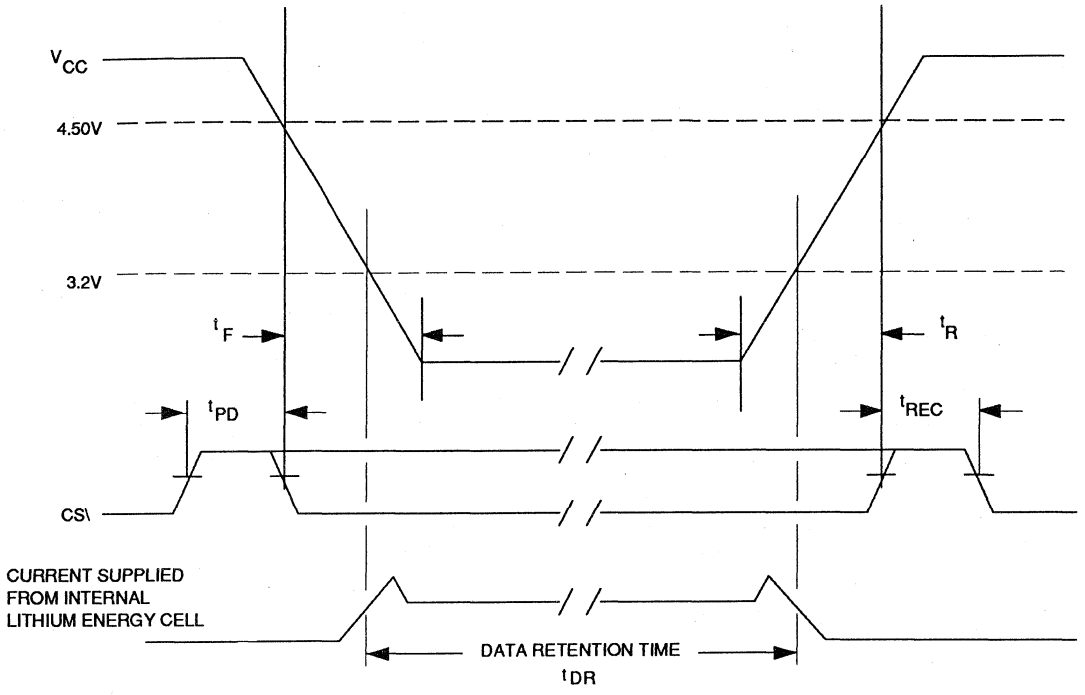
NOTE:
Input Levels = 0.8 volts and 2.2 volts.
Output Levels = 0.4 volts and 2.4 volts.

DS1287 IRQ\ RELEASE DELAY TIMING



NOTE:
Input Levels = 0.8 volts and 2.2 volts.
Output Levels = 0.4 volts and 2.4 volts.

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} slew from 4.5V to 0V(CE\ at V_{IH})	300		us	
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	100		us	
t_{REC}	CE\ at V_{IH} after Power-Up	20	200	ms	

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention	10		years	

NOTE:
The real time clock will keep time to an accuracy of ± 1 minute per month during data retention time for the period of t_{DR}.

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

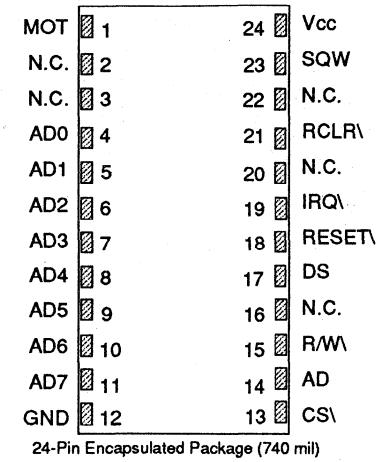
DALLAS SEMICONDUCTOR

DS1287A
Real Time Clock

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin-compatible with the MC146818
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month and year with leap year compensation
- Binary or BCD representation of time, calendar and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ\)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 us to 500 ms
  - End-of-clock update cycle

PIN DESCRIPTION



24-Pin Encapsulated Package (740 mil)

PIN NAMES (\ Denotes Condition Low)

AD0-AD7	-Multiplexed Address/Data Bus
NC	-No Connect
MOT	-Bus Type Selection
CS\	-Chip Select
AS	-Address Strobe
R/W\	-Read/Write Input
DS	-Data Strobe
RESET\	-Reset Input
IRQ\	-Interrupt Request Output
SQW	-Square Wave Output
V_{CC}	-+5 Volt Supply
GND	-Ground
RCLR\	-RAM Clear

NOTE

The RCLR\ pin is used to clear (set to logic 1) all 50 bytes of general purpose RAM but does not affect the RAM associated with the Real Time Clock. In order to clear the RAM, RCLR\ must be forced to an input logic zero (-0.3 to +0.8 volts) during battery backup mode when V_{CC} is not applied. The RCLR\ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. All other operations, descriptions and specifications are identical to the DS1287 Real Time Clock.

DALLAS SEMICONDUCTOR

DS1385
RAMified Real Time Chip 4K x 8

FEATURES

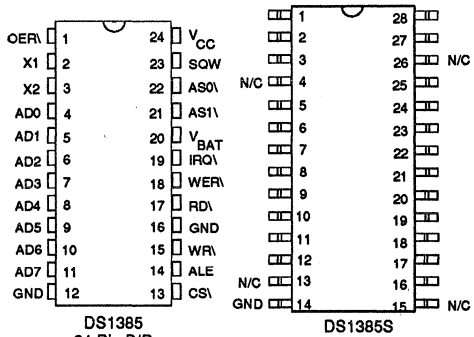
- Drop-in replacement for IBM AT computer clock/calendar
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
  - Separate 4K x 8 SRAM accessible by using RAM control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ\)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 us to 500 ms
  - End-of-clock update cycle
- Real time chip compatible with DS1285 Real Time Chip

DESCRIPTION

The main elements of the DS1385 RAMified Real Time Chip are the real time clock (RTC) and a 4K X 8 static RAM (SRAM) with interface latches (see Figure 1).

For PIN descriptions for X_1, X_2, crystal spec, and battery see DS1202 Serial Timekeeper Chip data sheet.

PIN DESCRIPTION



DS1385
24-Pin DIP
(600 mil)

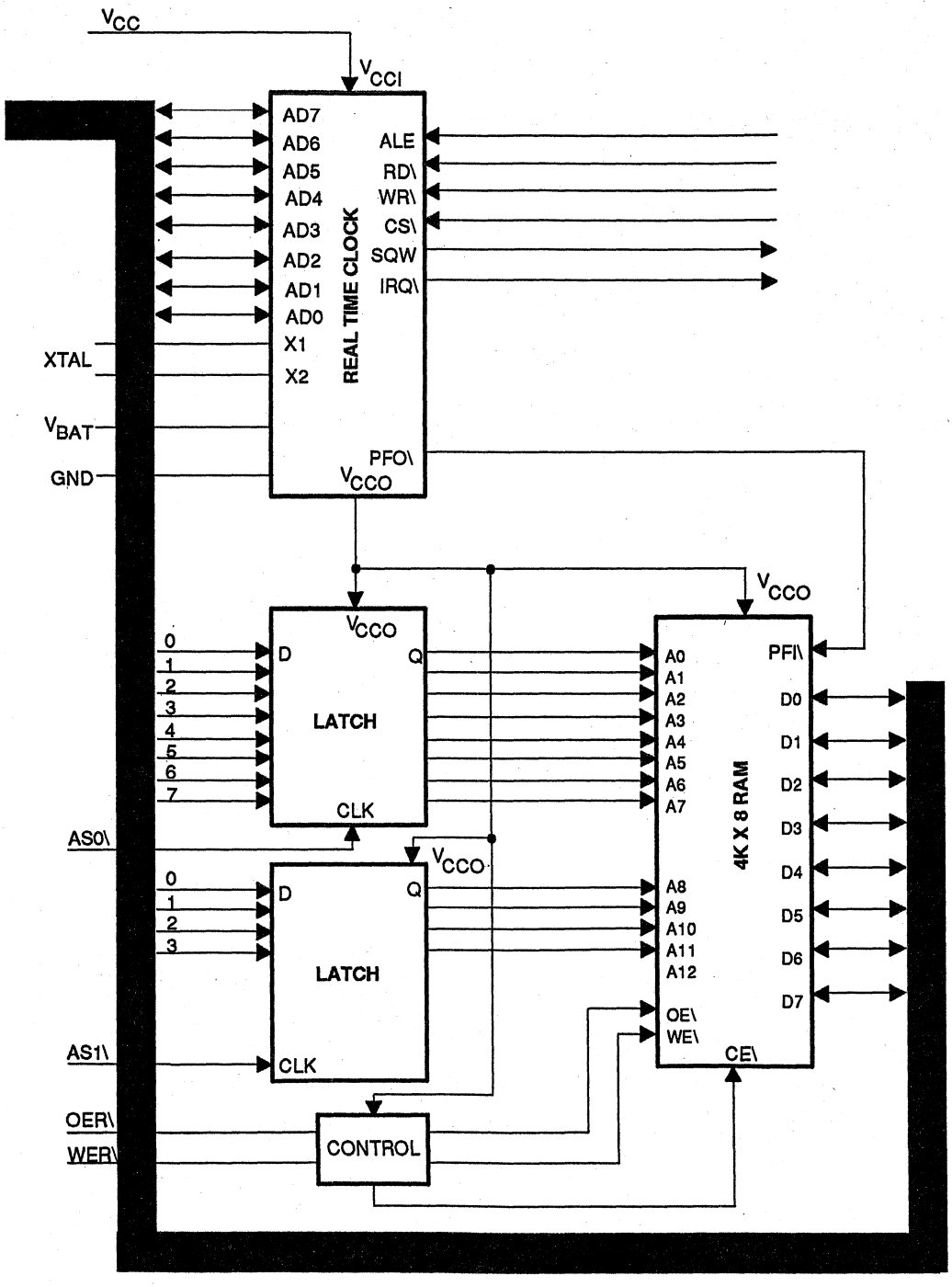
DS1385S
28-Pin SOIC
(330 mil)

PIN NAMES(\ Denotes Condition Low)

SIGNAL	DESCRIPTION
OER\	RAM Output Enable
X1	32.768 KHz Crystal
X2	Connection
AD0-AD7	Multiplexed Address/ Data Bus
GND	Ground
CS\	RTC Chip Select
ALE	RTC Address Strobe
WR\	RTC Write Strobe
GND	Ground, Battery
RD\	RTC Data Strobe
WER\	RAM Write Enable
IRQ\	Interrupt Request Output
V_{BAT}	Battery
AS1\	RAM Address Strobe
AS0\	RAM Address Strobe
SQW	Square Wave Output
V_{CC}	+5 Volt Supply
N/C	No Connect

See the DS1387 RAMified Real Time Clock data sheet for description and specifications.

DS1385 BLOCK DIAGRAM Figure 1

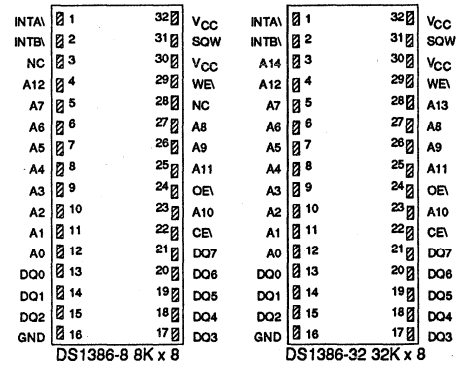


DALLAS SEMICONDUCTOR

DS1386
RAMified Timekeeper

FEATURES
- 8K or 32K bytes of user NV RAM
- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Watchdog timer restarts an out-of-control processor
- Alarm function schedules real-time related activities
- Embedded lithium energy cell maintains time, watchdog, user RAM, and alarm information
- Programmable interrupts and square wave outputs maintain 32-pin JEDEC footprint
- All registers are individually addressable via the address and data bus
- Accuracy is better than ±1 minute/month at 25° C
- Greater than 10 years of timekeeping in the absence of Vcc
- Interrupt signals active in power-down mode

PIN DESCRIPTION



DS1386-8 8K x 8
32-Pin Encapsulated Package
(740 Mil Extended)

DS1386-32 32K x 8
32-Pin Encapsulated Package
(740 mil Extended)

PIN NAMES (\ Indicates Condition Low)

INTA\	- Interrupt Output A
INTB\(INTB)	- Interrupt Output B
A0-A14	- Address Inputs
DQ0-DQ7	- Data Input/Output
CE\	- Chip Enable
OE\	- Output Enable
WE\	- Write Enable
V_{CC}	- +5 Volts
GND	- Ground
SQW	- Square Wave Output

DESCRIPTION

The DS1386 RAMified Timekeeper is a self-contained real time clock, alarm, watchdog timer, and interval timer in a 32-pin JEDEC DIP package. The DS1386 contains an embedded lithium energy source and a quartz crystal which eliminates the need for any external circuitry. Data contained within 8K or 32K by 8-bit registers can be read or written in the same manner as bytewide static RAM. Data is maintained in the RAMified Timekeeper by intelligent control circuitry which detects the status of Vcc and write protects memory when Vcc is out of tolerance. The lithium energy source can maintain data and real time for over ten years in the absence of Vcc. RAMified Timekeeper information includes hundredths of seconds, seconds, minutes, hours, day, date, month, and year. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap year. The RAMified Timekeeper operates in either 24 hour or 12 hour format with an AM/PM indicator. The watchdog timer provides alarm windows and interval timing between 0.01 seconds and 99.99 seconds. The real time alarm provides for preset times of up to one week.

OPERATION - READ REGISTERS

The DS1386 executes a read cycle whenever WE\ (Write Enable) is inactive (High) and CE\ (Chip Enable) and OE\ (Output Enable) are active (Low). The unique address specified by the six address inputs (A0-A5) defines which of the 64 registers is to be accessed. Valid data will be available to the eight data output drivers within t_{Acc} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the latter occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

OPERATION - WRITE REGISTERS

The DS1386 is in the write mode whenever the WE\ (Write Enable) and CE\ (Chip Enable) signals are in the active (Low) state after the address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery state (t_{WR}) before another cycle can be initiated. Data must be valid on the data bus with sufficient Data Set-Up (t_{DS}) and Data Hold Time (t_{DH}) with respect to the earlier rising edge of CE\ or WE\. The OE\ control signal should be kept inactive (High) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active), then WE\ will disable the outputs in t_{ODW} from its falling edge.

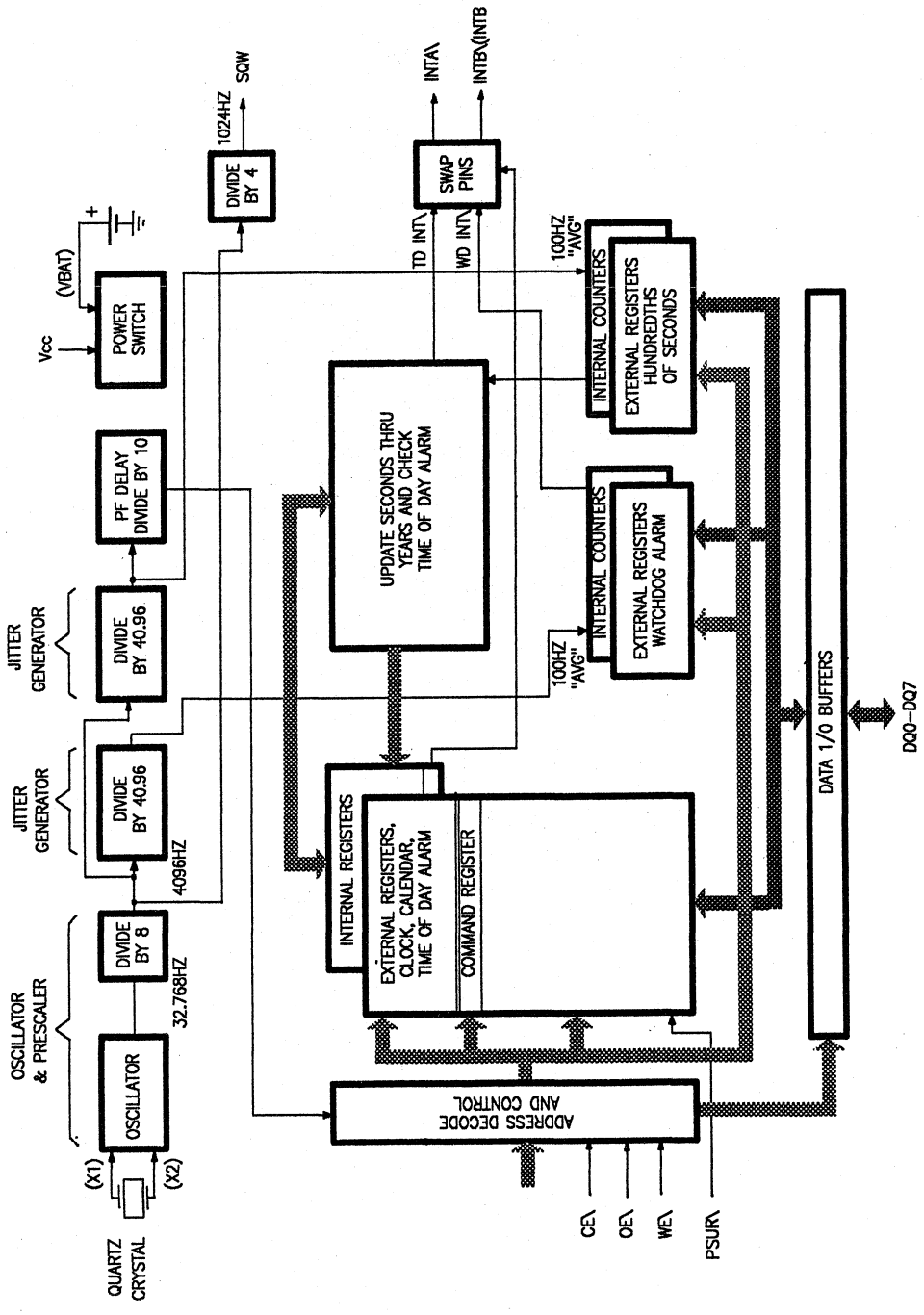
DATA RETENTION

The RAMified Timekeeper provides full functional capability when Vcc is greater than 4.5 volts and write-protects the register contents at 4.25 volts typical. Data is maintained in the absence of Vcc without any additional support circuitry. The DS1386 constantly monitors Vcc. Should the supply voltage decay, the RAMified Timekeeper will automatically write-protect itself and all inputs to the registers become Don't Care. The two interrupts INTA\ and INTB\ (INTB) and the internal clock and timers continue to run regardless of the level of Vcc. As Vcc falls below approximately 3.0 volts, a power switching circuit turns the internal lithium energy source on to maintain the clock and timer data and functionality. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc and disconnects the internal lithium energy source. Normal operation can resume after Vcc exceeds 4.5 volts for a period of 150 ms.

RAMified TIMEKEEPER REGISTERS

The RAMified Timekeeper has 64 registers which are eight bits wide that contain all of the timekeeping, alarm, watchdog, control, and data information. The clock, calendar, alarm, and watchdog registers are memory locations which contain external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy (see Figure 1). The Command Register bits are affected by both internal and external functions. This register will be discussed later. The 8K or 32K bytes of RAM registers can only be accessed from the external address and data bus. Register 0, 1, 2, 4, 6, 8, 9, and A contain time of day and date information (see Figure 2). Time of day information is stored in BCD. Registers 3, 5, and 7 contain the Time of Day Alarm information. Time of Day Alarm information is stored in BCD. Register B is the Command Register and information in this register is binary. Registers C and D are the Watchdog Alarm Registers and information which is stored in these two registers is in BCD. Registers E through 1FFF or 7FFF are user bytes and can be used to maintain data at the user's discretion.

BLOCK DIAGRAM Figure 1



TIME OF DAY REGISTERS

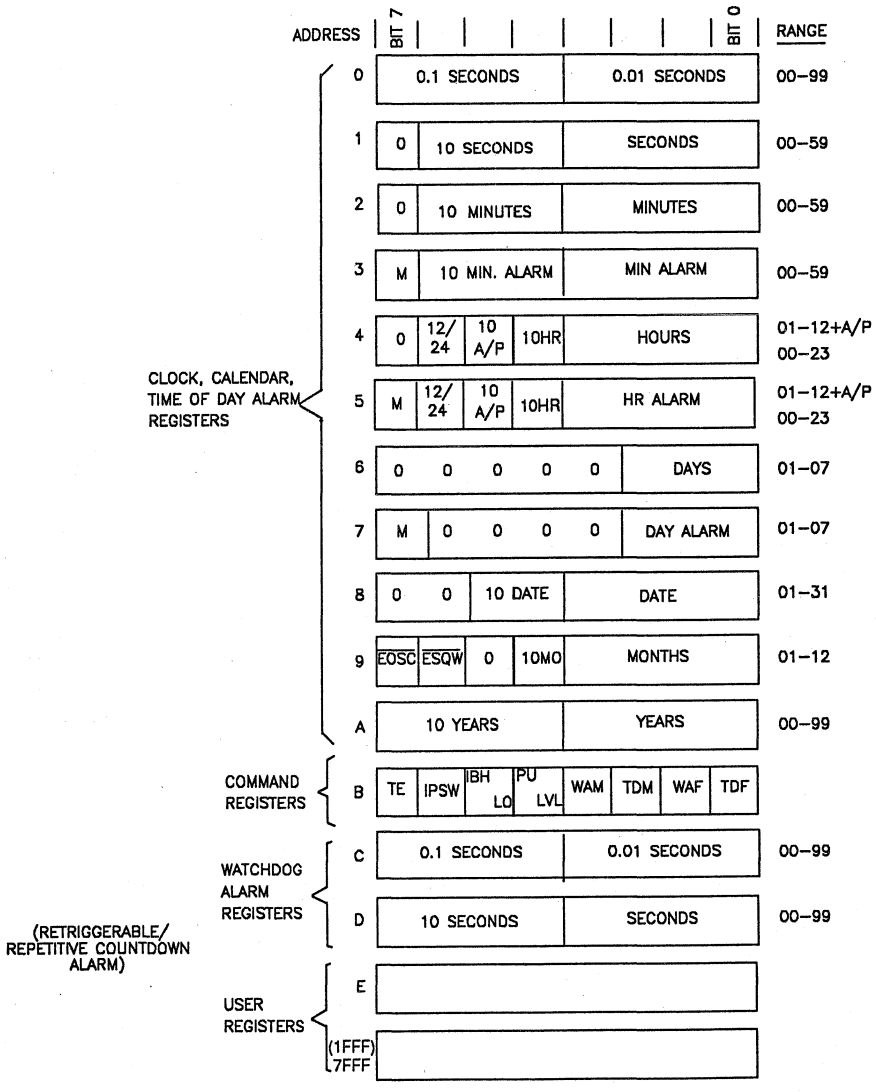
Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD. Ten bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the Months Register (9) are binary bits. When set to logic zero, EOSC\ (Bit 7) enables the Real Time Clock oscillator. This bit is set to logic one as shipped from Dallas Semiconductor to prevent lithium energy consumption during storage and shipment. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of this same byte controls the Square Wave Output (pin 31). When set to logic zero, the Square Wave Output Pin will output a 1024 Hz Square Wave Signal. When set to logic one the Square Wave Output Pin is in a high impedance state. Bit 6 of the Hours Register is defined as the 12 or 24 Hour Select Bit. When set to logic one, the 12 Hour Format is selected. In the 12 Hour Format, bit 5 is the AM/PM bit with logic one being PM. In the 24 Hour Mode, bit 5 is the Second 10 Hour bit (20-23 hours). The Time of Day Registers are updated every .01 seconds from the Real Time Clock, except when the TE bit (bit 7 of Register B) is set low or the clock oscillator is not running. The preferred method of synchronizing data access to and from the RAMified Timekeeper is to access the Command Register by doing a write cycle to address location 0B and setting the TE bit (Transfer Enable bit) to a logic zero. This will freeze the External Time of Day Registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the watch registers have been read or written, a second write cycle to location 0B, setting the TE bit to a logic one, will put the Time of Day Registers back to being updated every .01 second. No time is lost in the Real Time Clock because the internal copy of the Time of Day Register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Time of Day Registers is to ignore synchronization. However, any single read may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the Time of Day Alarm is checked during the period that hundreds of seconds reads 99 and are transferred to the external register when hundredths of seconds roll from 99 to 00. A way of making sure data is valid is to do multiple reads and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the write cycle has caused proper update is to do read verifies and re-execute the write cycle if data is not correct. While the possibility of erroneous results from reads and write cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the RAMified Timekeeper.

TIME OF DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the Time of Day Alarm Registers. Bits 3, 4, 5, and 6 of Register 7 will always read zero regardless of how they are written. Bit 7 of Registers 3, 5, and 7 are mask bits (Figure 3). When all of the mask bits are logic zero, a Time of Day Alarm will only occur when Registers 2, 4, and 6 match the values stored in Registers 3, 5, and 7. An alarm will be generated every day when bit 7 of Register 7 is set to a logic one. Similarly, an alarm is generated every hour when bit 7 of Registers 7 and 5 is set to a logic 1. When bit 7 of Registers 7, 5, and 3 is set to a logic 1, an alarm will occur every minute when Register 1 (seconds) rolls from 59 to 00.

Time of Day Alarm Registers are written and read in the same format as the Time of Day Registers. The Time of Day Alarm Flag and Interrupt is always cleared when Alarm Registers are read or written.

DS1386 RAMified TIMEKEEPER REGISTERS Figure 2



TIME OF DAY ALARM MASK BITS Figure 3

MINUTES	HOURS	DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN HOURS AND MINUTES MATCH
0	0	0	ALARM WHEN HOURS, MINUTES, AND DAYS MATCH

NOTE: ANY OTHER COMBINATIONS OF MASK BIT SETTINGS PRODUCE ILLOGICAL OPERATION.

WATCHDOG ALARM REGISTERS

Registers C and D contain the time for the Watchdog Alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register C or D will cause the Watchdog Alarm to reinitialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the Watchdog Timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The Watchdog Timer Countdown is interrupted and reinitialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the Watchdog Timer can prevent the Watchdog Alarm from ever going to an active level. If access does not occur, countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual countdown register is internal and is not readable. Writing registers C and D to zero will disable the Watchdog Alarm feature.

COMMAND REGISTER

Address location 0B is the Command Register where mask bits, control bits, and flag bits reside. Bit 0 is the Time of Day Alarm Flag (TDF). When this bit is set internally to a logic one, an alarm has occurred. The time of the alarm can be determined by reading the Time of Day Alarm Registers. However, if the transfer enable bit is set to logic zero the Time of Day registers may not reflect the exact time that the alarm occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm Registers are read. Bit 1 is the Watchdog Alarm Flag (WAF). When this bit is set internally to a logic one, a Watchdog Alarm has occurred. This bit is read only and writing this register has no effect on the bit. The bit is reset when any of the Time of Day Alarm Registers are accessed. Bit 2 of the Command Register contains the Time of Day Alarm Mask Bit (TDM). When this bit is written to a logic one, the Time of Day Alarm Interrupt . Output is deactivated regardless of the value of the Time of Day Alarm Flag. When TDM is set to logic zero, the Time of Day Interrupt Output will go to the active state which is determined by bits 0, 4, 5, and 6 of the Command Register. Bit 3 of the Command Register contains the Watchdog Alarm Mask Bit (WAM). When this bit is written to a logic one, the Watchdog Interrupt Output is deactivated regardless of the value in the Watchdog Alarm Registers. When WAM is set to logic zero, the Watchdog Interrupt Output will go to the active state which is determined by bits 1, 4, 5, and 6 of the Command Register. These four bits define how Interrupt Output Pins INTA\ and INTB\ (INTB) will be operated. Bit 4 of the Command Register determines whether both interrupts will output a pulse or level when activated. If bit 4 is set to logic one, the pulse mode is selected and INTA\ will sink current for a minimum of 3 ms and then release. Output INTB\(INTB) will either sink or source current for a minimum of 3 ms depending on the level of bit 5. When bit 5 is set to logic one, the B interrupt will source current. When bit 5 is set to logic zero, the B interrupt will sink current. Bit 6 of the Command Register directs which type of interrupt will be present on interrupt pins INTA\ or INTB\(INTB). When set to logic one, INTA\ becomes the Time of Day Alarm Interrupt pin and INTB\(INTB) becomes the Watchdog Interrupt pin. When bit 6 is set to logic zero, the interrupt functions are reversed such that the Time of Day Alarm will be output on INTB\(INTB) and the Watchdog Interrupt will be output on INTA\. Caution should be exercised when dynamically setting this bit as the interrupts will be reversed even if in an active state. Bit 7 of the Command Register is for Transfer Enable (TE). The function of this bit is described in the Time of Day Registers.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to + 70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0° C to 70° C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{cc}	4.5	5.0	5.5	V	10
INPUT LOGIC 1	V_{IH}	2.2		V_{cc} + 0.3	V	10
INPUT LOGIC 0	V_{IL}	-0.3		+0.8	V	10

DC ELECTRICAL CHARACTERISTICS

(0° C to 70° C, V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT	I_{IL}	-1.0		+1.0	uA	
OUTPUT LEAKAGE CURRENT	I_{LO}	-1.0		+1.0	uA	
I/O LEAKAGE CURRENT	I_{LIO}	-1.0		+1.0	uA	
OUTPUT CURRENT @ 2.4V	I_{OH}	-1.0			mA	
OUTPUT CURRENT @ 0.4V	I_{OL}	2.0			mA	13
STANDBY CURRENT CE\ = 2.2V	I_{CCS1}		3.0	7.0	mA	
STANDBY CURRENT CE\ > Vcc -0.5	I_{CCS2}			4.0	mA	
ACTIVE CURRENT	I_{CC}			15	mA	
WRITE PROTECTION VOLTAGE	V_{TP}		4.25		V	

CAPACITANCE

(t_A=25° C)

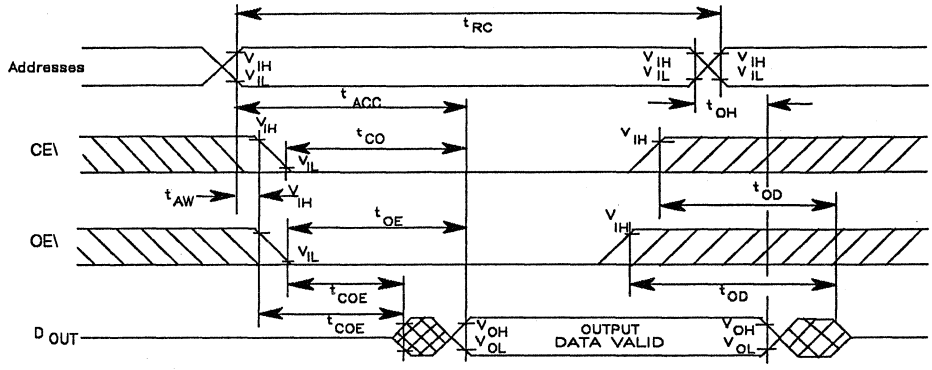
PARAMETER	SYMBOL	TYP.	MAX	UNITS	NOTES
INPUT CAPACITANCE	C_{IN}	7	10	pF	
OUTPUT CAPACITANCE	C_{OUT}	7	10	pF	
INPUT/OUTPUT CAPACITANCE	$C_{I/O}$	7	10	pF	

AC ELECTRICAL CHARACTERISTICS

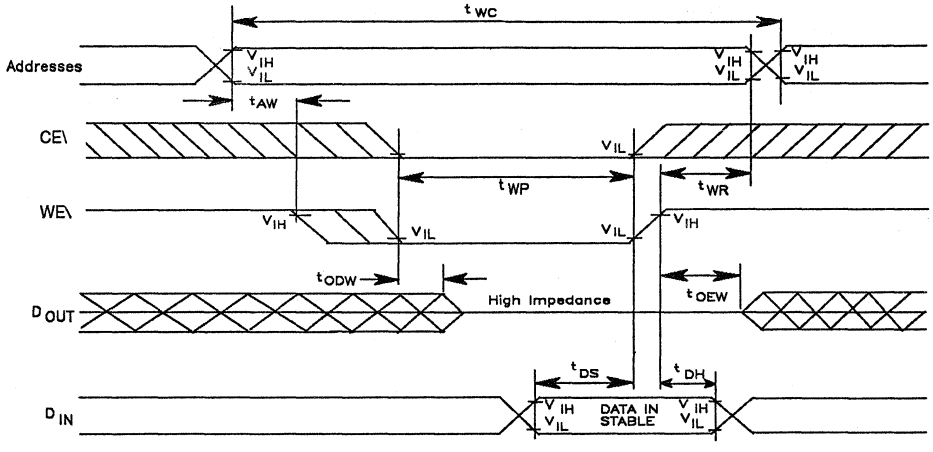
(0° C to 70° C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
READ CYCLE TIME	t_{RC}	150			ns	1
ADDRESS ACCESS TIME	t_{ACC}			150	ns	
CE\ ACCESS TIME	t_{CO}			150	ns	
OE\ ACCESS TIME	t_{OE}			75	ns	
OE\ OR CE\ TO OUTPUT ACTIVE	t_{COE}	10			ns	
OUTPUT HIGH Z FROM DESELECT	t_{OD}			75	ns	
OUTPUT HOLD FROM ADDRESS CHANGE	t_{OH}	10			ns	
WRITE CYCLE TIME	t_{WC}	150			ns	
WRITE PULSE WIDTH	t_{WP}	140			ns	3
ADDRESS SETUP TIME	t_{AW}	0			ns	
WRITE RECOVERY TIME	t_{WR}	10			ns	
OUTPUT HIGH Z FROM WE\	t_{ODW}			50	ns	
OUTPUT ACTIVE FROM WE\	t_{OEW}	10			ns	
DATA SETUP TIME	t_{DS}	60			ns	4
DATA HOLD TIME	t_{DH}	0			ns	4,5
INTA\, INTB\ PULSE WIDTH	t_{IPW}	3			ms	11,12

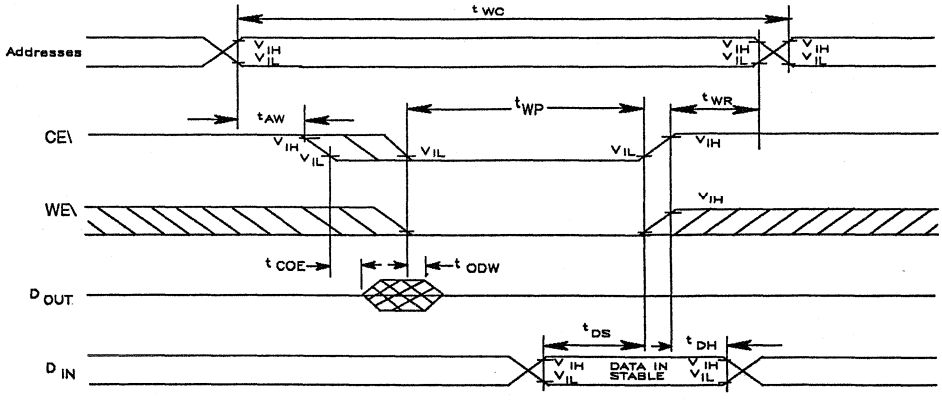
READ CYCLE (1)



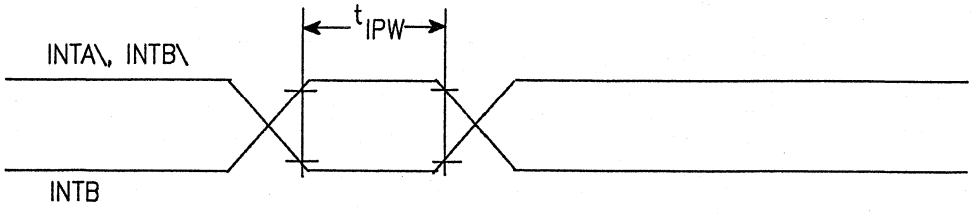
WRITE CYCLE 1 (2), (6), (7)



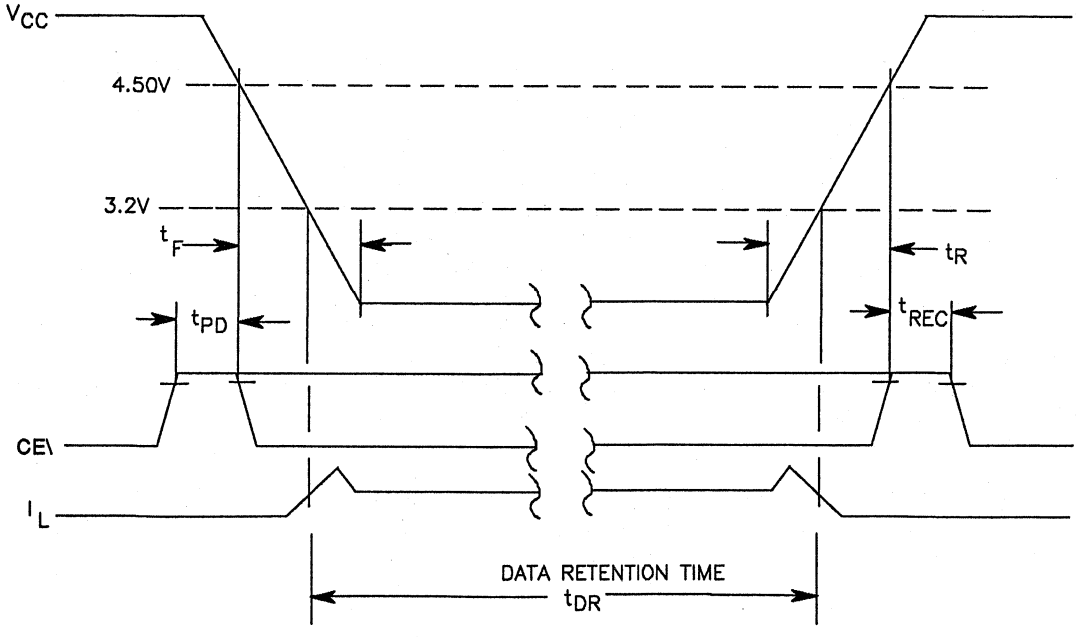
WRITE CYCLE 2 (2), (8)



TIMING DIAGRAM - INTERRUPT OUTPUTS PULSE MODE (SEE NOTES 11,12)



POWER-DOWN/POWER-UP CONDITION



LEAKAGE CURRENT I_L SUPPLIED FROM LITHIUM CELL

POWER-UP/POWER-DOWN CONDITION

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	350		us	
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	100		us	
t_{REC}	CE\ at V_{IH} after Power-Up	150		ms	

(t_A=25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

1. WE\ is high for a read cycle.
2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of the CE\ and WE\. t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.
4. t_{DS} or t_{DH} are measured from the earlier of CE\ or WE\ going high.
5. t_{DH} is measured from WE\ going high. If CE\ is used to terminate the write cycle, then t_{DH} = 20 ns.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition, the output buffers remain in a high impedance state during this period.
8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1386 is marked with a four digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All voltages are referenced to ground.
11. Applies to both interrupt pins when the alarms are set to pulse.
12. Interrupt output occurs within 100 ns on the alarm condition existing.
13. Both INTA\ and INTB\(INTB) are open drain outputs.

AC TEST CONDITIONS

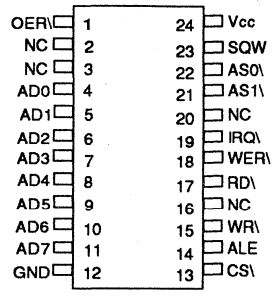
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns.

DALLAS SEMICONDUCTOR

DS1387
RAMified Real Time Clock

FEATURES
- Drop-in replacement for IBM AT computer clock/calendar
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations plus 4K x 8 of static RAM
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
  - Separate 4K x 8 SRAM accessible by using RAM control pins
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable:
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 us to 500 ms
  - End-of-clock update cycle

PIN DESCRIPTION
(\ Denotes Condition Low)



24-PIN ENCAPSULATED PACKAGE
(740 mil)

PIN NAMES

PIN	SIGNAL	DESCRIPTION
1	OER\	RAM Output Enable
2	NC	No Connection
3	NC	No Connection
4-11	AD0-AD7	Multiplexed Address/ Data Bus
12	GND	Ground
13	CS\	RTC Chip Select
14	ALE	RTC Address Strobe
15	WR\	RTC Write Strobe
16	NC	No Connection
17	RD\	RTC Data Strobe
18	WER\	RAM Write Enable
19	IRQ\	Interrupt Request Output
20	NC	No Connection
21	AS1\	RAM Address Strobe
22	AS0\	RAM Address Strobe
23	SQW	Square Wave Output
24	V_{CC}	+5 Volt Supply

DESCRIPTION
The main elements of the DS1387 are the Real Time Clock (RTC) and a 4K X 8 static RAM with interface latches (see Figure 1). The operation of each of these is discussed on the following pages.

OPERATION

The RTC function is the same as the DS1287 Real Time Clock. The RTC functions in the Intel mode only. Access to the RTC is accomplished with four controls: ALE, RD\, WR\ and CS\. For a complete description of the RTC, consult the DS1287 data sheet.

4K X 8 RAM

The addresses of the 4K X 8 SRAM are connected to the eight-pin multiplexed address/data bus through latches. On power-up the RAM is taken out of write-protect status by the power-fail output signal (PFO) from the Real Time Clock. The PFO signal becomes active at 4.25 volts max.

Each latch is clocked by a rising edge signal. The controls are Address Strobe Zero (AS0\) and Address Strobe One (AS1\). Using these clock controls and the two RAM control signals Output Enable RAM (OER\) and Write Enable RAM (WER\), data can be written to or read from memory (see Figure 2). AS0\ is used to latch the lower order address. It is necessary to meet the setup and hold time with valid addresses on AD0-AD7 to accomplish this cycle. In a similar manner, the upper order addresses are latched using AS1\. If the upper or lower order address is correct from a prior cycle, it is not necessary to repeat the address latching sequence.

The data transfer occurs in one of two ways. If a write cycle is to occur, valid data is placed on the bus (AD0-AD7). The Write RAM signal (WER\) is then driven active, and data on the bus is written to RAM provided RAM write timing specifications are met. If a read cycle is to occur, the Output Enable for RAM (OER\) is driven active, and data becomes valid on the bus (AD0-AD7) provided that proper RAM access time parameters are met. Control signals WER\ and OER\ should never be active at the same time. In addition, access to the RTC function must not be attempted when the RAM is being accessed. The internal RAM chip enable is active when either WER\ or OER\ is active. CS\ is for the control of the RTC function only (see Figure 1).

SPECIFICATIONS

Consult the DS1287 data sheet for complete electrical, mechanical, and technical specifications for the RTC. The RTC is the same as the DS1287, with the following exceptions:

1. Pin 1 on the DS1287 is the MOT pin; it is the OER\ pin on the DS1387. The bus selection capability of the DS1287 has been eliminated on the DS1387. Only the Intel bus interface timing is applicable.

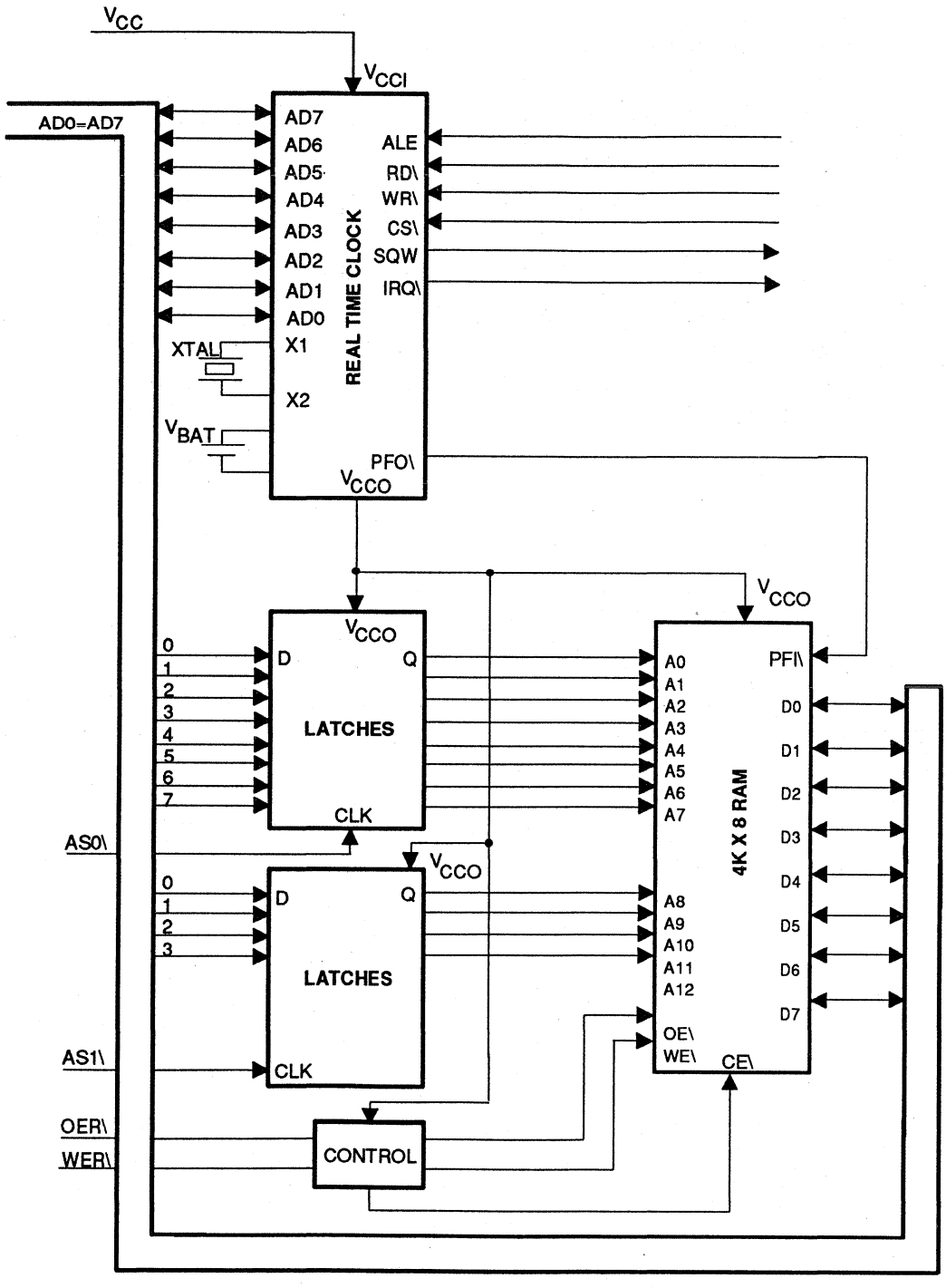
2. Pin 18 on the DS1287 is the RESET\ pin; it is the WER\ pin on the DS1387. The DS1387 will operate the same as the DS1287 with RESET\ tied to V_{CC}. To clear the interrupt request output (IRQ\) requires a read cycle to the RTC register C.

3. Pins 21 and 22 on the DS1287 are No Connections; these pins are AS1\ and AS0\ on the DS1387.

4. The DS1387 has an additional 4K X 8 of nonvolatile SRAM that is controlled with the signals AS0\, AS1\, OER\ and WER\. See the timing diagrams and AC electrical characteristics on the following pages for these additional specifications.

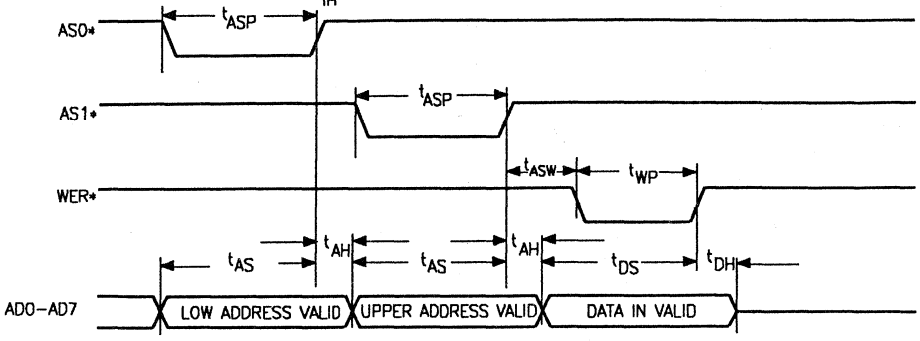
5. The active power supply current of the DS1387 is 35 mA typical and 50 mA maximum. Active power is defined as OER\ or WER\ low. When both OER\ and WER\ are high, the DS1387 enters a standby mode which reduces the power supply current requirement to 3 mA typical.

DS1387 BLOCK DIAGRAM Figure 1

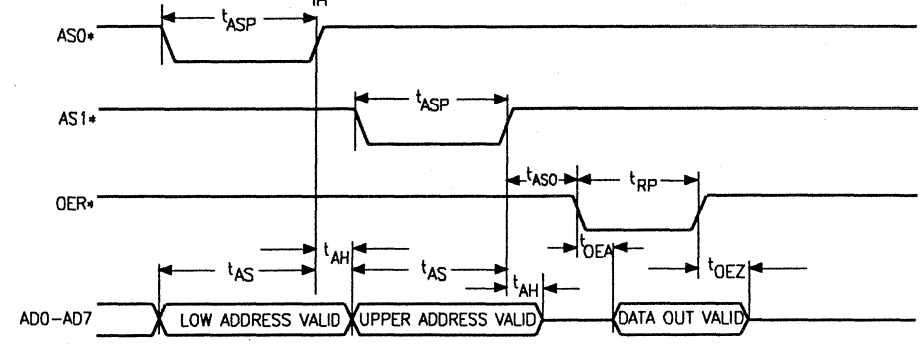


TIMING DIAGRAMS Figure 2

WRITE TIMING OER\ = V_{IH}



READ TIMING WER\ = V_{IH}



AC ELECTRICAL CHARACTERISTICS

(0° to 70°C, V_{CC}= 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX.	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable	t_{OEA}			200	ns	
Access Time Write Pulse Width	t_{WP}	200			ns	
OER\ to Output in High Z	t_{OEZ}			50	ns	
READ Pulse Width	t_{RP}	200			ns	
AS0\,AS1\ Pulse Width	t_{ASP}	75			ns	
ASX\ High to OER\ Low	t_{ASO}	20			ns	1
ASX\ High to WER\ Low	t_{ASW}	20			ns	1

NOTE

1. ASX is either AS0\ or AS1\.

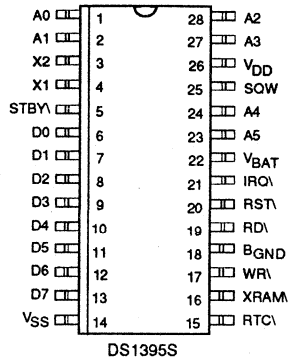
DALLAS SEMICONDUCTOR

DS139x
RAMified Real Time Clock

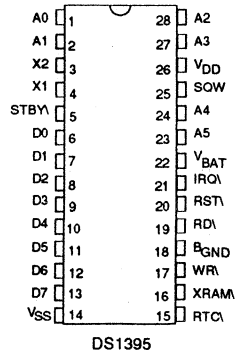
FEATURES

- Ideal for EISA bus PCs
- Functionally compatible with MC146818 in 32 KHz mode
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary or BCD representations of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Interfaced with software as 64 RAM locations plus 4K x 8 of static RAM
  - -14 bytes of clock and control registers
  - -50 bytes of general and control registers
  - -Separate 4K x 8 nonvolatile SRAM
- Programmable square wave output signal
- Bus-compatible interrupt signals (IRQ\)
- Three interrupts are separately software-maskable and testable:
  - -Time-of-day alarm once/second to once/day
  - -Periodic rates from 122 us to 500 ms
  - -End-of-clock update cycle
- 28-pin JEDEC footprint
- DIP and SOIC packages available

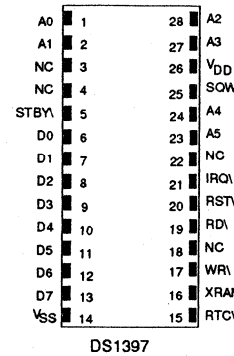
PIN DESCRIPTION



DS1395S
28-Pin SOIC (330 mil)



DS1395
28-Pin DIP (600 mil)



DS1397
28-Pin Encapsulated Package (740 mil)

PIN DESCRIPTIONS
(\ Denotes Condition Low)

VDD, VSS: Bus operational power is supplied to the part via these pins. The voltage level present on these pins should be monitored to transition between operational power and battery power.

D0-D7 — Data Bus (bidirectional): Data is written into the device from the data bus if either XRAM\ or RTC\ is asserted during a write cycle at the rising edge of a WR\ pulse. Data is read from the device and driven onto the data bus if either XRAM\ or RTC\ is asserted during a read cycle when the RD\ signal is low.

A0-A5 — Address Bus (input): Various internal registers of the device are selected by these lines. When RTC\ is asserted, A0 selects between the indirect address register and RTC data register. When the XRAM\ is asserted, A0-A5 address the 32-byte page of RAM. When A5 is high, the RAM page register is accessible. When A5 is low, A0-A4 address the 32-byte page of RAM.

RD\ — Read Strobe (input): Data is read from the selected register and driven onto the data bus by the device when this line is low and either RTC\ or XRAM\ is asserted.

WR\ — Write Strobe (input): Data is written into the device from the data bus on the rising edge after a low pulse on this line when the device has been selected by either the XRAM\ or RTC\ signals.

STBY\ — Standby (input): Accesses to the device are inhibited and outputs are tri-stated to a high impedance state when this signal is asserted low. All data in RAM of the device is preserved. The real time clock continues to keep time.

If a read or write cycle is in progress when the STBY\ signal is asserted low, the internal cycle will be terminated when either the external cycle completes or when the internal chip enable condition (V_{DD} is 4.25 volts, typical) is negated, whichever occurs first.

RTC\ — Real Time Clock Select (input): When this signal is asserted low, the real time clock registers are accessible. Registers are selected by the A0 line. Data is driven onto the data bus when RD\ is low. Data is received from the bus when WR\ is pulsed low and then high.

SQW — Square Wave (output): Frequency selectable output. Frequency is selected by setting register A bits RSO-RS3. See Table 2 for frequencies that can be selected.

XRAM\ — Extended RAM Select (input): When this signal is asserted low, the extended RAM bytes are accessible. The XRAM page register is selected when the A5 address line is high. A 32-byte page of RAM is accessible when A5 is low. A0-A4 select the bytes within the page of RAM. Data is driven onto the data bus when RD\ is low. Data is received from the bus when WR\ is pulsed low and then high.

IRQ\ — Interrupt Request (output): The IRQ\ signal is an active low, open drain output that is used as a processor interrupt request. The IRQ\ output follows the state of the interrupt pending bit (bit 7) in status register C. IRQ\ can be asserted by the alarm, update ended, or periodic interrupt functions depending on the configuration of register B.

RESET\ — Reset (input): The reset signal is used to initialize certain registers to allow proper operation of the RTC module. When RESET\ is low, the following occurs.

1) The following register bits are cleared:
    a. Periodic interrupt (PIE)
    b. Alarm interrupt enable (AIE)
    c. Update ended interrupt (UF)
    d. Interrupt request flag (IRQF)
    e. Periodic interrupt flag (PF)
    f. Alarm interrupt flag (AF)
    g. Square wave output enable (SQWE)
    h. Update ended interrupt enable (UIE)
2) The IRQ\ pin is in the high impedance state.
3) The RTC is not processor accessible.

ADDITIONAL PIN DESCRIPTION (FOR DS1395, 1395S)

X1, X2: Connections for a standard 32.768 KHz quartz crystal, Daiwa part number DT-26S or equivalent. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. These crystals can be ordered from Dallas Semiconductor, part number DS9032.

V_{BAT}: Battery input for any standard 3 volt lithium cell or other energy source. Battery voltage must be held between 2 and 3.4 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as 1.26 x V_{BAT}. A maximum load of .5 uA at 25°C in the absence of power should be used to size the external energy source.

B_{GND}-Battery ground: This pin or pin 14 can be used for the battery ground return.

OPERATION

Power-Down/Power-Up: The real time clock module will continue to operate and all of the RAM, time, and calendar and alarm memory locations will remain non-volatile regardless of the voltage level of V_{DD}. When the voltage level applied to the V_{DD} input is greater than 4.25 volts (typical), the module becomes accessible after 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied.

When V_{DD} falls below the CE_{THR} (4.25 volts typical), the chip select inputs RTC\ and XRAM\ are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. When V_{DD} falls below 3.2 volts (typical), the module is switched over to an internal power source so that power is not interrupted to timekeeping and nonvolatile RAM functions.

Address Map: The registers of the device appear in two distinct address ranges. One set of registers is active when RTC\ is asserted low and represents the real time clock. The second set of registers is active when XRAM\ is asserted low and represents the extended RAM.

RTC Address Map: The address map of the RTC module is shown in Figure 2. The address map consists of 50 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information. All 64 bytes can be accessed as read/write registers except for the following:

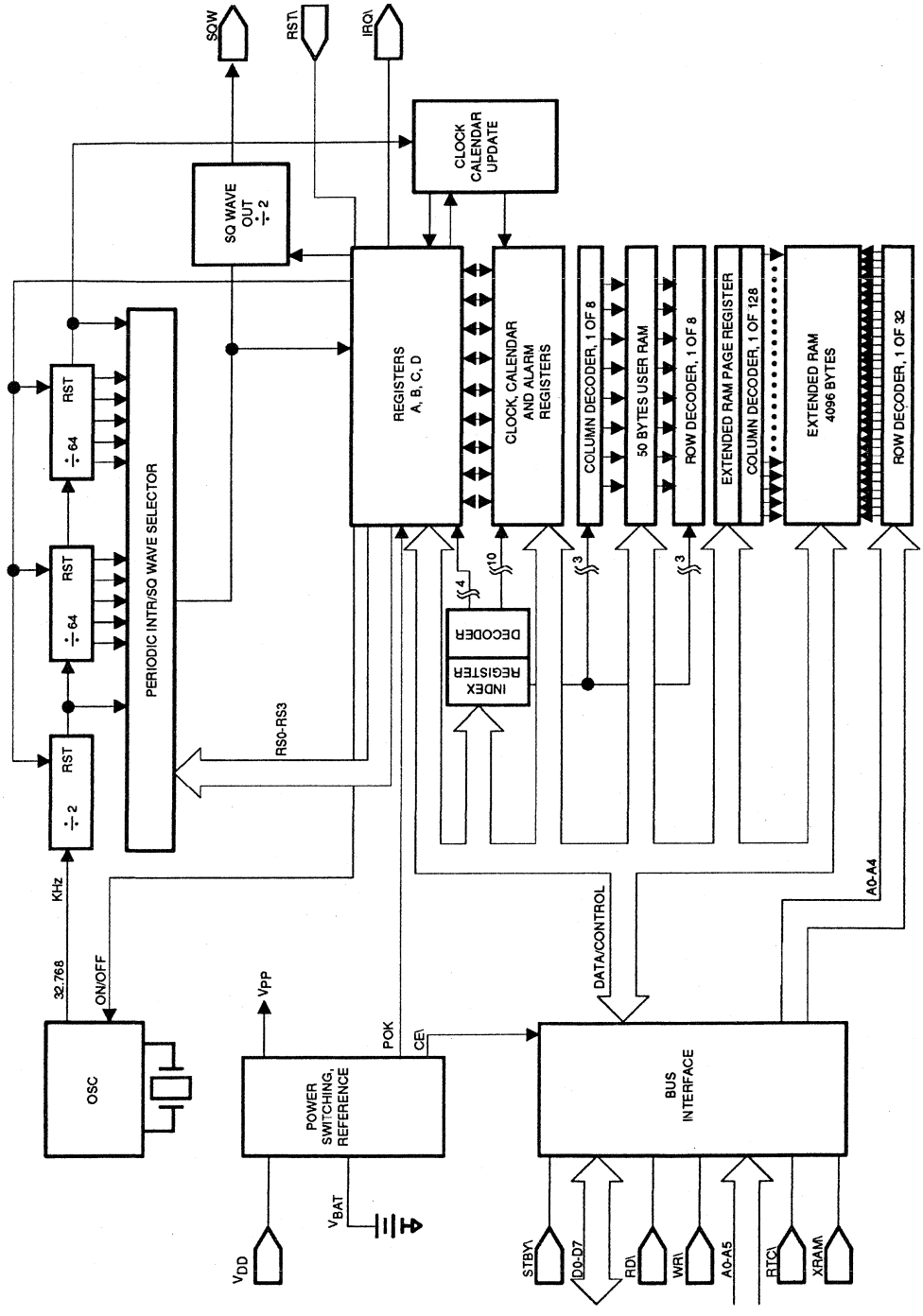
(1) Registers C and D are Read Only (status information)
(2) Bit 7 of register A is Read Only
(3) Bit 7 of the "Seconds" byte (00) is Read Only

The first byte of the real time clock address map is the RTC indirect address register, accessible when A0 is low. The second byte is the RTC data register, accessible when A0 is high. The function of the RTC indirect address register is to point to one of the 64 RTC registers that are indirectly accessible through the RTC data register.

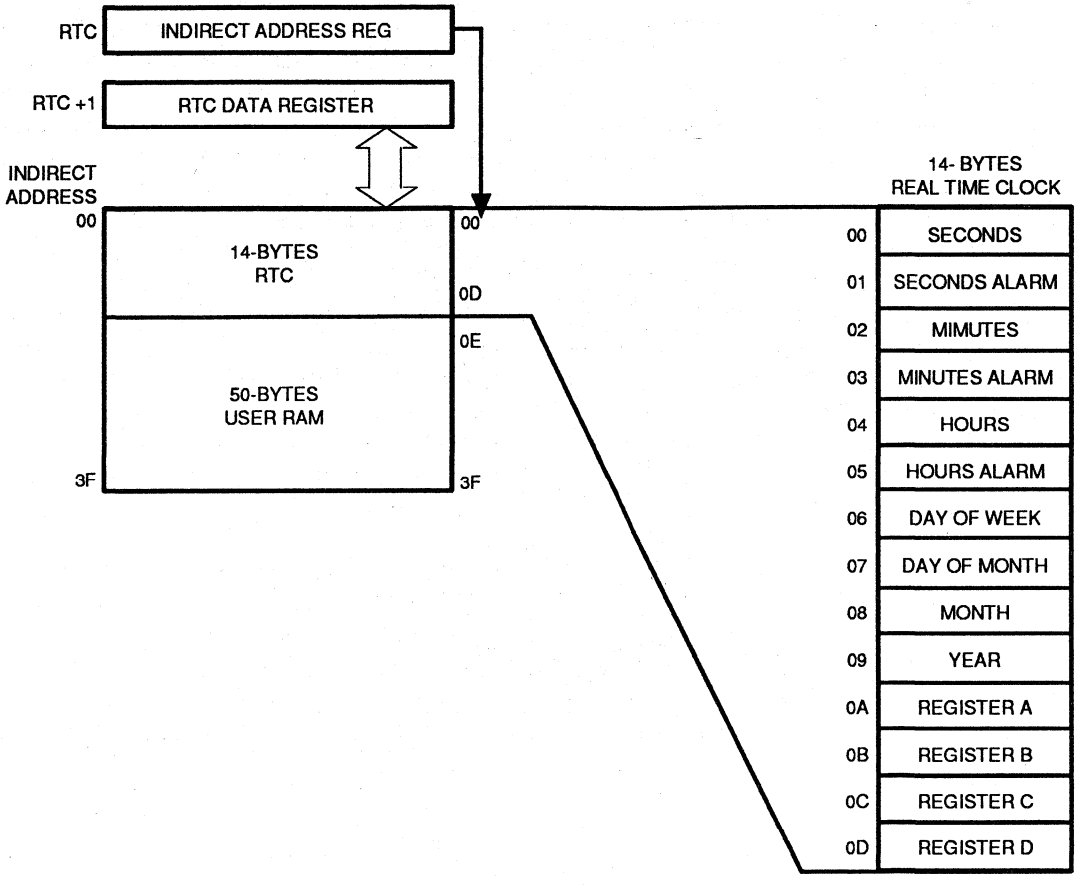
Extended RAM Address Map: The first 32 bytes of the extended RAM represent one of 128 pages of general purpose nonvolatile memory. These 32 bytes on a page are addressed by A0 through A4 when A5 is low. When A5 is high, the XRAM page register is accessible. The value in the XRAM page register points to one of 128 pages of nonvolatile memory available. The address of the XRAM page register is dependent only on A5 being high; thus, there are 31 aliases of this register in I/0 spaces. (See Figure 2.)

Time, Calendar, and Alarm Locations: The time and calendar information is obtained by reading the appropriate memory bytes. The

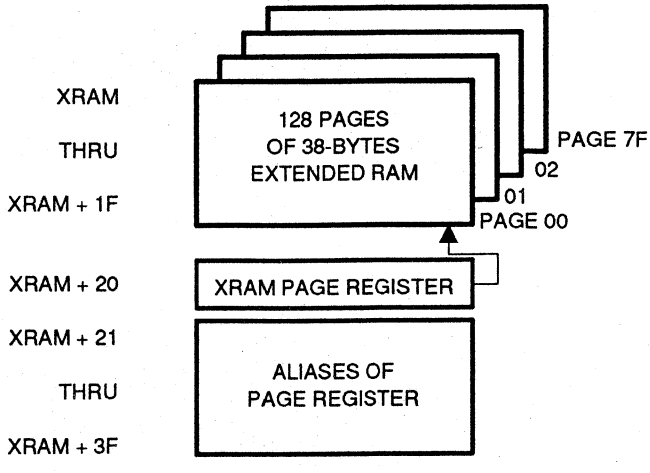
DS139x BLOCK DIAGRAM Figure 1



REAL TIME CLOCK RAM MAP Figure 2



EXTENDED RAM ADDRESS MAP Figure 3



time, calendar, and alarm are set or initialized by writing to the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either binary or binary coded decimal (BCD) format. Before writing to the internal time, calendar, and alarm registers, the SET access bit in register B should be set to a logic one. This prevents updates from occurring while the access is being attempted. In addition to writing to the ten time, calendar, and alarm registers in a a selected format (binary or BCD), the Data Mode (DM) bit of register B must be set to the appropriate logic level. All ten time, calendar, and alarm registers must use the same data mode. The SET bit in register B should be cleared after the DM bit has been written to allow the real time clock to update the time and calendar bytes.

Once initialized, the RTC makes all the updates in the selected mode. The data mode cannot be changed without reinitializing all ten data bytes. Table 1 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second, the time and calendar bytes are advanced and a check for an alarm condition is made. If a read of the time and calendar information is made during an update, it is possible that the seconds, minutes, and hours, and date may not correlate. The probability of reading the incorrect time is low; however, precautions should be taken. See the section entitled "Update Cycle".

Nonvolatile RAM: The 50 general purpose nonvolatile RAM bytes are not dedicated to any

TIME, CALENDAR, AND ALARM DATA MODES (Table 1)

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours 24-Hour Mode	0-23	00-17	00-23
5	Hours Alarm 12-hr. Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours Alarm 24-hr. Mode	0-23	00-17	00-23
6	Day of Week Sunday = 1	1-7	01-07	01-07
7	Date of Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

specific function. They can be accessed by the processor as nonvolatile memory at any time, even during an update cycle.

Interrupts: The RTC includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates of 500 ms to 122 us. The update-ended interrupt can be used to indicate to the processor that an update cycle is complete. Each of these interrupt conditions is described in greater detail in the following sections.

Enabling Interrupts: Three bits in register B are used to select which source or sources of interrupt will be enabled. Writing a logic 1 to the appropriate interrupt-enable bit permits the interrupt to be initiated when the interrupt event occurs. A logic zero in the interrupt-enable bit prohibits the IRQ\ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, the IRQ\ pin is asserted immediately even though the event causing the interrupt may have occurred much earlier. As a result, there are cases where the program should clear any pending interrupt conditions before enabling new interrupts.

Interrupt Status: Register C is used as an interrupt status register. Three flag bits correspond to the three interrupt sources. These three bits are set respectively when the appropriate interrupt condition is satisfied regardless of the setting of the interrupt enable bits in register B. These flag bits can be used in a polling mode without enabling the corresponding interrupt enable bits. When a flag bit is set in register C, this is an indication to the program that an interrupt event has occurred since register C has last been read. The act of reading register C clears all flag bits. Therefore all flag bits should be examined by software with each read of register C to ensure that no interrupts are lost. Interrupt flags are double buffered so that new interrupt events are held pending.

If an interrupt enable bit in register B is set and its corresponding interrupt flag in register C is also set, the IRQ\ bit is asserted low. The IRQ\ bit is asserted low as long as at least one of the three interrupt sources has both its flag bit (in register C) and its enable bit (in register B) set. The IRQF bit in register C will read logic one as long as the IRQ\ pin is being driven low. The microprocessor can determine if the RTC module has initiated the interrupt by reading register C. A logic one in the bit 7 position of register C indicates that one or more interrupts have been initiated by the RTC module. The act of reading register C clears all active flag bits and the IRQF bit.

Periodic Interrupt: The periodic interrupt will cause the RTC module to generate an interrupt at time intervals ranging from 122 microseconds to 500 milliseconds. This function is separate from the alarm function which can generate interrupts on intervals of once per second to once per day. The periodic interrupt rate is selected using the RSO-RS3 bits in register A as shown in Table 2. Changing the RS bits affects both the periodic interrupt rate and the square wave output rate.

Update (Cycle) Ended Interrupt: The Update-In-Progress (UIP) bit in register A pulses once per second whenever an update cycle occurs. The Update Ended Interrupt Flag (UF) will be set at the conclusion of the update cycle or when the UIP bit in register A toggles from logic one to logic zero. If the Update-Ended Interrupt Enable (UIE) bit in register B is also set, the IRQ\ pin will be asserted low. (See Figure 4.)

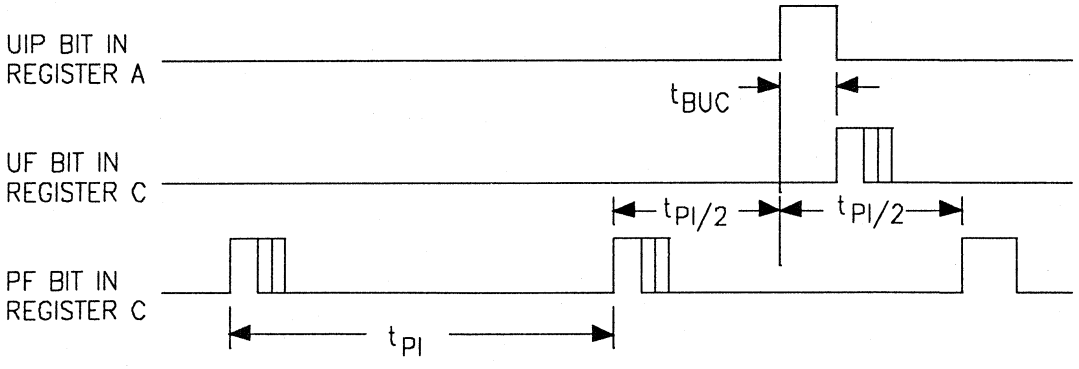
Alarm Interrupt: The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate locations, the alarm

interrupt is initiated at the specified time each day if the alarm enable bit is set to logic one. Second, it is used to insert a don't care code into one or more of the three alarm bytes. The don't care code is any hexadecimal value from CO to FF. The two most significant bits of each byte set the don't care condition when they are set to logic one. An alarm each hour occurs when don't care codes are written in the minutes and seconds alarm locations. When don't care codes are written into all three alarm locations, an alarm interrupt can be generated each second.

OSCILLATOR CONTROL BITS

When the DS1397 real time clock module is shipped from the factory, the internal oscillator is disabled. This feature prevents the lithium energy source from being used until the RTC module is installed in a system. A pattern of 010 in bits 4 through 6 of register A will turn on the oscillator and enable the countdown chain. A pattern of 11X will turn on the oscillator but will leave the countdown chain in reset. All other bit pattern combinations in bits 4 through 6 will hold the oscillator off.

PERIODIC INTERRUPT AND UPDATE ENDED INTERUPT RELATIONSHIP Figure 4



NOTES:

t_{PI} = Periodic Interrupt Time Interval per Table 2.
t_{BUC} = Delay Time Before Update Cycle = 244 us.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the fifteen divider taps are made available to a 1 of 15 selector. The divider taps can be used for two purposes. First, they can generate a fixed frequency square wave output signal on the SQW pin; second, they can generate interrupts at a selected frequency. The RSO-RS3 bits in register A establish the square wave output frequency and/or interrupt rate. These frequencies are listed in Table 2. Once the frequency is selected, the SQW pin signal can be enabled or disabled under program control using the Square Wave Enable (SQWE) bit in register B. See the section entitled "Periodic Interrupt."

UPDATE CYCLE: The RTC executes an update cycle once per second regardless of the state of the SET bit in register B. When the SET bit in register B is set to logic one, the user copy of the double buffered time, calendar, and alarm bytes is frozen and will not update as the time increments. However, the time countdown chain

continues to update the internal copy of the buffer. This feature allows accurate time to be maintained independently of reading or writing the time calendar or alarm buffers. This also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with its corresponding time byte and issues an alarm interrupt if a match or don't care code is present in all three alarm byte positions.

There are three methods that can be employed to accurately access time, date, and calendar data from the real time clock . The first uses the update-ended interrupt. If this interrupt is enabled, an interrupt occurs after every update cycle. Immediately following this interrupt, the processor has 999 milliseconds in which to read time and date information before the next update cycle. If the processor reads the time and date within this time interval, no possibility exists for reading inconsistent time and calendar data. As with all interrupts, the IRQF bit in register C should be cleared before leaving the interrupt service routine.

Using the second method for reading time and date, the processor polls the Update-In-Progress (UIP) bit in register A to determine if the update cycle is in progress. The UIP bit will pulse once each second. After the UIP bit goes to logic one, the update transfer occurs 244 microseconds later. If the UIP bit reads logic zero, the processor has at least 244 microseconds before the time/date data will be updated. Therefore, the system should ensure that interrupts and DMA activity do not preclude reading the time and date information within 244 microseconds.

The third method uses the periodic interrupt to determine if an update cycle is in progress. The UIP bit in register A is pulsed high halfway between two PF bit pulses in register C (see Figure 4). The processor should read time and date information within the time interval of (t_{PI}/ 2) 244 us.

REGISTERS: The real time clock module has four control registers that are accessible at all times, even during update cycles.

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP: The Update-In-Progress (UIP) bit is a status flag that can be monitored by the processor. When the UIP bit reads logic one, the update transfer will soon occur. When the UIP reads zero, the update transfer will not occur for at least 244 microseconds. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RESET. Writing the SET bit in register B to a logic one inhibits any update transfer and clears the UIP status bit.

DV0, DV1, DV2: These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn on the oscillator and allow the RTC to keep time. A pattern of 11X enables the oscillator but holds the countdown chain in reset. The first update cycle transfer occurs after 500 milliseconds after the oscillator first becomes operational (500 ms + t_{RC} after writing a pattern of 010 to bits DV0, DV1, and DV2, respectively). If the timing chain is held in reset with oscillator running by writing a

pattern of 11x, the first update transfer occurs 500 ms after writing a pattern of 010 to bits DV0, DV1, and DV2, respectively.

RS3, RS2, RS1, RS0: These four bits are used to select one of 13 taps on the 15 stage divider and to disable the divider output pin signal. (See Table 2.) The selected tap can be used to generate an output square wave (on the SQW pin) and/or a periodic interrupt. The user can do one of the following:

1. Enable the interrupt with the PIE bit;
2. Enable the SQW output pin with the SQWE bit;
3. Enable both at the same time and rate; or
4. Enable neither.

PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY Table 2

SELECT BITS REGISTER A				t_{PI} PERIODIC	SQW OUTPUT
RS3	RS2	RS1	RS0	INTERRUPT RATE	FREQUENCY
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 us	8.192 KHz
0	1	0	0	244.141 us	4.096 KHz
0	1	0	1	488.281 us	2.048 KHz
0	1	1	0	976.5625 us	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

REGISTER B MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET: When the SET bit is logic zero, the update transfer functions normally by advancing the real time clock value once each second. When the SET bit is logic one, all update transfers are inhibited and the program can initialize the time and calendar byte without an update occurring in the midst of the initialization. Data read from the time and calendar bytes will be static as long as the SET bit is logic one. The SET bit is a read/write bit which is not modified by RESET or internal functions of the RTC module.

When the SET bit is a logic one, data written to registers A and B is inhibited from transferring to the active control registers. That is, registers A and B are double buffered, and data written or read from these registers will affect or reflect the contents of the holding registers only as long as the SET bit is logic one. As a result, changes made to the RS or DV bits will not take effect until the SET bit is cleared. Any programmed interrupts in effect before the SET was written to logic one will remain in effect, at the previous rate, until the SET bit is cleared.

PIE: The Periodic Interrupt Enable (PIE) bit is a read/write bit that allows the Periodic interrupt Flag (PF) bit in register C to cause the IRQ\ pin to be driven low. When the PIE bit is set to logic one, periodic interrupts are generated by driving the IRQ\ pin low at the periodic interrupt rate specified by the RS3 through RS0 bits of register A. A logic zero in the PIE bit inhibits the IRQ\ output from being driven by a periodic interrupt. PF is always set at the periodic interrupt rate regardless of the state of the PIE bit. The PIE bit is not modified by any internal RTC module functions but is cleared by the hardware RESET signal.

AIE: The Alarm Interrupt Enable (AIE) bit is a read/write bit, which, when set to logic one, permits the Alarm Flag (AF) bit in register C to assert the IRQ\ signal. An alarm interrupt occurs for each second that the three alarm bytes (including the don't care alarm codes) equals the three time bytes. When the AIE bit is set to logic zero, the AF bit does not assert the IRQ\ signal. The AIE bit is not modified by any internal RTC functions but is cleared by the hardware RESET signal.

UIE: The Update ended Interrupt Enable (UIE) bit is a read/write bit which, when set to logic one, enables the Update end Flag (UF) in register C to assert the IRQ\ pin low. The RESET pin going low or the SET bit going high clears the UIE bit.

SQWE: When the SQuare Wave Enable (SQWE) bit is set to logic one, a square wave signal at the rate selected by the rate selection bits is output to the SQW pin. When the SQWE bit is written to logic zero, the SQW pin is held low. The SQWE bit is cleared by the RESET pin. The SQWE bit is a read/write bit. Changes made to this bit while the SET bit is set to logic one will not take effect until the SET bit is written to logic zero.

DM: The Data Mode (DM) bit indicates whether the time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is a read/write bit that is not modified by RESET or internal functions of the RTC module. A logic one written to the DM bit selects the binary data format while a logic zero selects the BCD format. Changes made to this bit while the SET bit is set to logic one will not take effect until the SET bit is written to logic zero.

24/12: The 24/12 control bit selects the format of the hours byte. A logic one selects the 24-hour mode and a logic zero selects the 12-hour mode. This bit is a read/write bit that is not affected by RESET or internal functions of the RTC module.

REGISTER C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

DSE: The Daylight Savings Enable (DSE) bit is a read/write bit that enables two special updates when the DSE bit is set to logic one. On the first Sunday in April, the time increments from 1:59:59 am to 3:00:00 am. On the last Sunday in October when the time first reaches 1:59:59 am, it changes to 1:00:00 am. These special updates do not occur when the DSE bit is logic zero. This bit is a read/write bit that is not modified by RESET or internal functions of the RTC module.

IRQF: The Interrupt ReQuest Flag (IRQF) bit is set to logic one when one or more of the following conditions are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

That is, IRQF = PF x PIE + AF x AIE + UF x UIE.

Any time the IRQF bit is logic one, the IRQ\ pin is driven low. All flag bits are cleared to logic zero after reading register C or when the RESET pin is low.

PF: The Periodic interrupt Flag (PF) is a read-only bit that is set to logic one when an edge occurs on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic divide rate. The PF bit is set to logic one independent of the state of the PIE bit. When both the PF and PIE bits are set to logic one, the IRQ\ signal is asserted and the IRQF bit is set to logic one. The PF bit is cleared by a hardware RESET or by a read of register C.

AF: The Alarm interrupt Flag (AF) is set when the current time matches the alarm register time. If the AIE bit is also set to logic one, the IRQ\ pin is driven low and the IRQF bit is set to logic one. The AF bit is cleared by a hardware RESET\ or by a read of register C.

REGISTER D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

UF: The Update ended interrupt Flag (UF) is set after each update cycle. If the UIE bit is also set to logic one, the IRQ\ pin is driven low and the IRQF bit is set to logic one. The UF bit is cleared by a hardware RESET or by a read of register C.

Bits 3 through 0: The remaining bits in register C are read only and will always read logic zero.

VRT: The Valid RAM and Time (VRT) bit is set to the logic one state by the manufacturer prior to shipment. This is a read-only bit and should always read logic one as long as the internal lithium energy source is capable of retaining nonvolatile RAM and keeping time. If a logic zero is read, contents of the time and RAM data registers are questionable. This bit is not affected by the RESET pin.

Bits 6 through 0: The remaining bits in register D are read-only and will always read logic zero.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} Pin Potential to Ground Pin	-0.3 to + 7V
Input Voltage	V_{SS}-0.3 to V_{DD} + 0.3V
Power Dissipation	500mW
Storage Temperature	-40 to +70°C
Ambient Temperature	0 to +70°C
Soldering Temperature	260° for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0 to 70°C)

CHARACTERISTIC	TEST CONDITION	SYM	MIN.	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	10
Input High Voltage	Recognized as a High Signal Over Recommended V_{DD} and t_A Range	V_{IH}	2.2	V_{DD}+ 0.3	V V	
Input Low Voltage	Recognized as a Low Signal Over Recommended V_{DD} and t_A Range	V_{IL}	-0.3	-0.8	V	
Battery Voltage		V_{BAT}	2.0	3.4	V	

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0V +/- 10%, V_{SS}=0V, t_A=0 to 70°C)

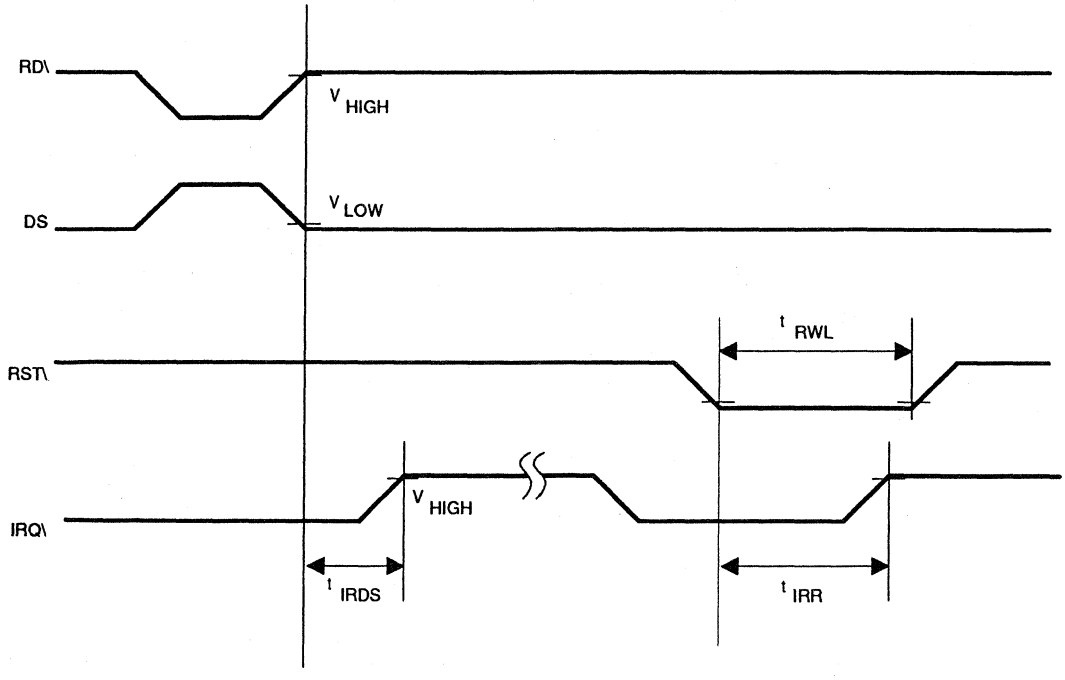
CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT
Input Leakage V_{IL}=OV, V_{IH}=V_{DD}	RST\ for any Single Pin: D0-7, RD\, WR\, A0-5, XRAM\, RTC\	I_I		+\-1	uA
Output High Voltage	V_{DD}=5.0V I_{LOAD} =1 mA	V_{OH}	2.4		V
Output Low Voltage	V_{DD} = 5.0V I_{LOAD} = 4 mA	V_{OL}		0.4	V
Power Supply Current	Outputs Unloaded	I_{DD}		50	mA
Input Current	STBY\=V_{DD}	I_{STBY}		-1	uA
Input Current	STBY\=V_{SS}	I_{STBY}		+500	uA

AC SWITCHING CHARACTERISTICS

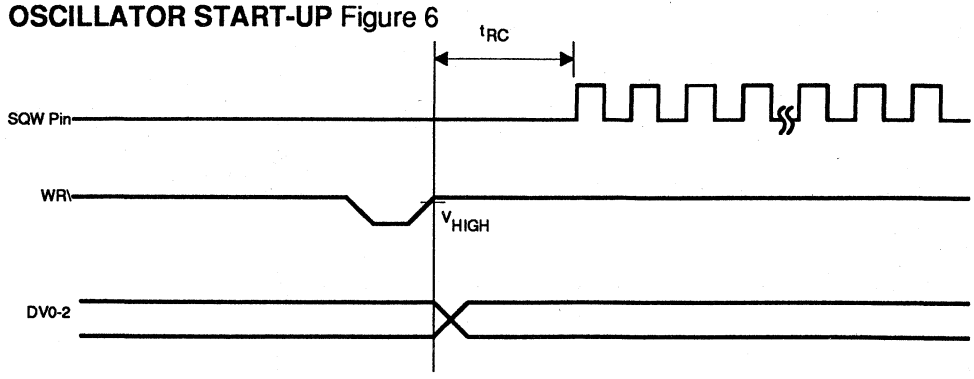
(0°C to 70°C, V_{DD}=4.5V to 5.5V)

CHARACTERISTIC	TEST CONDITION	SYM	MIN	MAX	UNIT
Reset Pulse Width		t_{RWL}	5		us
Oscillator Startup	From Software Enable Via DV Bits	t_{RC}		1	s
IRQ Release From DS Low		t_{IRDS}		2	us
IRQ Release From RESET\ Low		t_{IRR}		2	us
VRT Bit Delay	Lithium Source < 2.5V	t_{VRTD}		2	us

IRQ RELEASE DELAY Figure 5



OSCILLATOR START-UP Figure 6



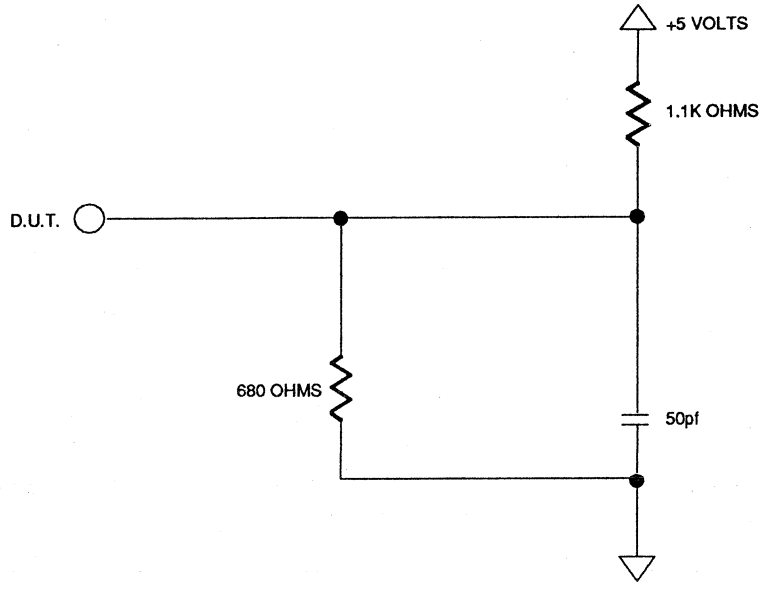
NOTE:
Timing assumes RS3-0 Bits = 0011, minimum t_{PI}.

BUS TIMING

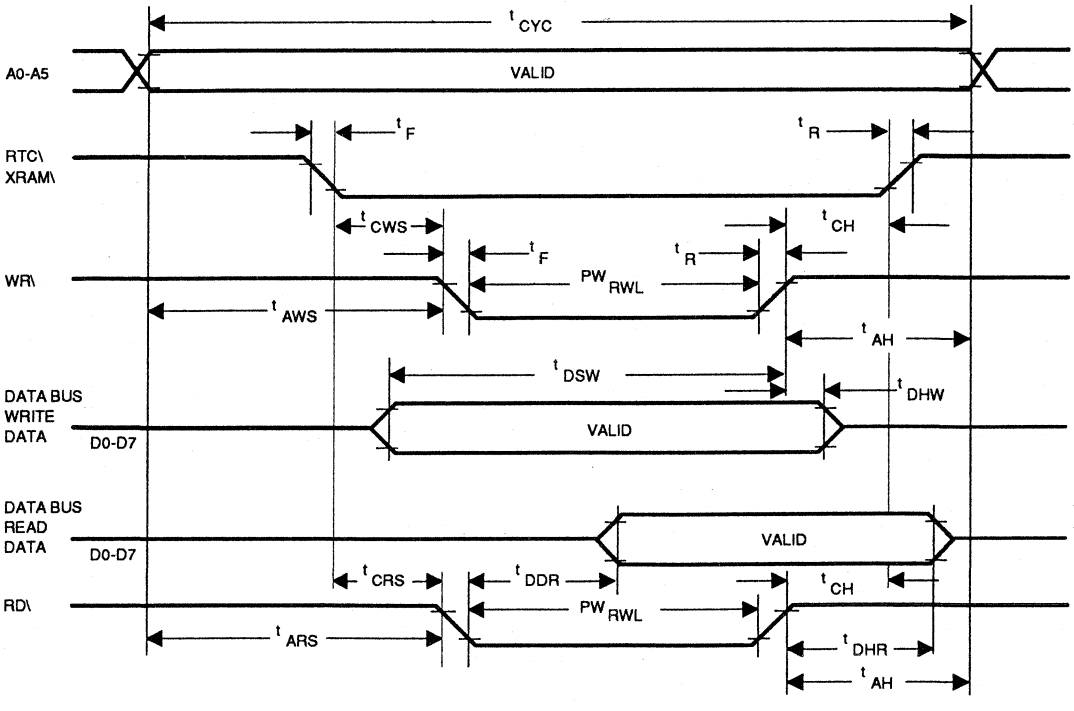
(0° to 70°C, V_{DD}=4.5V to 5.5V)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Cycle Time	t_{CYC}	395	DC	ns
Pulse Width, RD/WR Low	PW_{RWL}	200		ns
Signal Rise and Fall Time,RTC\,XRAM\,RD\,WR\	t_R, t_F		30	ns
Address Hold Time	t_{AH}	20		ns
Address Setup Time Before RD\	t_{ARS}	50		ns
Address Setup Time Before WR\	t_{AWS}	0		ns
Chip Select Setup Time Before RD\	t_{CRS}	50		ns
Chip Select Setup Time Before WR\	t_{CWS}	0		ns
Chip Select Hold Time After RD\ or WR\	t_{CH}	20		ns
Read Data Hold Time	t_{DHR}	10	100	ns
Write Data Hold Time	t_{DHW}	0		ns
Peripheral Output Data Delay Time From RD (See Figure 4)	t_{DDR}	20	240	ns
Peripheral Write Data Setup Time	t_{DSW}	200		ns

OUTPUT LOAD Figure 7



BUS READ/WRITE TIMING Figure 8



POWER-DOWN/ POWER-UP TIMING

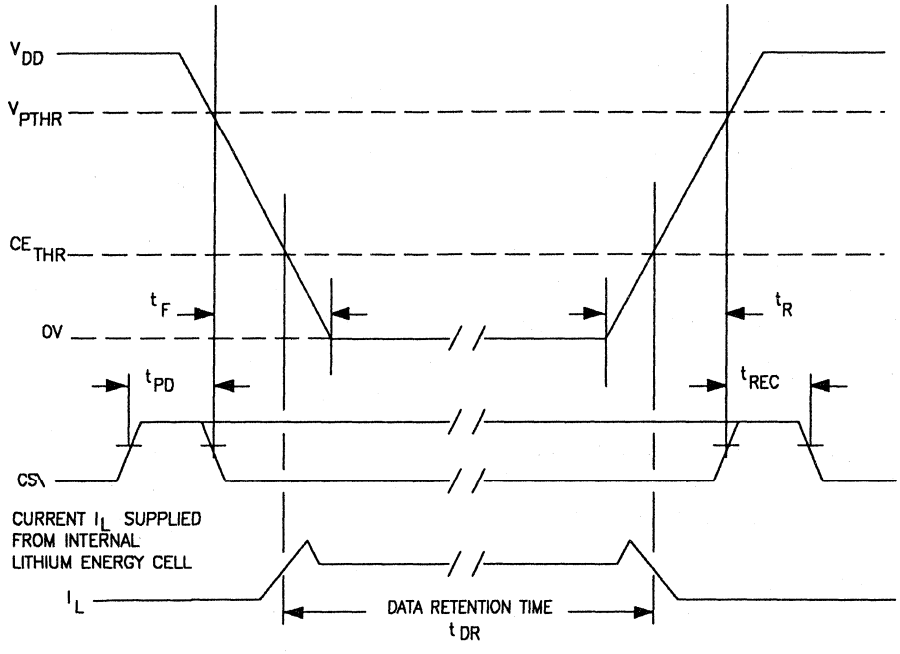
PARAMETER	SYM	MIN	MAX	UNIT
CE False before Power-Down	t_{PD}	0		us
V_{DD} Slew From 4.5V to 0.0V (CE False)	t_F	300		us
V_{DD} Slew Rate From 0.0V to 4.5V (CE False)	t_R	100		us
CE True After Power-Up	t_{REC}	20	200	ms

GENERAL INFORMATION

CE = Chip Enabled for access, i.e., (RD\ + WR) (XRAM\ + RTC\)

Expected Data Retention @ 25°C (DS1397 only)	t_{DR}	10		Years
Clock Accuracy for t_{DR} @ 25°C (DS1397 only)	C_Q	+/-1		Min/Mo
Clock Accuracy Temperature Coefficient (DS1397)	K		.050	ppm/°C²
Clock Temperature Coefficient Turnover Temperature (DS1397 only)	t_O	20	30	°C
Chip Power Switch Threshold	V_{PTHR}	V_{BATT}+/-50	Max	mV
Chip Enable Threshold (DS1397 only)	CE_{THR}	4.0	4.5	V

POWER-DOWN/POWER-UP CONNECTION Figure 9



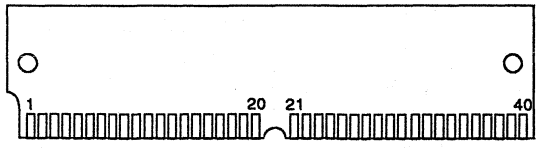
DALLAS SEMICONDUCTOR

DS2286
CPU Supervisory Stik

FEATURES

- Keeps track of time from 1/100 of a second up to the year
- Maintains 8K of setup information for personalization
- Senses switch closure and supplies energy pulse to start power supply when power is off
- Permanently powered with a lifetime lithium energy source
- Monitors microprocessor's vital signs for out-of-tolerance incoming power and errant software execution
- Orchestrates start-up and halting of the microprocessor
- Accommodates pushbutton reset input
- Alarm function schedules real time related activities
- Low-power CMOS; TTL-compatible
- Programmable interrupts and square wave output
- Conforms to standard 40-position JEDEC connection scheme
- Suitable for battery-powered applications

PIN DESCRIPTION



PIN NAMES (\ Denotes Condition Low)

PIN	DESC.	PIN	DESC.
1	A0	21	DQ6
2	A1	22	DQ7
3	A2	23	CER\
4	A3	24	OE\
5	A4	25	WE\
6	A5	26	CET\
7	A6	27	INTP\
8	A7	28	INTB\ (INTB)
9	A8	29	SQW\
10	A9	30	RST\
11	A10	31	PBRST\
12	A11	32	PF
13	A12	33	PF\
14	DQ0	34	PSI\
15	DQ1	35	PSO\
16	DQ2	36	IN
17	DQ3	37	NMI\
18	DQ4	38	ST\
19	DQ5	39	WC\ /SC
20	GND	40	V_{CC}

DESCRIPTION

The DS2286 CPU Supervisory Stik watches over the performance of a computer system, directs its activity, supplies up-to-date information for personalization, and turns the system off and on based on preprogrammed information. All of the permanently powered functions of the system are grouped together and kept alive with a self-contained, lithium energy source. These functions include a real time clock for time and date stamping, 8K X 8 of nonvolatile static RAM

PIN DESCRIPTION DETAIL

PIN #	NAME	I/O	DESCRIPTION
1-13	A0-A12	I	Address
14-19	DQ0-DQ6	I/O	Data Bus
20	GND	-	Ground
21	DQ6	I/O	Data
22	DQ7	I/O	Data
23	CER\	I	Chip Enable
24	OE\	I	Output Enable
25	WE\	I	Write Enable
26	CET\	I	Chip Enable Time
27	INTP\	O	Interrupt A
28	INTB\ (INTB)	O	Interrupt B
29	SQW\	O	Square Wave Out
30	RST\	I	Reset
31	PBRST\	I	Pushbutton Reset
32	PF	O	Power Fail
33	PF\	O	Power Fail
34	PSI\	I	Power Supply Input
35	PSO\	O	Power Supply Output
36	IN	I	Early Warning In
37	NMI\	O	Nonmaskable Interrupt
38	ST\	I	Strobe Input
39	WC\ /SC	I	Wakeup Control
40	V_{CC}	I	Power

(SRAM) for personalization and configuration, a watchdog timer for monitoring software execution, a power supply monitor, a kickstart energy pulse that can turn the system on or off under preprogrammed conditions, and finally, pushbutton and reset control of the microprocessor. The 40-position CPU Supervisory Stik uses a parallel access system identical to standard bytewide SRAM, providing high performance and a simple interface.

OPERATION

The three main elements of the DS2286 CPU Supervisory Stik are the DS1239 MicroManager Chip, DS1283 Watchdog Timekeeper, and Nonvolatile Static RAM (Figure 1). Operation of each of these is described below.

MicroManager

The DS2286 contains 8K X 8 of nonvolatile SRAM. Key to the maintenance of this SRAM is the DS1239 MicroManager Chip, which performs several functions within the Stik and for circuits external to the Stik. The IN pin samples upstream power supply conditions either from an AC power source or a higher level DC power source from which Vcc is derived. When the IN pin senses that the power source is going off line, the MicroManager warns the processor of impending power loss via the Non-Maskable Interrupt (NMI\) pin. Data is maintained within SRAM when external Vcc is absent by a lithium energy cell on the DS2286 under the supervision of the MicroManager. As Vcc goes to an out-of-tolerance condition (below 4.5 volts), the DS1239 inhibits access to RAM via the Chip Enable Input, thus protecting RAM against inadvertent data loss. At this time the Power-Fail Output (PF\) is driven low and remains low until Vcc is restored to nominal limits. As the Vcc supply falls below the level of the lithium energy cell, power is switched from Vcc to the lithium cell. When Vcc returns to nominal limits, the lithium cell is disconnected and Vcc is restored to RAM. SRAM is kept in write-protect for 100 nS minimum after Vcc is restored to nominal limits while the RST\ signal holds the processor in reset for 100 ms minimum.

In addition to managing RAM, the DS1239 also provides a watchdog function for a microprocessor. The Strobe Input (ST) must be toggled (high to low) within a 200 ms window or the RST\ output will be driven low for 50 ms minimum. In

this manner, errant software execution can be detected and stopped; the system then automatically restarts. The DS1239 can also perform the system watchdog function. If use of this pin is not desired, the ST\ input can be left floating, which will disable this function.

Another feature of the DS1239 is a Power Supply Wakeup Signal. The Power-Up Input Signal (PSI\) is a level-sensitive input that is internally pulled up to a high level. When this input is momentarily pulled to low level via a contact closure or one of the interrupts of the DS1283, the Power-Up Output Signal (PSO\) will send out a 1.7 volt pulse for 200 ms with a source current of 10 mA minimum from the lithium energy cell. Once the power supply is up, PSO\ is maintained at high level by Vcc until PSI\ is again momentarily pulled low, which will return PSO\ to low level. This feature allows for the power supply to be kick started from the lithium energy cell when Vcc power is absent. When this feature is not needed, PSI\ should be left in a high impedance state. The wake/sleep control (WC/SC\) provides a method for a microprocessor to put the DS1239 in low-power mode for battery-operated applications. This pin should be left floating when not in use. For more details on operational and electrical characteristics of the DS1239 MicroManager, please consult the data sheet on this device.

Watchdog Timekeeper

The DS2286 performs real time timekeeping and has a sophisticated interrupt capability based on watchdog duties and real time occurrences. These functions are accomplished with the DS1283 Watchdog Timekeeper Chip, which has a bytewide bus structure and control signals CET\, OE\, and WE\. The 64 8-bit registers within the DS1283 are accessed in the same manner as bytewide SRAM. Both interrupts and the watchdog timer are completely programmable. A 32.768 crystal is provided on the Stik that provides the time base for timekeeping. The DS1283 as connected on the Stik functions exactly like the DS1286 Watchdog Timekeeper. For more details on the operational and electrical characteristics of the DS1286 and DS1283, please consult the data sheets.

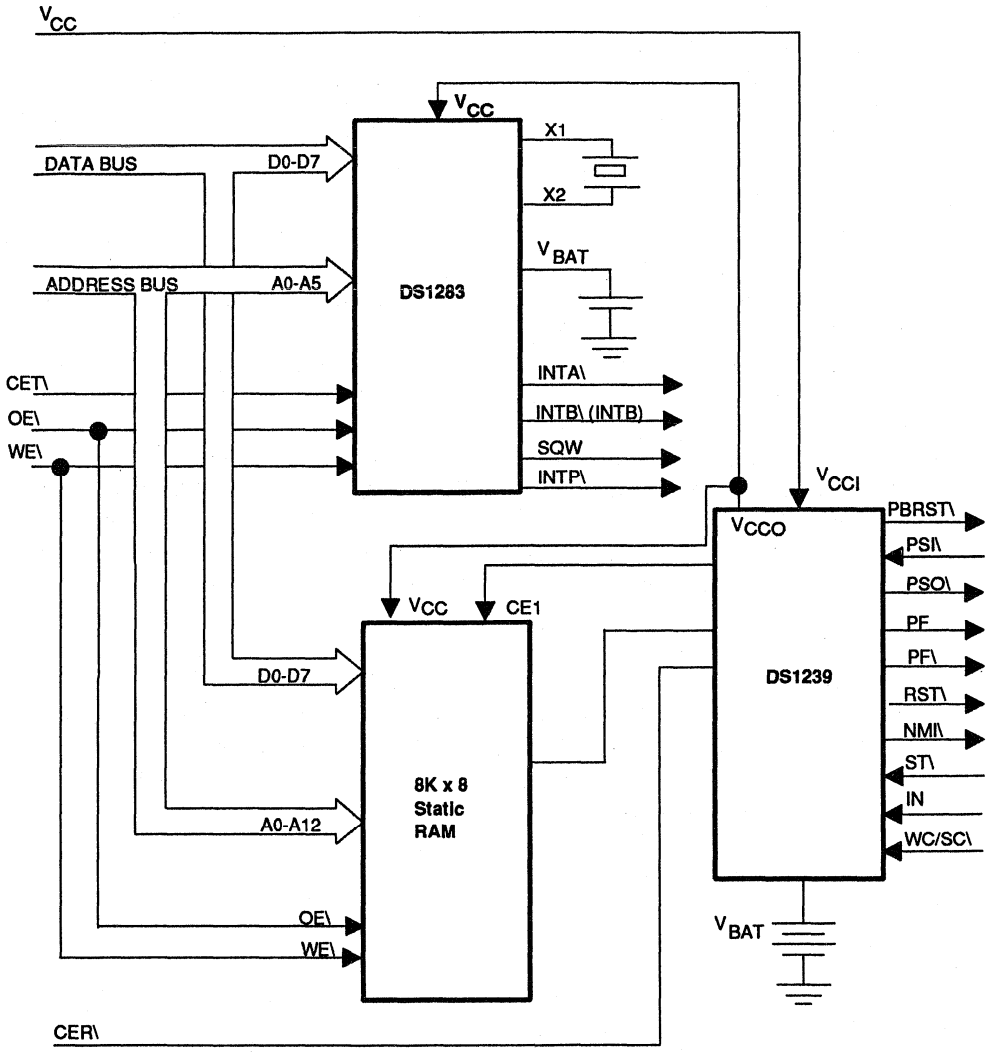
Nonvolatile Static RAM

The DS2286 contains 8K X 8 bytes of nonvolatile SRAM. The RAM is a standard bytewide memory accessed via the parallel address and data bus using the control signals CER\, OE\, and WE\.

SPECIFICATIONS

Both DC and AC electrical characteristics are covered in the respective data sheets for components used on the CPU Supervisory Stik and are not repeated in this text.

BLOCK DIAGRAM Figure 1



DALLAS SEMICONDUCTOR

DS2287
CPU Supervisory Stik

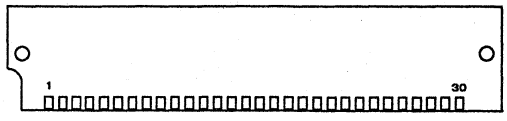
FEATURES

- Keeps track of time from seconds to years with leap year compensation
- Maintains 8K or 32K bytes of setup information for personalization
- Permanently powered with a lifetime lithium energy source
- Senses switch closure and supplies energy pulse to start power supply when power is off
- Monitors microprocessor's vital signs for out-of-tolerance incoming power and errant software execution
- Orchestrates start-up and halting of the microprocessor
- Multiplex address and data bus reduces pin count
- Accommodates pushbutton reset input
- Low-power CMOS
- Conforms to standard 30-position JEDEC connection scheme

DESCRIPTION

The DS2287 CPU Supervisory Stik watches over the performance of a computer system, directs its activity and supplies up-to-date information for personalization. All of the permanently-powered functions of the system are grouped together and kept alive with a self-contained, lithium energy source. These functions include a real time clock for time and date stamping, 8K x 8 or 32K x 8 of nonvolatile static RAM for personalization and configuration, a watchdog timer for monitoring software execution, a power supply monitor, a kickstart energy pulse that can be used to turn on the system, and a pushbutton reset control for the microprocessor. The 30-pin CPU Supervisory Stik uses a multiplex address and data bus to accommodate maximum functionality with minimum pin count.

PIN DESCRIPTION



PIN NAMES (\ Denotes Condition Low)

PIN#	SIGNAL	PIN#	SIGNAL
1	OER\	16	IRQ\
2	AD0	17	AS0\
3	AD1	18	AS1\
4	AD2	19	SQW
5	AD3	20	Vcc
6	AD4	21	PF\
7	AD5	22	IN
8	AD6	23	PSI\
9	AD7	24	PS0
10	CS\	25	NMI\
11	GND	26	ST\
12	AS\	27	RST\
13	R/W\	28	PBRST\
14	DS\	29	PF
15	WER\	30	GND

ORDERING INFORMATION

DS2287-8	8K x 8 CPU Supervisory Stik
DS2287-32	32K x 8 CPU Supervisory Stik

PIN DESCRIPTION DETAIL

PIN#	NAME	I/O	DESCRIPTION
1	OER\	I	**Output Enable.**
2-9	AD0-AD7	I/O	**Address.**
10	CS\	I	**Chip Select.**
11	GND	-	**RTC Ground.**
12	AS\	I	**Address Strobe.**
13	R/W\	I	**Read/Write Clock.**
14	DS\	I	**Data Strobe.**
15	WER\	I	**Write Enable RAM.**
16	IRQ\	O	**Interrupt Request.**
17-18	AS0\-AS1\	I	**Address Strobe.**
19	SQW	O	**Square Wave.**
20	V_{cc}	I	**Power.**
21	PF\	I	**Power Fail Input.**
22	IN	I	**Voltage Sense Input.**
23	PSI\	I	**Power Supply.**
24	PSO	O	**Power Supply.**
25	NMI\	O	**Nonmaskable Interrupt.**
26	ST\	I	**Strobe.**
27	RST\	O	**Reset.**
28	PBRST\	I	**Pushbutton Reset.**
29	PF	O	**Power Fail.**
30	GND	-	**Ground.**

OPERATION

The three main elements of the DS2287 CPU Supervisory Stik are the DS1239 MicroManager, DS1285 Real Time Chip, and nonvolatile SRAM (Figure 1). Operation of each of these is described below.

MicroManager

The DS2287 contains 8K or 32K X 8 of nonvolatile SRAM. Key to the maintenance of this SRAM is the DS1239 MicroManager, which performs several functions within the Stik and for circuits external to the Stik. The IN pin samples upstream power supply conditions either from an AC power source or a higher level DC power source than V_{cc}. When the IN pin senses that the power source is going off line, the MicroManager warns the processor of impending power loss via the Non-Maskable Interrupt (NMI\). As power is lost, V_{cc} goes low. When V_{cc} drops below 4.5 volts, the Reset Output (RST\) goes to the active level, terminating processor activity.

In the absence of external V_{cc}, a lithium energy cell on the DS2287 maintains data within SRAM under the supervision of the MicroManager. As the V_{cc} supply falls below the level of the lithium energy cell, power is switched from V_{cc} to the lithium cell. When V_{cc} returns to nominal limits, the lithium cell is disconnected and V_{cc} is restored to RAM.

When V_{cc} drops to an out-of-tolerance condition (below 4.5 volts), the DS1239 inhibits access to RAM via the chip enable input, thereby protecting RAM from inadvertent data loss. At this time, the Power-Fail Output (PF\) is driven low; it remains low until V_{cc} is within nominal limits.

The SRAM is kept in write-protect for 100 ns minimum after V_{cc} is restored to nominal limits; the RST\ signal holds the processor in reset for 100 ms minimum.

In addition to managing RAM, the DS1239 provides a watchdog function for the microprocessor. The Strobe Input (ST\) must be toggled (high to low) within a 200 ms window or the RST\ will be driven low for 50 ms minimum. In this manner, errant software execution can be detected and stopped; the system will then automatically restart. If this feature is not desired, the ST\ can be left floating, which will disable the watchdog timer.

Another feature of the DS1239 is a Power Sup-

ply Wakeup Signal. The Power-Up Input Signal (PSI\) is a level-sensitive input that is internally pulled up to a high level. When this input is momentarily pulled to ground with a contact closure, the Power-Up Output (PSO) sends out a 1.7 volt pulse for 200 ms with a source current of 10 mA minimum. Once the power supply is up, PSO\ is maintained at high level by V_{CC} until PSI\ is again momentarily pulled low, which will return PSO to low level. This feature allows the power supply to be kick started from the lithium energy cell when V_{CC} power is absent. When this feature is not needed, the PSI\ should be left in a high impedance state. For more details on operational and electrical characteristics of the DS1239 Micro Manager, consult the data sheet on this device.

Real Time Clock

The CPU Supervisory Stik performs real-time timekeeping and has a sophisticated interrupt capability based on real time occurrences. This real time function is accomplished with the DS1285 Real Time Chip, which has a multiplex bus structure and its own set of control signals. A 32.768 MHz crystal mounted on the Stik supplies the time base for timekeeping. The DS1285 connected to the CPU Supervisory Stik functions exactly like the DS1287 Real Time Clock. For more details on operational and electrical characteristics of the DS1287, consult the data sheet on this device.

Nonvolatile Static RAM

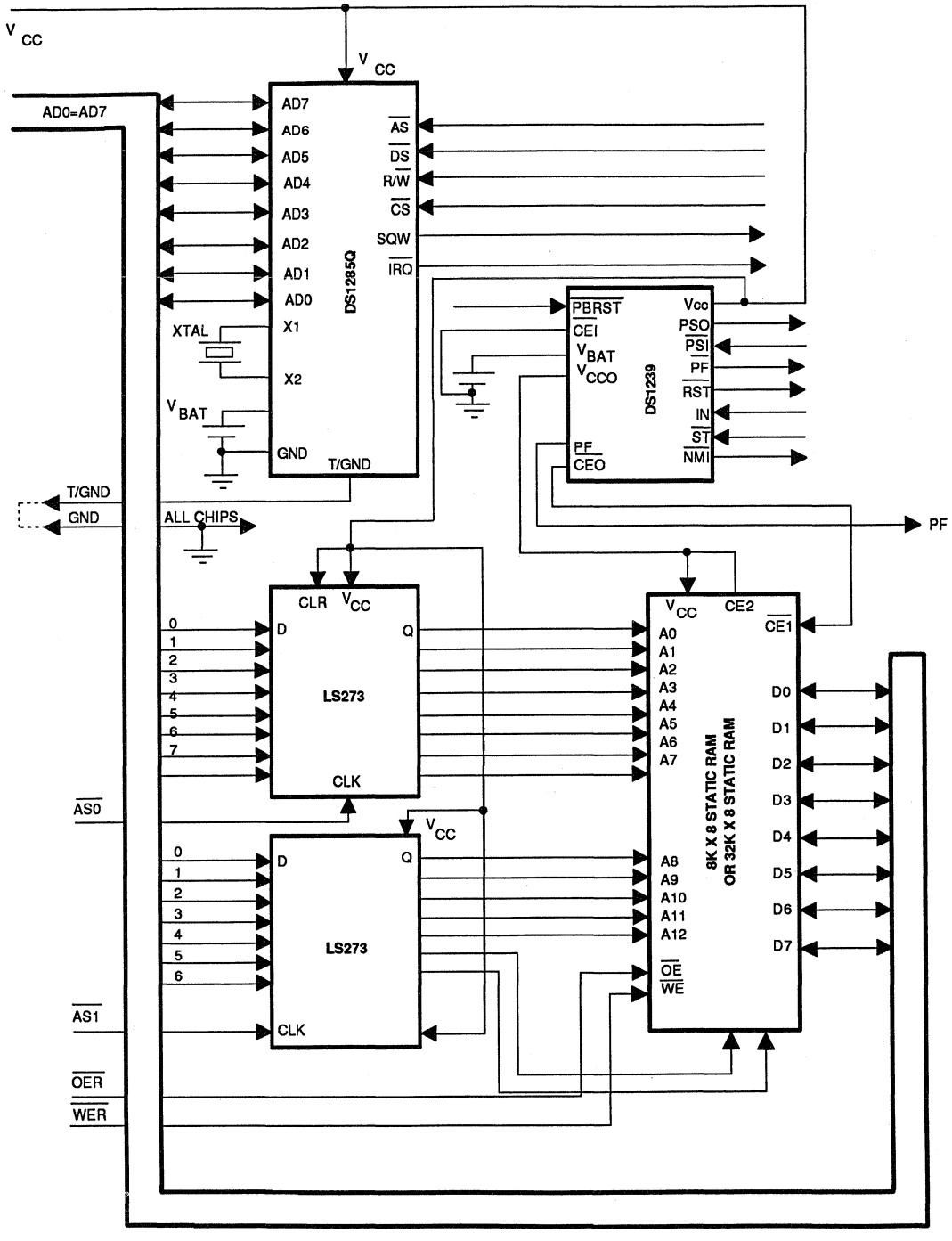
The DS2287 contains an 8K or 32K x 8 SRAM. This RAM is a standard bytewide memory and, therefore, has a non-multiplexed bus. Two 74L5273 "D"-type latches interface the SRAM with the multiplex 8-pin bus provided. On power-up the latches are cleared and enabled by the Power-Fail Signal (PF\). Each latch is controlled by signals called Address Strobe 0 (AS0\) and Address Strobe 1 (AS1\). Using these two latch controls and the two RAM control signals Output Enable RAM (OER\) and Write Enable RAM (WER\), it is possible to read or write RAM using three separate cycles (Figure 2). The first cycle is used to latch the lower order address using AS0\. It is only necessary to meet the setup and hold time with valid addresses on AD0-AD7 to accomplish this cycle.

In a similar manner, the upper-order addresses are latched using AS1\. The third cycle is for data transfer and occurs in one of two ways. If a write cycle is to occur, valid data is placed on the bus (AD0-AD7). The WER\ signal is then driven active and the data on the bus is written to RAM, provided RAM write timing specifications are met. If a read cycle is to occur, the OER\ is driven active, and data becomes valid on the bus (AD0-AD7) provided that proper RAM access time parameters are met. Note that WER\ and OER\ are never active at the same time.

Specifications

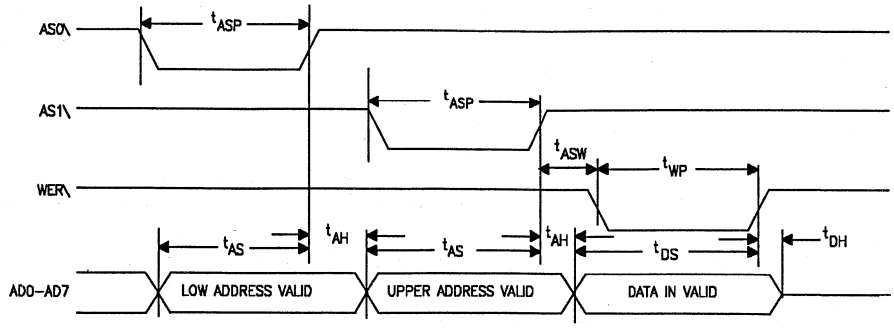
Both DC and AC electrical characteristics are covered in the respective data sheets for the DS1285 and the DS1239 and thus are not repeated in this text. The 74LS273 latches accept and input logic 1 at 2.0 volts at 40 uA and input logic 0 at 0.8 volts sinking 1.6 mA.

DS2287 BLOCK DIAGRAM Figure 1

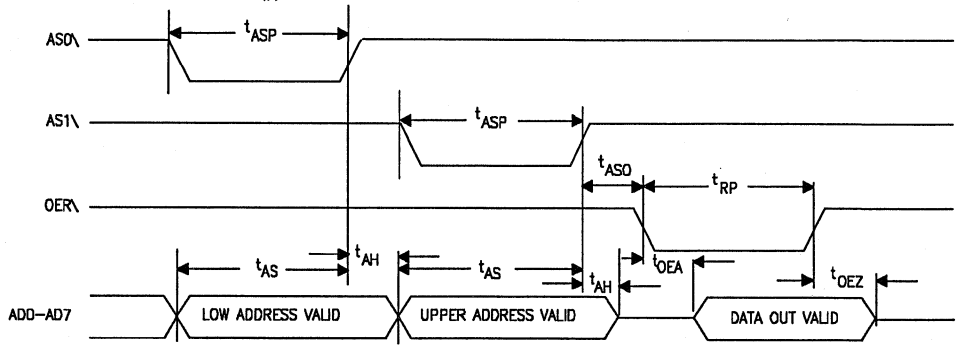


TIMING DIAGRAMS Figure 2

WRITE TIMING OER\ = V_{IH}



READ TIMING WER\ = V_{IH}



AC ELECTRICAL CHARACTERISTICS

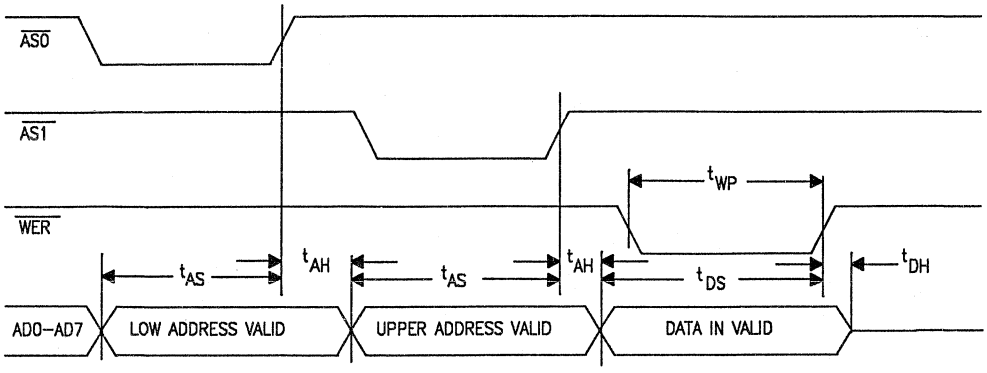
(0^0 to 70^0C, V_{CC}= 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX.	UNITS	NOTES
Address Setup Time	t_{AS}	50			ns	
Address Hold Time	t_{AH}	0			ns	
Data Setup Time	t_{DS}	75			ns	
Data Hold Time	t_{DH}	0			ns	
Output Enable Access	t_{OEA}			200	ns	
Write Pulse Width	t_{WP}	200			ns	
OER\ to Output in High Z	t_{OEZ}			50	ns	
READ Pulse Width	t_{RP}	200			ns	
AS0\ AS1\ Pulse Width	t_{ASP}	75			ns	
ASX\ High to OER\ Low	t_{ASO}	20			ns	1
ASX\ High to WER\ Low	t_{ASW}	20			ns	1

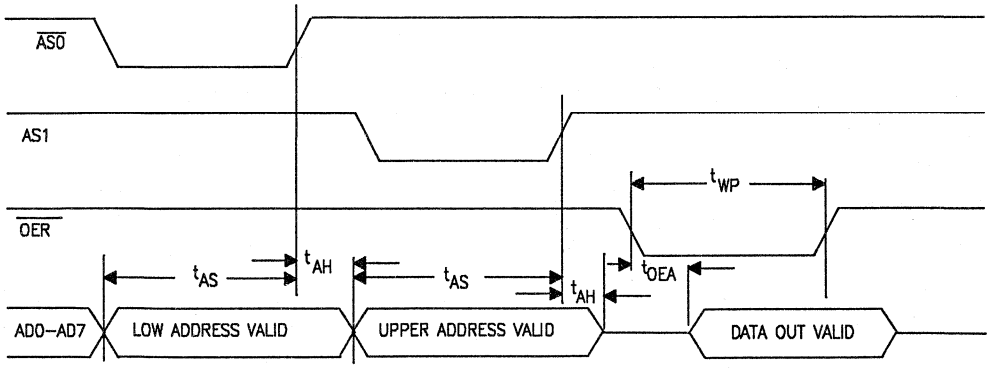
NOTE:

1. ASX\ is either AS0\ or AS1\.

WRITE TIMING OER = V_{IL} Figure 2



READ TIMING WER=V_{IH} Figure 3



User Insertable Memory

DALLAS SEMICONDUCTOR

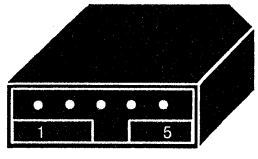
DS1201
Electronic Tag

FEATURES

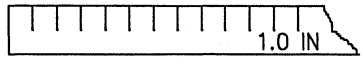
- User-insertable, nonvolatile 1024 bits of read/write memory
- Low-power CMOS circuitry allows for 10 years of data retention
- Miniature and transportable
- Durable and rugged
- Impervious to handling
- Four million bits/second data rate
- Single byte or multiple byte data transfer capability
- No restrictions on the number of write cycles
- Applications include software authorization, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record.

PACKAGE/PIN DESCRIPTION

SIDE



BOTTOM: PIN VIEW



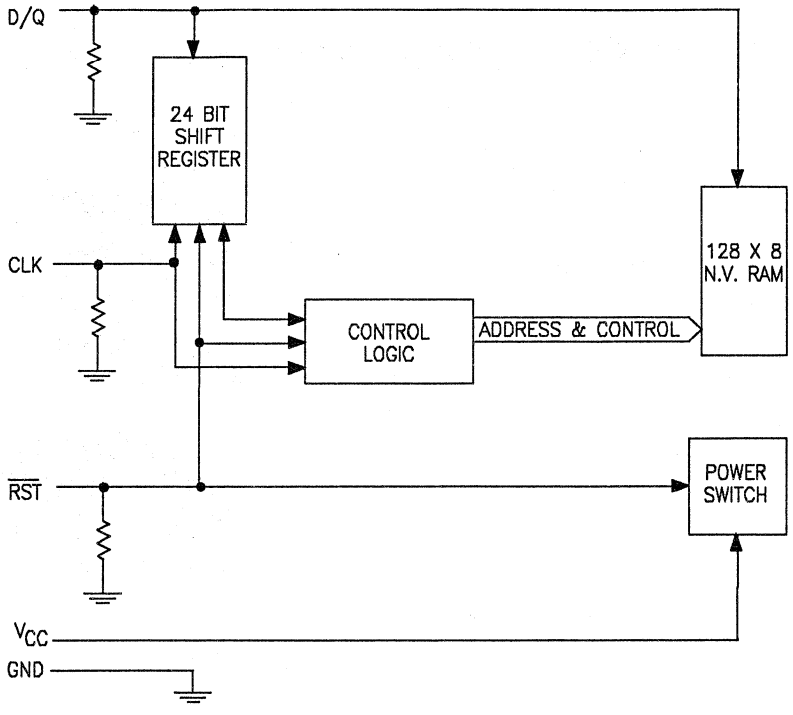
PIN NAMES (\ Denotes Condition Low)

Pin 1	Vcc	+5 Volts
Pin 2	RST\	RESET\
Pin 3	DQ	Data Input/Output
Pin 4	CLK	Clock
Pin 5	GND	Ground

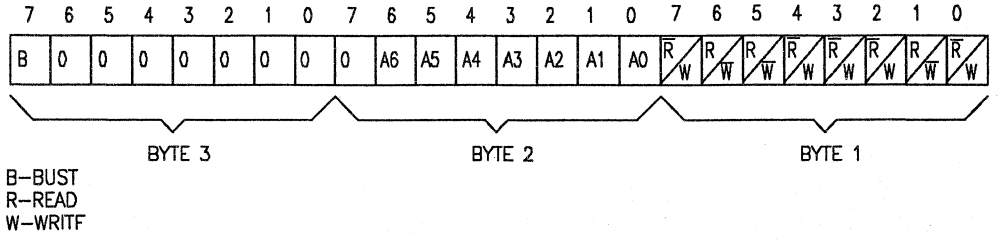
DESCRIPTION

The DS1201 Electronic Tag is a miniature nonvolatile, read/write memory system which can randomly access individual 8-bit strings (bytes) or sequentially access the entire 1024-bit contents (burst). Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLOCK, RESET\, and DATA INPUT/OUTPUT. Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user.

ELECTRONIC TAG BLOCK DIAGRAM Figure 1



ADDRESS/COMMAND Figure 2



OPERATION

The block diagram (Figure 1) of the Electronic Tag illustrates the main elements of the device: shift register, control logic, nonvolatile RAM, and power switch. To initiate a memory cycle RESET\ is taken high and 24 bits are loaded into the shift register, providing both address and command information. Each bit is serial input on the rising edge of the CLOCK input. Seven address bits specify one of the 128 RAM locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 CLOCKs which load the shift register, additional CLOCKs will output data for a read or input data for a write. The number of CLOCK pulses equals 24 plus 8 for byte mode or 24 plus 1024 for burst mode.

The tag can be used as a four-pin or five-pin device, depending on the application. For hard-wired applications, active power is supplied by the Vcc pin. Alternatively, for user-insertable applications, power can be supplied by the RESET\ pin.

ADDRESS/COMMAND

Each memory transfer consists of a three-byte address/command input called the address/command. The address/command is shown in Figure 2. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address/command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the tag are ignored until RESET\ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address inputs A0 in bit 0 through A6 in bit 6. Bit 7 of the second byte of the address/command word must be set to logic 0. This bit is reserved for future higher density versions of the tag. If bit 7 does not equal logic 0, the cycle is aborted and all future inputs to the tag are ignored until RESET\ is brought low and then high again to begin a new cycle. The third byte of the address/command is also set aside for future expansion. Bits 0 through 6 must be set to logic 0 or the cycle is aborted and all future inputs are ignored until RESET\ is brought low and then high again to begin a new cycle. Bit 7 of byte 3 of the address/command is used along with address bits A0 through A6 to define burst mode. When A0 through A6 equals logic 0 and bit 7 of byte 3 of the address command equals logic 1, the tag will enter the burst mode after the address/command sequence is complete.

BURST MODE

Burst mode is specified for the Electronic Tag when all address bits (A0-A6) of the address/command are set to logic 0 and bit 7 of byte 3 to logic 1. The burst mode causes 128 consecutive bytes to be read or written. Burst mode terminates when the RESET\ input is driven low.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RESET\ input high. The RESET\ input serves three functions. First, RESET\ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the RESET\ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for RESET\ of 2 mA @ 3.8 volts is required. However if the Vcc pin is connected to a 5-volt source within nominal limits, then the RESET\ pin is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 uA. Finally, the RESET\ signal provides a method of terminating either single byte or multiple byte data transfers. A CLOCK cycle is a sequence of falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the CLOCK cycle. Address/command bits and data bits are input on the rising edge of the CLOCK and data bits are output on the falling edge of the CLOCK. All data transfer terminates

if the RESET\ input is low and D/Q pin goes to a high impedance state. When data transfer to the tag is terminated using RESET\, the transition of RESET\ must occur while the clock is at high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 3.

DATA INPUT

Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next eight CLOCK cycles, assuming that the read/write and write/read bits are properly set (for data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1).

DATA OUTPUT

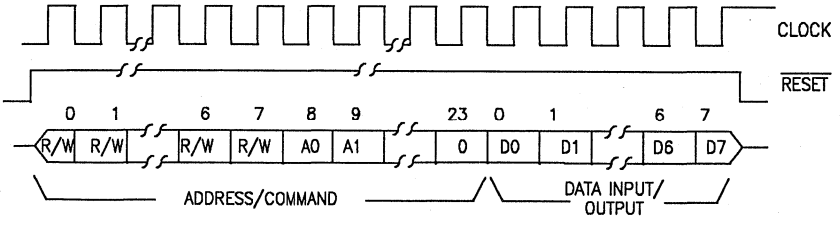
Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles (for data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0).

TAG CONNECTIONS

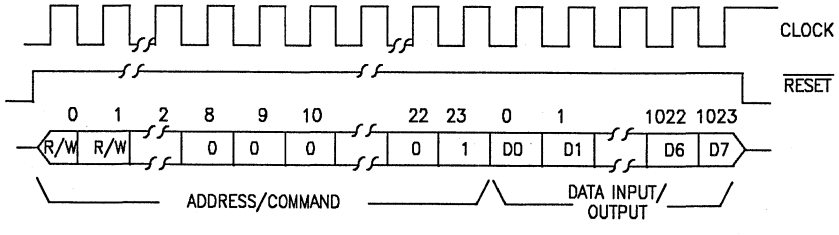
The tag is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A key is provided to prevent the tag from being plugged in backwards and to aid in alignment of the receptacle. For portable applications, contact to the tag pins can be determined to ensure connection integrity before data transfer begins. CLOCK, RESET\, and DATA INPUT/OUTPUT all have internal 40K ohm pulldown resistors to ground which can be sensed by a reading device.

DATA TRANSFER Figure 3

SINGLE BYTE TRANSFER



BURST MODE TRANSFER

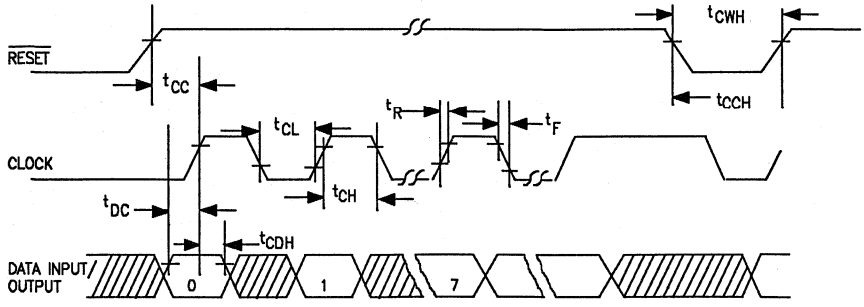


NOTES

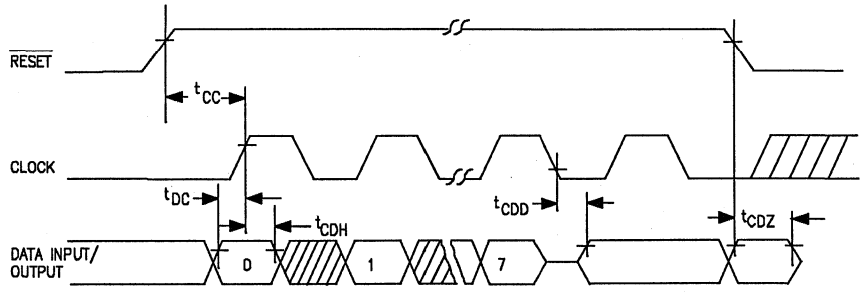
1. Data input sampled on rising edge of clock cycle.
2. Data output changes on falling edge of clock.

READ/WRITE DATA TRANSFER Figure 4

WRITE DATA TRANSFER



READ DATA TRANSFER



NOTES:

1. All voltages and resistances are referenced to ground.
2. Input levels apply to CLK, D/Q, and RST\ while V_{CC} is within nominal limits. When V_{CC} is not connected to the tag, then RST\ input reverts to V_{IHE}.
3. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10 ns maximum rise and fall time.
4. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
5. For CLK, D/Q, RST\ and V_{CC} at 5 volts.
6. Load capacitance = 50 pF.
7. Applies to RST\ when V_{CC} < 3.8 volts.
8. Measured with outputs open.
9. Measured at V_{IH} of RST; greater than or equal to 3.8V when RST\ supplies power.
10. Logic 1 maximum is V_{CC} + 0.3V if the V_{CC} pin supplies power and RST +0.3V if the RST\ pin supplies power.
11. RST\ logic 1 maximum is V_{CC} + 0.3V if the V_{cc} pin supplies power and 5.5V maximum if RST\ supplies power.
12. Each DS1201 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average AC RST\ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3})(C_L + 140)f$
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHz.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I_{TOTAL} current of 5 mA.
14. When RST\ is supplying power t_{CWH} must be increased to 100 ms.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground -1.0 TO +7.0v
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute manimum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1,2,10
Logic 0	V_{IL}	-0.3		0.8	V	1
RESET\ Logic 1	V_{IHE}	3.8			V	1,7,11
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_L			+500	uA	5
Output Leakage	I_{LO}			+500	uA	5
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
RST\ Input Resistance	Z_{RST}	10		40	K ohms	1
D/Q Input Resistance	Z_{DQ}	10		40	K ohms	1
CLK Input Resistance	Z_{CLK}	10		40	K ohms	1
Active Current	I_{CC1}			6	mA	8
Standby Current	I_{CC2}			2.5	mA	8
RST\ Current	I_{RST}				mA	7,8,13

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	3,9
Data to CLK Hold	t_{CDH}	40			ns	3,9
Data to CLK Delay	t_{CDD}			125	ns	3,4,6,9
CLK Low Time	t_{CL}	125			ns	3,9
CLK High Time	t_{CH}	125			ns	3,9
CLK Frequency	f_{CLK}	DC		4.0	MHz	3,9
CLK Rise & Fall	t_R,t_F			500	ns	9
RST\ to CLK Setup	t_{CC}	1			uS	3,9
CLK to RST Hold	t_{CCH}	40			ns	3,9
RST\ Inactive Time	t_{CWH}	125			ns	3,9,14
RST\ to I/O High Z	t_{CDZ}			50	ns	3,9
Expected Data Retention Time	t_{DR}	10			Years	12

DALLAS SEMICONDUCTOR

DS1217A
Nonvolatile Read/Write Cartridge

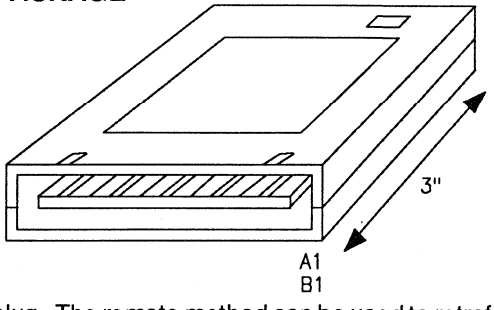
FEATURES

- User-insertable
- Capacity up to 32K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP socket via ribbon cable
- Data retention greater than 10 years
- Automatic write protection circuitry safeguards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0°C to 70°C

SIGNAL CONNECTIONS (\ Denotes Condition Low)

Name	Position		Name
Ground	A1	B1	No Connect
+5 Volts	A2	B2	Address 14
Write Enable\	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
Output Enable\	A8	B8	Address 3
Address 10	A9	B9	Address 2
Cartridge Enable\	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data (DQ0)
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

PACKAGE



DESCRIPTION

The DS1217A Nonvolatile Read/Write Cartridge is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge is available in density ranges from 2K x 8 to 32K x 8 in 8K byte increments. A card edge connector is required for connection to a host system; a standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a 28-conductor ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems that have JEDEC 28-pin bytewide memory sites.

The DS1217A cartridge has a lifetime energy source to retain data and circuitry needed to automatically protect memory contents. Reading and writing the memory locations is the same as using conventional static RAM. If the user wants to convert from read/write memory to read-only memory, a manual switch is provided to unconditionally protect memory contents.

READ MODE

The DS1217A is executing a read cycle whenever WE\ (write enable) is inactive (high) and CE\ (cartridge enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that CE\ and OE\ (output enable) access times are also satisfied. If OE\ and CE\ times are not satisfied, then data access must be measured from the latter occurring signal (CE\ or OE\); the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217A is in the write mode whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recover time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write protected.

DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217A constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM. To retain data during power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217A checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. For this reason, the cartridge provides battery redundancy. The DS1217A features an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts.

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems that contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin ribbon cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B15) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and driving circuitry is increased.

CARTRIDGE NUMBERING Table 1

PART NO.	DENSITY	UNUSED ADDRESS INPUTS
DS1217A/16K-25	2K x 8	*Address 11, 12, 13, 14
DS1217A/64K-25	8K x 8	*Address 13, 14
DS1217A/128K-25	16K x 8	*Address 14
DS1217A/192K-25	24K x 8	
DS1217A/256K-25	32K x 8	

*Unused address inputs must be held low (V_{IL}).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Connection Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		V_{CC}	V
Input Low Voltage	V_{IL}	0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-60		+60	uA
I/O Leakage Current $C_{EI} \geq V_{IH} \leq V_{CC}$	I_{IO}	-10		+10	uA
Output Current @ 2.4V	I_{OH}	-1.0			mA
Output Current @ 0.4V	I_{OL}	2.0			mA
Standby Current CE\=2.2V	I_{CCS1}		5.0	10	mA
Operating Current	I_{CCO1}		35	75	mA

CAPACITANCE

(t_A = 25°C)

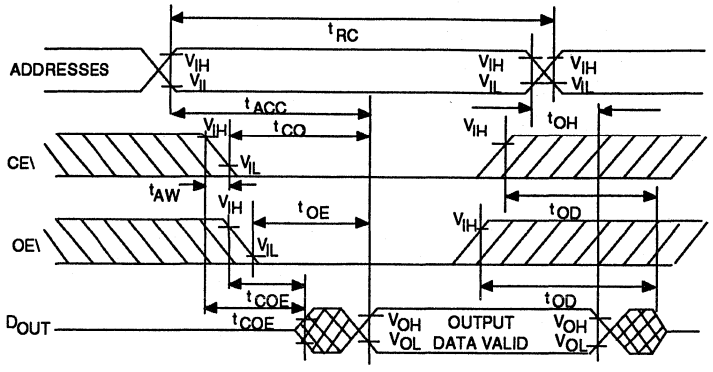
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	75	pF	
Input/Output Capacitance	$C_{I/O}$	75	pF	

AC ELECTRICAL CHARACTERISTICS

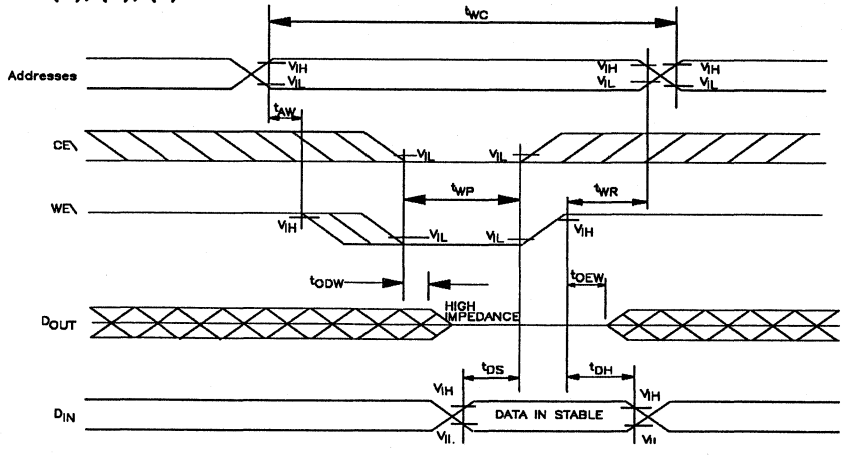
(0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			250	ns	
OE\ to Output Valid	t_{OE}			125	ns	
CE\ to Output Valid	t_{CO}			250	ns	
OE\ or CE\ to Output Active	t_{COE}	5			ns	5
Output High Z from Deselection	t_{OD}			125	ns	5
Output Hold from Address Change	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z from WE\	t_{ODW}			100	ns	5
Output Active from WE\	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time from WE\	t_{DH}	20			ns	4

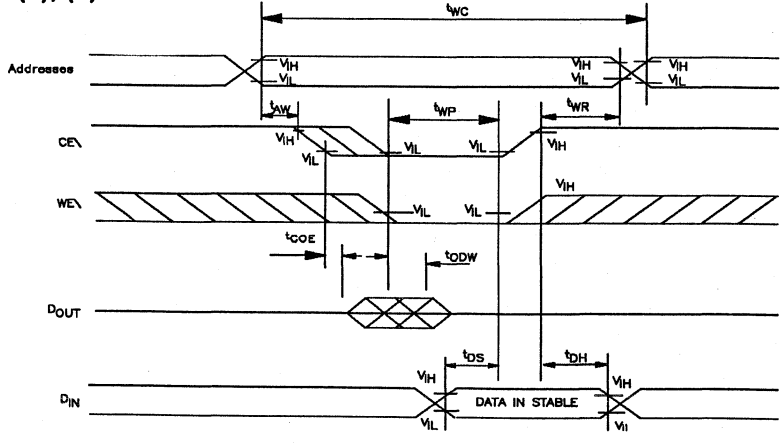
READ CYCLE (1)



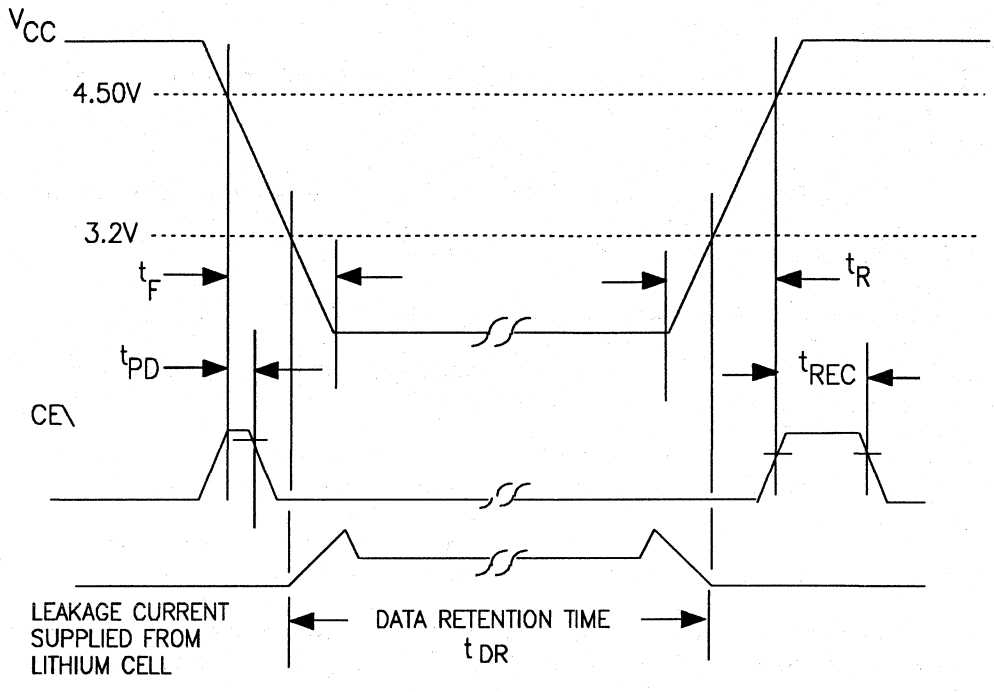
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		us	10
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	100		us	
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		us	
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	10

(t_A = 25°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when the device is in battery backup mode.

NOTES:

1. WE\ is high for a read cycle.

2. OE\ = V_{IH} or V_{IL}. If OE\ = V_{IH} during the write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of CE\ and WE\.
   t_{WP} is measured from the latter of CE\ or WE\ going low to the earlier of CE\ or WE\ going high.

4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.

5. These parameters are sampled with a 5pF load and are not 100% tested.

6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.

8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remains in a high impedance state during this period.

9. Each DS1217A is marked with a 4-digit date code AABB. AA designates the year of manufacture; BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

10. Removing and installing the cartridge with power applied may disturb data.

DC Test Conditions
Outputs Open
t Cycle = 250ns
All Voltages Are Referenced to Ground

AC Test Conditions
Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V

DALLAS SEMICONDUCTOR

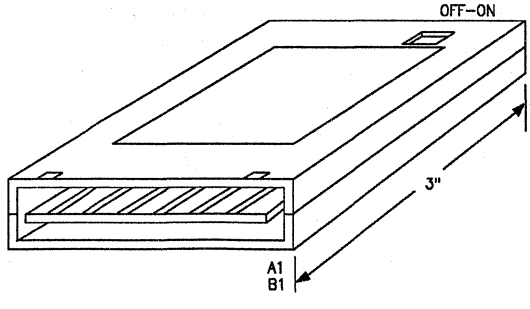
DS1217M
Nonvolatile Read/Write Cartridge

FEATURES
- User-insertable
- Data retention greater than 5 years
- Capacity up to 512K x 8
- Standard bytewide pinout facilitates connection to JEDEC 28-pin DIP via ribbon cable
- Software-controlled banks maintain 32 x 8 JEDEC 28-pin compatibility
- Multiple cartridges can reside on a common bus
- Automatic write protection circuitry safe-guards against data loss
- Manual switch unconditionally protects data
- Compact size and shape
- Rugged and durable
- Wide operating temperature range of 0-70°C

PIN DESCRIPTION

NAME	POSITION	NAME
Ground	A1 / B1	No Connect
+5 Volts	A2 / B2	Address 14
Write Enable	A3 / B3	Address 12
Address 13	A4 / B4	Address 7
Address 8	A5 / B5	Address 6
Address 9	A6 / B6	Address 5
Address 11	A7 / B7	Address 4
Output Enable	A8 / B8	Address 3
Address 10	A9 / B9	Address 2
Cartridge Enable	A10 / B10	Address 1
Data I/O 7	A11 / B11	Address 0
Data I/O 6	A12 / B12	Data I/O 0
Data I/O 5	A13 / B13	Data I/O 1
Data I/O 4	A14 / B14	Data I/O 2
Data I/O 3	A15 / B15	Ground

PACKAGE



DESCRIPTION
The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 64K x 8 to 512K x 8. The cartridge is accessed in continuous 32K byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30 pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems which have JEDEC 28-pin bytewide memory sites.

READ MODE

The DS1217M is executing a read cycle whenever WE\ (write enable) is inactive (high) and CE\ (cartridge enable) is active (low). The unique address specified by the address inputs (A0-A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that CE\ (cartridge enable) and OE\ (output enable) access times are also satisfied. If OE\ and CE\ times are not satisified, then data access must be measured from the late occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is inhibited and all accesses are ignored.

WRITE MODE

The DS1217M is in the write mode whenever both WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\. All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated.The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 volts. When V_{CC} is less than 4.5 volts, the memory is write-protected.

DATA RETENTION MODE

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.5 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5 volts. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge thus has redundant batteries and an internal isolation switch which provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0 volts.

BANK SWITCHING

Bank switching is accomplished via address lines A8, A9, A10, and A11. Initially, on power-up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64-bit pattern which will set the band switch, a read cycle of 1111 (address inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 3 bits. Each set of address inputs is entered into the DS1217M by executing read cycles.The first eleven cycles

must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10, and A11. However, address line 8 defines which of the 16 banks is to be enabled, or all banks are deselected, as per Table 3. Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See DS1222 BankSwitch Chip data sheet for more detail.)

REMOTE CONNECTION VIA A RIBBON CABLE

Existing systems which contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right-justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B1) on the card edge connector should be grounded to futher enhance data integrity. Access time push-out may occur as the distance between the cartridge and the driving circuitry is increased.

TABLE 1 - CARTRIDGE NUMBERING

PART NO.	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64K x 8	2
DS1217M 1-25	128K x 8	4
DS1217M 2-25	156K x 8	8
DS1217M 3-25	384K x 8	2
DS1217M 4-25	512K x 8	16

TABLE 2 - ADDRESS INPUT PATTERN

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A9	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1	1
A10	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A11	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

TABLE 3 - BANK SELECT TABLE

BANK	A8 BIT SEQUENCE				
SELECTED	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	1	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

ABSOLUTE MAXIMUM RATINGS*

Voltage on Connection Relative to Ground	-0.3V to +7.0V
Operation Temperature	0°C to 70°C
Storage Temperature	-50°C to +70°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliabilty.

RECOMMENDED DC OPERATION CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2		V_{CC}	V
Input Low Voltage	V_{IL}	0.0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V + /-10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-60		+60	uA
I/O Leakage Current CE\ ≥ V_{IH} ≤ V_{CC}	I_{IO}	-10	+10		uA
Output Current @ 2.4V	I_{OH}	-1.0			mA
Output Current @ 0.4V	I_{OL}	2.0			mA
Standby Current CE\ = 2.2V	I_{CCS1}		15	25	mA
Operating Current	I_{CCO1}		50	100	mA

DC TEST CONDITIONS

Outputs Open
t Cycle = 250 ns
All Voltages Are Referenced to Ground

CAPACITANCE

(t_A =25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	100	pF	
Input/Output Capacitance	C_{OUT}	100	pF	

AC ELECTRICAL CHARACTERISTICS

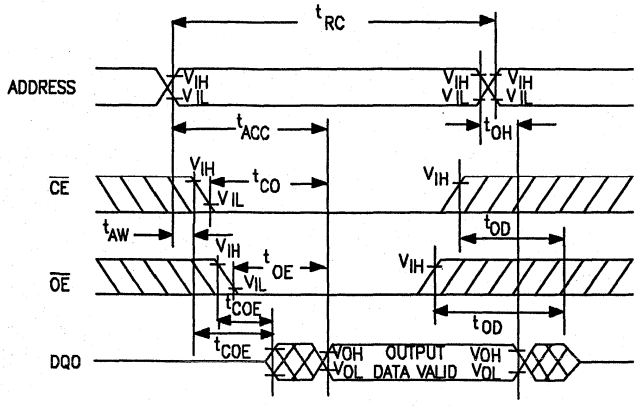
(0°C to 70°C, V_{CC} = 5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
Access Time	t_{ACC}			210	ns	
OE\ to Output Valid	t_{OE}			125	ns	
CE\ to Output Valid	t_{CO}			210	ns	
OE\ or CE\ to Output Active	t_{COE}	5			ns	5
Output High Z From Deselection	t_{OD}			125	ns	5
Output Hold From Address Change	t_{OH}	5			ns	
Read Recovery Time	t_{RR}	40			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR}	20			ns	
Output High Z From WE\	t_{ODW}			100	ns	5
Output Active From WE\	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	100			ns	4
Data Hold Time From WE\	t_{DH}	20			ns	4

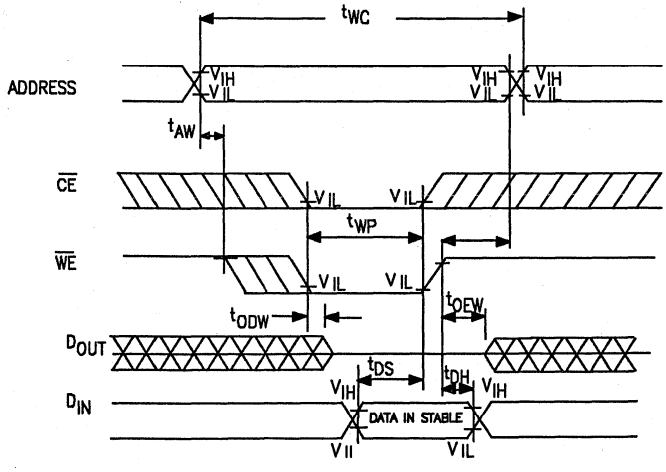
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
    Input: 1.5V
    Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

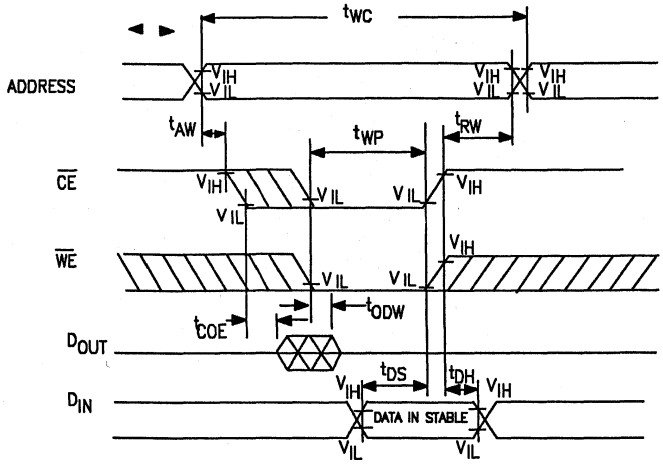
READ CYCLE (1)



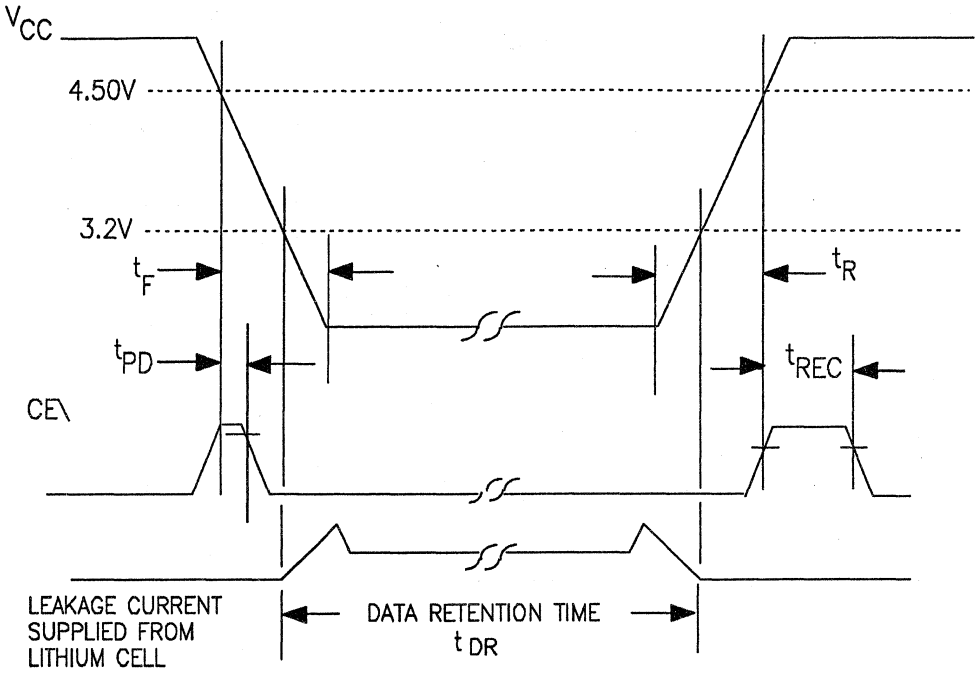
WRITE CYCLE 1 (2), (6), (7)



WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		*u* s	10
t_F	V_{CC} slew from 4.5V to 0V (CE\ at V_{IH})	100		*u* s	
t_R	V_{CC} slew from 0V to 4.5V (CE\ at V_{IH})	0		*u* s	
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	10

(t_A=25°C)

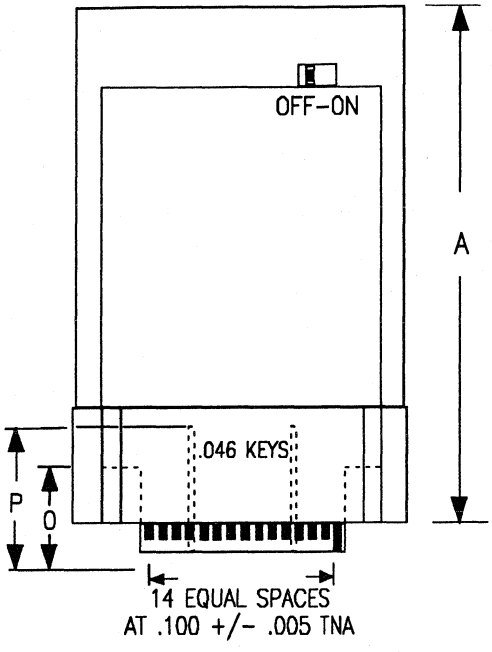
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	5		years	9

WARNING:
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

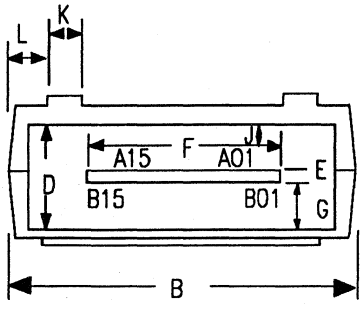
NOTES:

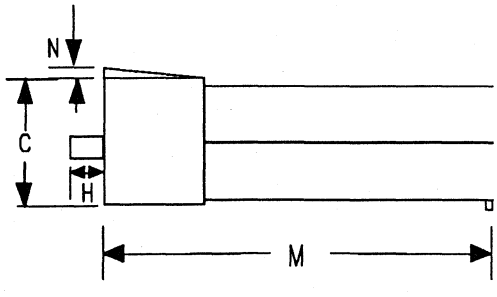
1. WE\ is high for a read cycle.
2. OE\ = V_{IH} or V_{IL}. if OE \ = V_{IH} during a write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE\ and WE\. t_{WP} Is measured from the latter of CE\ or WE\ going low to the earlier of CE\ of WE\ going high.
4. t_{DH}, t_{DS} are measured from the earlier of CE\ or WE\ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the CE\ low transition occurs simultaneously with or later than the WE\ low transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the CE\ high transition occurs prior to or simultaneously with the WE\ high transition in Write Cycle 1, the output buffers remain in a high impedance state in this period.
8. If WE\ is low or the WE\ low transition occurs prior to or simultaneously with the CE\ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS1217M is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. Removing and installing the cartridge with power applied may disturb data.

NONVOLATILE READ/WRITE CARTRIDGE
DS1217M



DIM.	INCHES	
	MIN	MAX.
A	3.020	3.040
B	2.280	2.300
C	.600	.630
D	.440	.460
E	.060	.065
F	1.590	1.607
G	.220	.250
H	.115	.135
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060
O	.039	.405
P	.405	.425



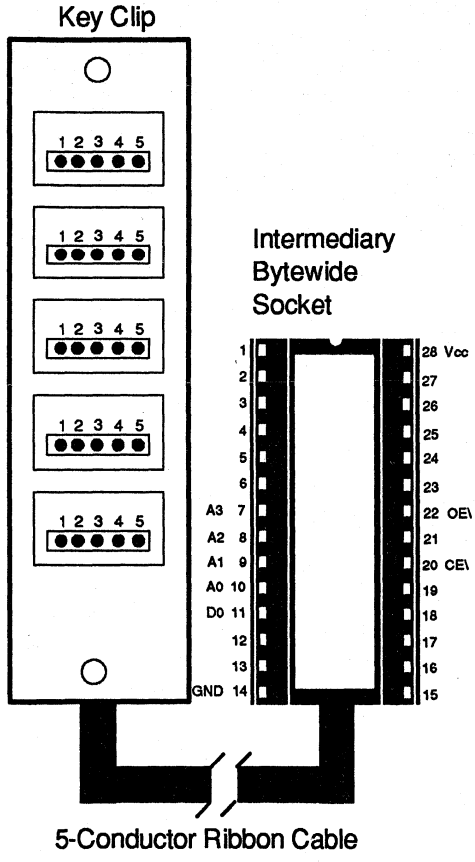


DALLAS SEMICONDUCTOR

DS1250
KeyRing

FEATURES

- Low-cost, add-on fixture for Electronic Keys and Tags
- No hardware changes needed to retrofit existing systems
- Layman installation
- Normal system operation unaffected
- Key or Tag communication totally controlled by software
- Typical 50 Kbps communication rate
- Up to five Keys and/or Tags resident at one time



PIN CONNECTIONS AND DEFINITIONS
(\ Denotes Condition Low)

Intermediary Bytewide Socket

Pin 7 - 10	Address Inputs
Pin 11	D0
Pin 20	Conditioned Chip Enable (CE\)
Pin 22	Output Enable (OE\)
Pin 14	Ground
Pin 28	V_{CC}

*All pins pass through except 20

Key Clip

Pin 1	V_{CC} +5 Volts
Pin 2	RST\ - RESET\
Pin 3	DQ - Data In/Out
Pin 4	CLK - Clock
Pin 5	GND - Ground

DESCRIPTION

The DS1250 KeyRing adapts low pin-count Electronic Keys (DS1204U), TimeKeys (DS1207) or Electronic Tags (DS1201) to JEDEC bytewide memory signals without affecting system operation. A simple, layman procedure is all that is needed to retrofit an existing system. Any 28-pin RAM, ROM, or EPROM can be removed, placed in the intermediary socket, and then reinstalled in the original location leaving the system intact. The emanating five-conductor ribbon cable can be routed out of the system enclosure if desired and the clip can be attached where convenient with the adhesive provided. Up to five Keys and/or Tags can be inserted in the clip at the same time. The intermediary socket contains a CMOS integrated circuit that redirects information flow from the bytewide memory to the inserted keys/tags. A special software-generated address sequence causes the redirection to take place. Typical data transfer rates of 50 Kbps are possible with an assembly language software driver.

HARDWARE IMPLEMENTATION: 28-PIN ROM SOCKET

Bytewide KeyRing application begins with a system board that contains a 28-pin socket with or without a ROM contained in the socket. In most system implementations and all PCs, there is at least one ROM that is used for boot sequences, basic I/O system implementation, EPROM storage, or some form of dedicated software monitor application.

To install the KeyRing, remove the existing 28-pin ROM and insert the bytewide KeyRing socket pins into the system board socket. After this is accomplished, reinsert the original ROM into the socket at the top of the KeyRing. Then route the five-conductor ribbon cable that connects the clip to the bytewide socket to the outside of the computer cabinet. Finally, attach the clip to a convenient place on the computer cabinet using the supplied adhesive.

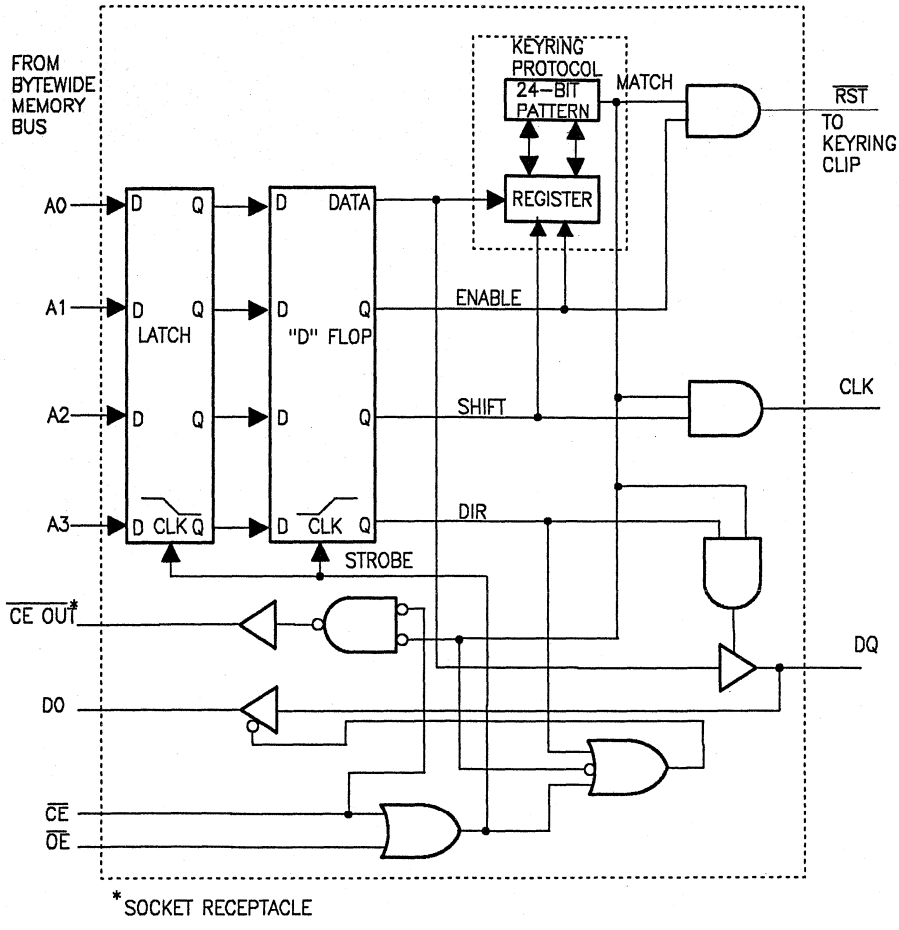
Under normal conditions, the system ROM will function as before, with address and data lines being transparently ported through the KeyRing socket and presented to the system ROM as in the original configuration. As a result, existing non-Key-protected software will run on the system unaffected. However, if certain address lines are probed with specific patterns under software control, the KeyRing is activated and the system ROM bus becomes electrically disconnected from the system board. Instead, the address and data bus become electrically tied to the KeyRing bus. At this point, communication to the system board ROM socket is passed on transparently to any device(s) that is inserted into the KeyRing clip.

KEYRING OPERATION

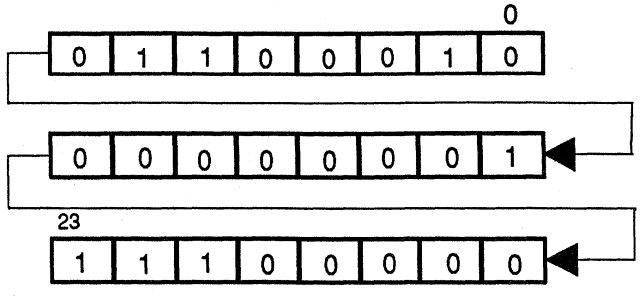
The main parts of the KeyRing are shown in the block diagram of Figure 1. Information presented on address inputs of the ROM are latched into the KeyRing on the falling edge of a strobe signal derived from the logical combination of CE\ In and OE\ In. The CE\ input is connected to the memory bus CE\ and the OE\ input is connected to the memory bus OE\ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 24-bit KeyRing protocol and to logic that will generate signals for Keys and Tags. The KeyRing protocol is derived from address inputs A0, A1, and A2. A1 is an enable signal that activates the communications sequence. A0 defines the data that is compared for recognition. A2 is used to clock in information defined by A0. Initially, the A1 input must be set high to enable communications. A1 must remain high during the pattern recognition sequence and subsequent communications with keys after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and access is denied.

Data transfer though the KeyRing occurs by matching a 24-bit pattern, as shown in Figure 2. This pattern is presented to a register on each

KEYRING BLOCK DIAGRAM Figure 1

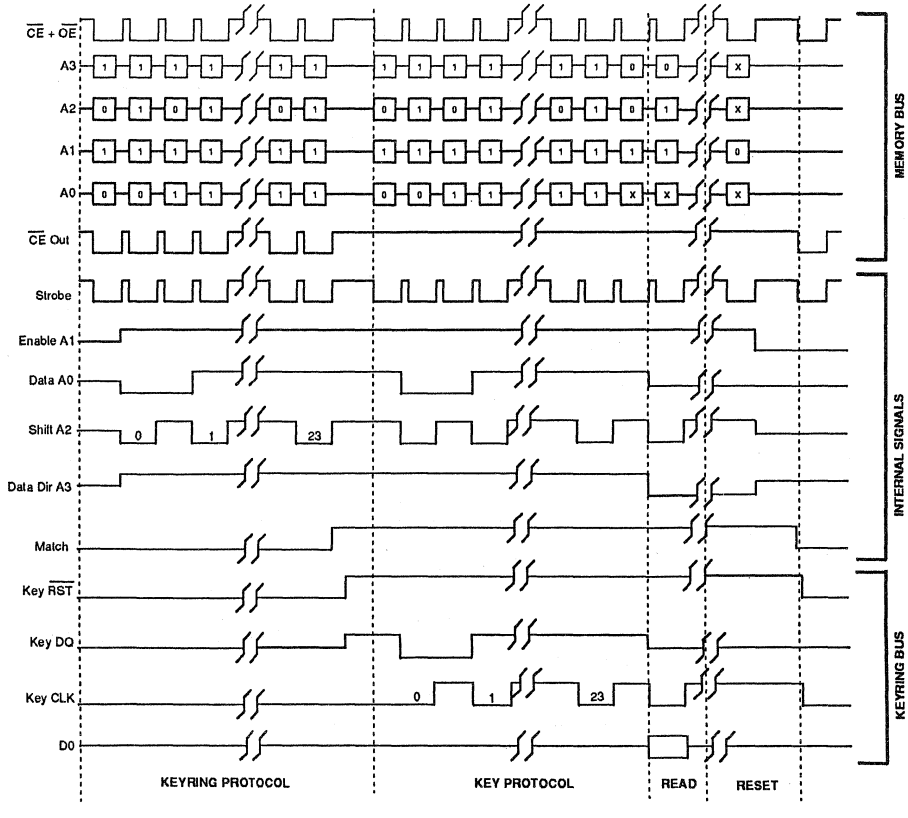


KEYRING SIGNALS Figure 2



rising edge of the strobe. Therefore, data is input for comparison to the KeyRing protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal that causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles. The first memory cycle sets A2 low, establishing the shift clock low. The second memory cycle sets A2 high, causing the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the same level for both memory cycles. Address input A3 is used to control the direction of data going to and from Keys. This input is not used during pattern recognition of the KeyRing protocol. After the 24-bit pattern has been correctly entered, a match signal is generated. The match signal is logically combined with the enable signal to generate the RST\ signal for Keys. The match signal is also used to disable Chip Enable to the topside memory and enable a gate that allows Key DQ to drive D0 line to the memory bus. When RST\ is driven high, devices attached to the KeyRing become active. Subsequent shift signals derived from A2 will now be recognized at the Key clock. The data signal for the Key is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on Key DQ. When A3 is set low, devices attached to the KeyRing can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the Key DQ.

KEYRING SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	uA	
Output Leakage	I_{LO}			1	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+4			mA	
RST\ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE (t_A=25°C)

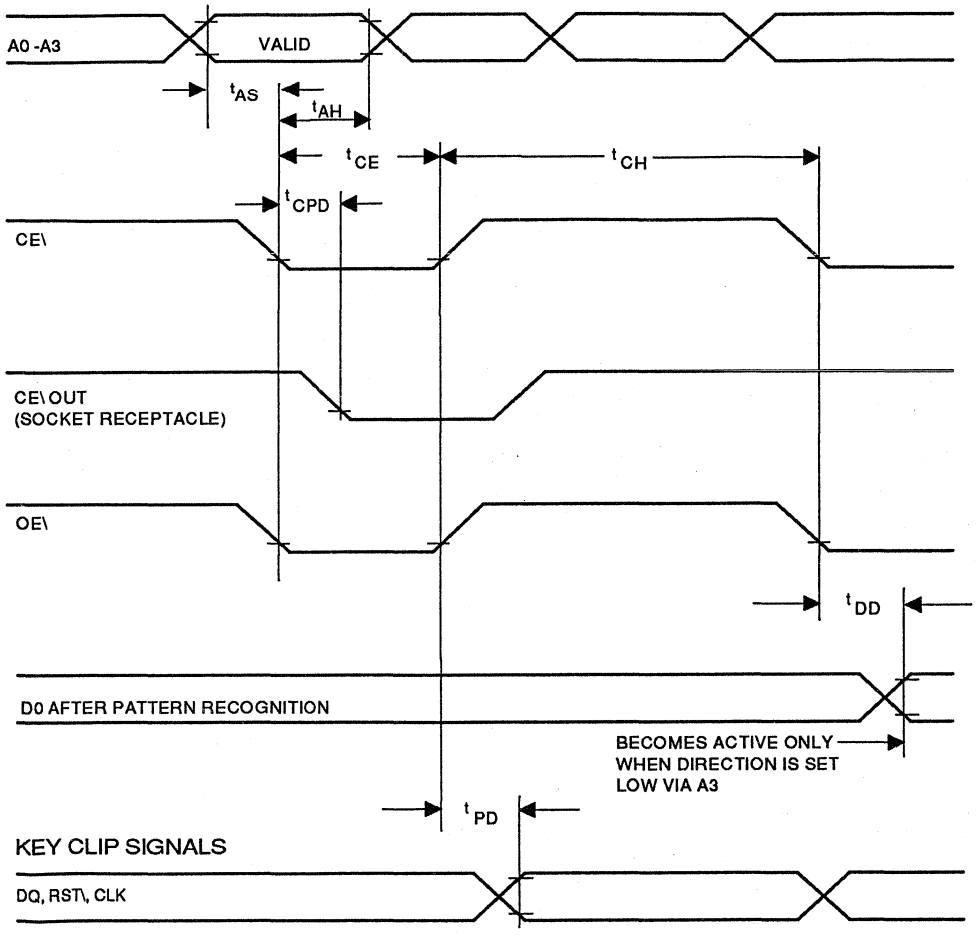
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V +/- 10%)

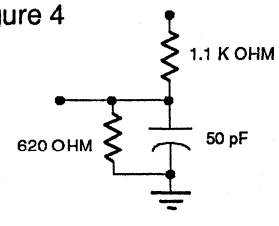
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
CE\ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
CE\ Inactive	t_{CH}	30			ns	
CE\ Propagation Delay	t_{CPD}			10	ns	

BYTEWIDE MEMORY BUS

BYTEWIDE MEMORY BUS



OUTPUT LOAD Figure 4



NOTES:

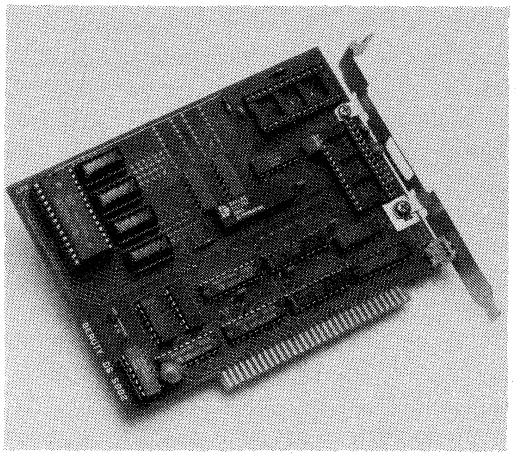
1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

DALLAS SEMICONDUCTOR

DS6010
PC Port

FEATURES

- Half-size expansion card that interfaces the PC, XT, AT, and compatible computers with Dallas Semiconductor memory cartridges and cartridge clips
- Software included supports the installation and controls operation
- Responds to all PC DOS commands
- Self-booting on power-up after installation
- Occupies only two 32K x 8 blocks of the PC memory map
- Provides the equivalent of a 4-megabyte solid-state disk drive when used with the DS9020 Cartridge Clip
- Contains a real time clock for time stamping and dating of file transactions
- Software-controlled DIP switch simplifies installation
- High-performance data transfer
- Low operating power
- Optional software protection and access control is available with the DS1204U Electronic Key



DESCRIPTION

The DS6010 PC Port is a half-size expansion slot card that interfaces DS1217 Nonvolatile Read/Write Cartridges and DS9020 Cartridge Clips to the IBM PC, XT, AT, or compatible computers. Included is a software package that is used to both install and operate the expansion port. After user interaction between the software and the operator, cartridges and Cartridge Clips will operate under DOS commands as a disk drive. Up to eight cartridges can be modularly added to a computer with each DS6010. This system addition allows compatible computers to be used in environments that are unsuitable for rotating mass memory. The PC Port occupies only two 32K x 8 blocks of memory space by using software-controlled bank switching techniques. The DS1216C SmartWatch, also included on the card, time stamps and dates file transactions.

OPERATION

The DS6010 PC Port uses several Dallas Semiconductor parts that perform the decoding and control functions of the PC Port. The following discussion assumes some understanding of each specific device. A more detailed explanation can be found in the individual data sheets.

The signals from the expansion bus that are used by the DS6010 arrive through the 62-position card edge connector as shown in Figure 1. These signals are used by the DS6010 to develop two 32K x 8 memory spaces from unused sections of the computer memory map. One of the memory spaces is mapped to cartridges and Cartridge Clips through two 28-pin bytewide memory sockets that have a pinout as shown in Figure 2. The two sockets are bused directly together. One socket (U10) is mounted horizontal to the IBM expansion slot seating plane and allows for convenient connection via ribbon cable to a cartridge or Cartridge Clip mounted within the computer cabinet. (See Figure 3.) The second socket (U11) is mounted vertically and is positioned near the mounting bracket of the DS6010. This socket provides convenient connection via ribbon cable to a cartridge or cartridge clip mounted externally to the computer cabinet. The second memory space developed by the DS6010 contains the DS1216C SmartWatch and 32K x 8 of nonvolatile static RAM.

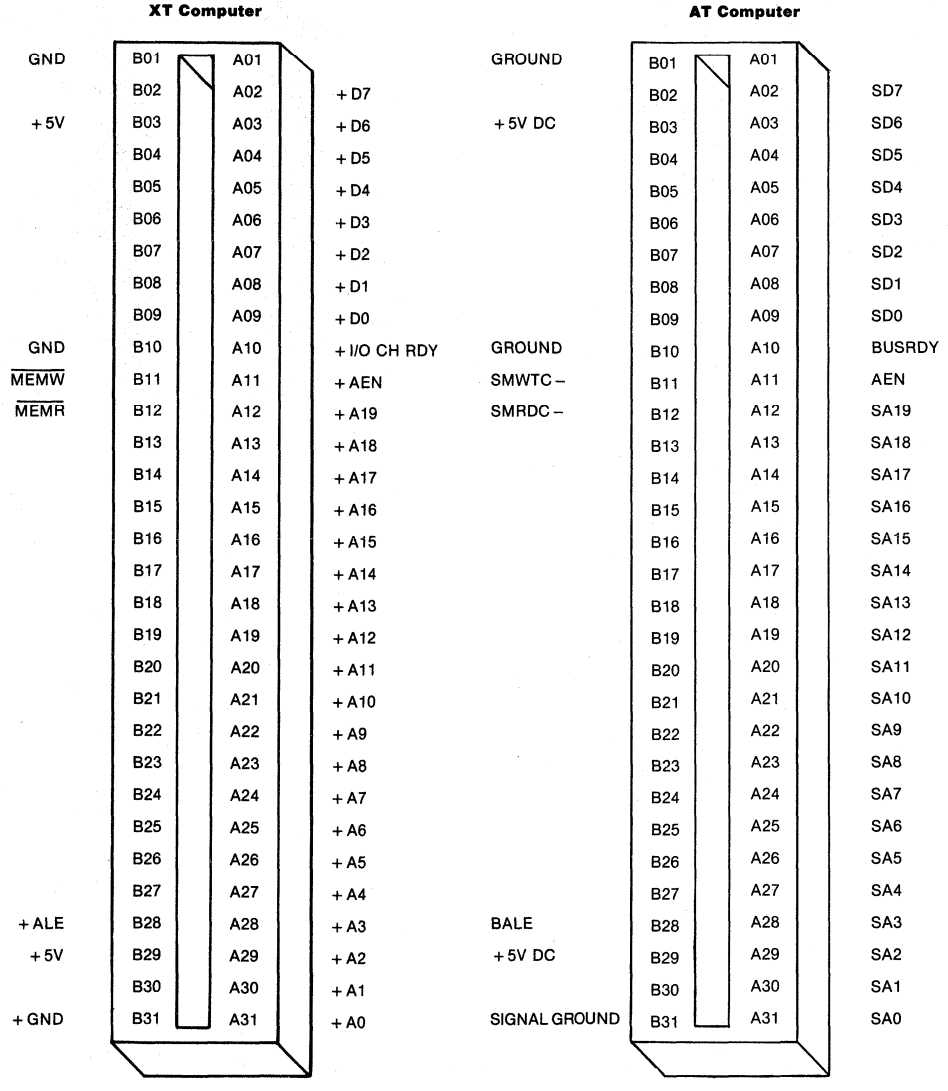
The decoding scheme of the DS6010 is both flexible and soft. The two 32K x 8 blocks of memory space can be located anywhere within the one megabyte memory map of the system. Normally the lower 640K bytes are reserved for DRAM so the decoder would be set for some area in upper memory space. The decoder scheme is soft because the software supplied with the DS6010 can set the decoder boundaries using software commands. These commands are directed to the DS1292 Eliminator, which is an electronic replacement for mechanical DIP switches. The Eliminator is nonvolatile; once the switches are set, they will remain in the programmed state indefinitely. The interface between the system bus and the Eliminator is developed by the DS1206 Phantom Serial Interface Chip. The DS1206 has the ability to decipher memory cycles that do not impact other system operations into the signals that set the DS1292 to the proper address boundaries. Once the Eliminator is properly set, the logic locks out future changes to the decoder settings.

ELECTRICAL OPERATION

The address bus A0 through A14 arrives at the inputs of two 74HC244 line receivers through the 62-position card edge connector (see Figure 4). Since both of the gate signals are grounded, the 74HC244 acts only as a buffer. All 15 address lines are bussed directly through to the bytewide memory socket sights. A third 74HC244 is used to buffer control signals MEMR\ (Memory Read), MEMW\ (Memory Write), and IORDY (I/O Ready). MEMR\ and MEMW\ are both logically ORed with signals developed by the decoder logic that will be discussed later in this text. This logic produces the OE\ (Output Enable) and WE\ (Write Enable) signals for the bytewide memory socket sites.

The IORDY line is an output signal from the PC Port card to the computer expansion bus. When this signal is active, the current bus cycle is extended. The DS6010 drives this line low when either a memory read or a write cycle is being executed to one of the 32K x 8 memory blocks. A set of four NAND gates (1-74HC00) and the DS1000 5-Tap Silicon Delay Line Chip generate a cycle stretch signal that controls the length of time that the IBM PC Port will hold the IORDY signal active. As shipped by Dallas Semiconductor, this length of time is set at 500ns. However, this length of time can be shortened or lengthened by changing the value of the DS1000. The length of time allotted must be long enough to allow for the propagation delay of

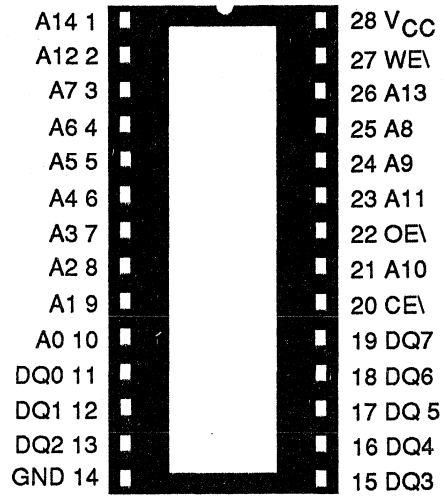
IBM EXPANSION BUS 62-PIN CONNECTION Figure 1



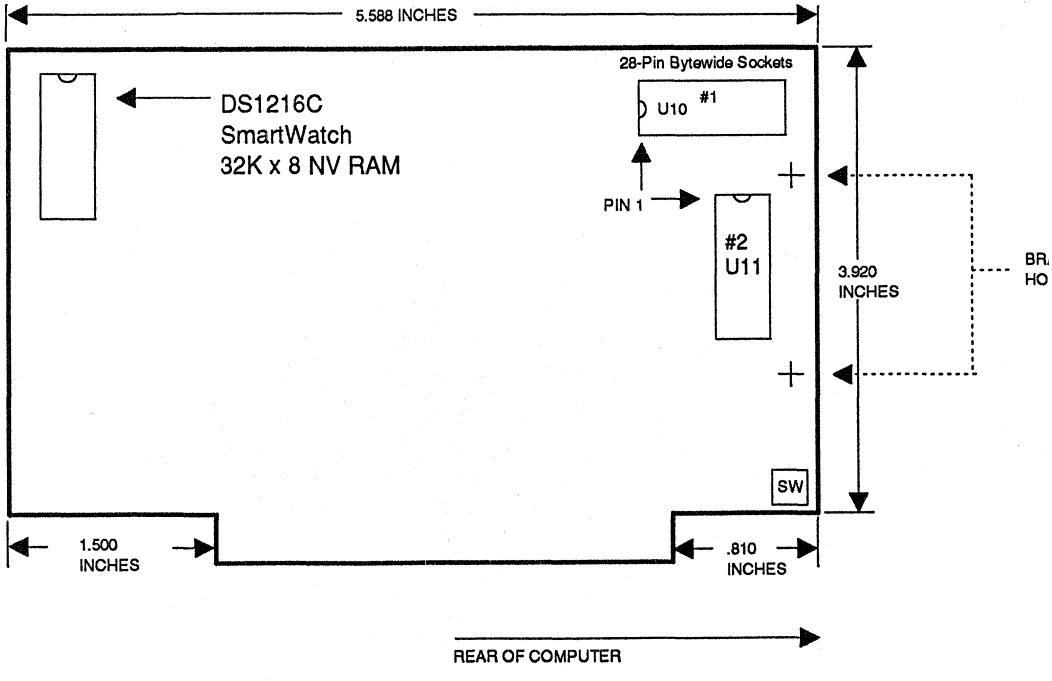
28-PIN BYTEWIDE SOCKET PINOUT Figure 2

PIN NAMES (\ Denotes Condition Low)

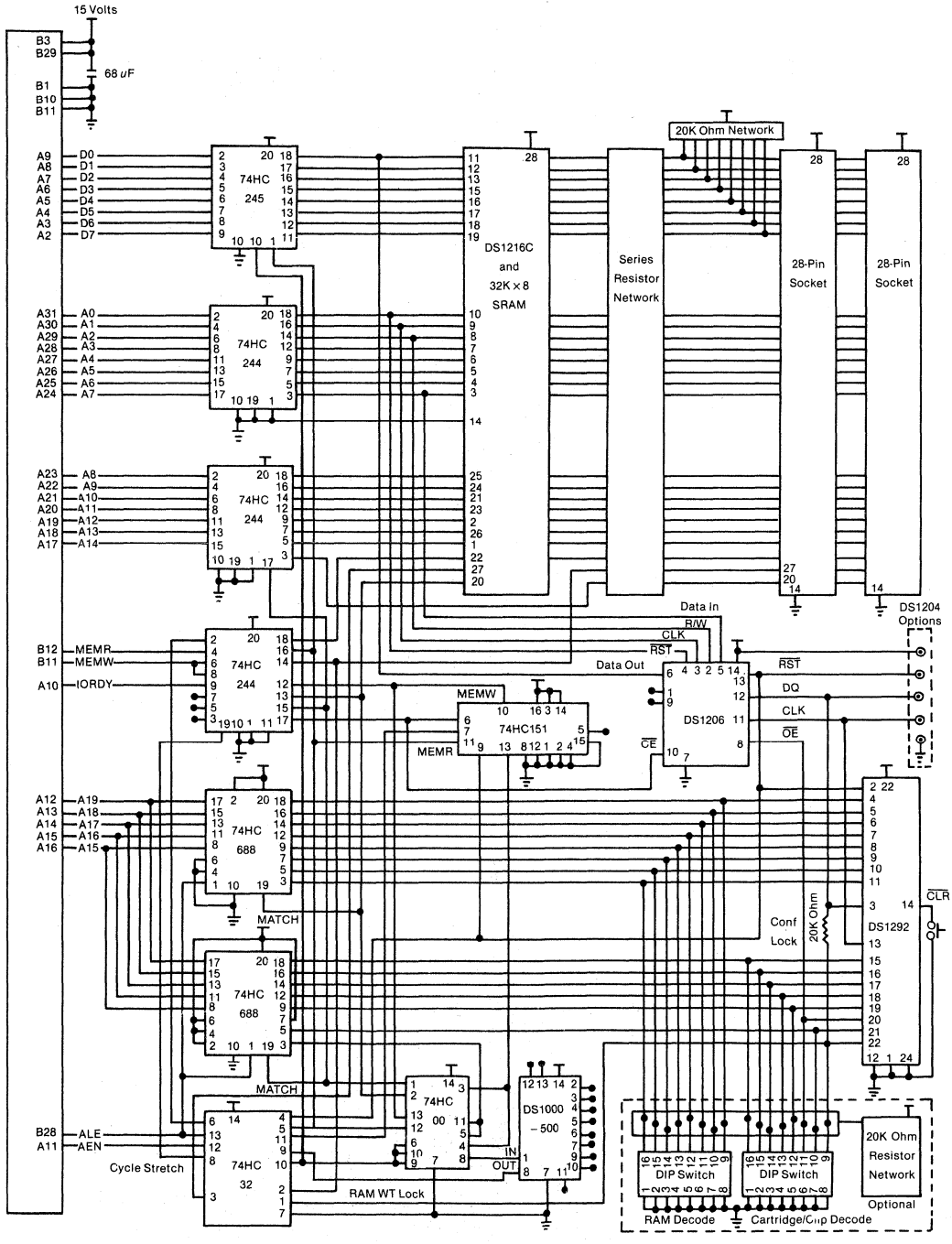
A0-A14	Address Inputs
CE\	Chip Enables
GND	Ground
DQ0-DQ7	Data In/Data Out
V_{CC}	Power (+5V)
WE\	Write Enable
OE\	Output Enable



28-PIN BYTEWIDE SOCKET LOCATIONS Figure 3

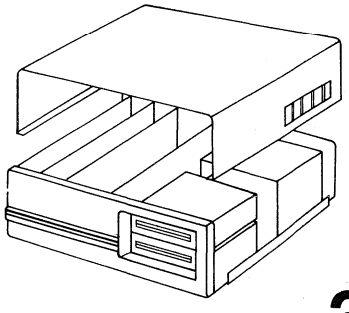


DS6010 PC PORT ELECTRICAL SCHEMATIC Figure 4

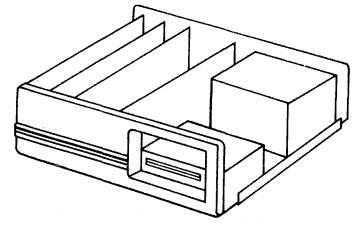


INSTALLATION Figure 5

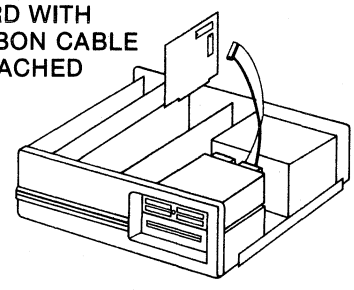
1. REMOVE COVER



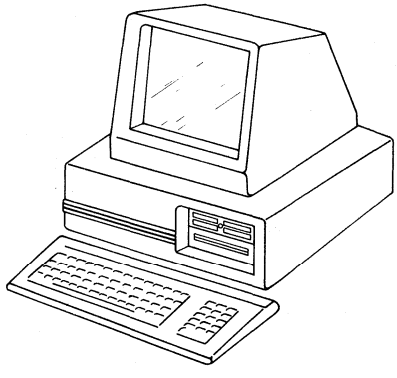
2. REMOVE FLOPPY DISK DRIVE



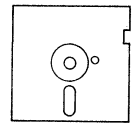
3. INSTALL THE CARTRIDGE CLIP, INSERT THE PC PORT I/O CARD WITH RIBBON CABLE ATTACHED



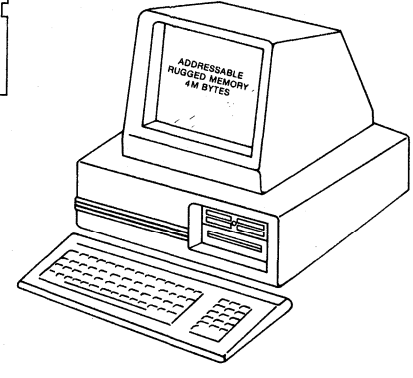
4. REASSEMBLE COMPUTER



5. INSTALL SOFTWARE



6. FUNCTIONAL SOLID-STATE COMPUTER



the buffers and the access time of the cartridges or Cartridge Clip that is installed into the 32K x 8 socket sites.

The data bus D0 through D7 arrives at a 74HC245 octal transceiver through the 62-position card edge connector. The 74HC245 has both a gate and a direction control. The direction control is set via the MEMR\ signal which is buffered by a 74HC244 line receiver. The direction control will, therefore, set the 74HC245 to drive the system bus whenever the MEMR\ signal is in the active state and when the gate signal is also active. The gate on the 74HC245 is controlled by the logical combinations of MEMR\ and MEMW\ and the match output pin of two 74HC688 8-bit identity comparators. The logic combination of these four signals is accomplished using three two-input NAND gates. The output pins of the 74HC688 also become the CE\ (Chip Enable) inputs for the two 32K x 8 memory blocks. The CE\ signal for the 28-pin sockets for cartridge and Cartridge Clip connection is buffered through a 74HC244. The gates to the 74HC688 are enabled by the ALE (Address Latch Enable) signal from the computer expansion bus that is active when system bus addresses are valid.

Address lines A15 through A19 are connected to the P input sides of the 8-bit binary comparator. The Q input sides are connected for the most part to the Eliminator. The comparison of the P and Q sides will, therefore, produce a match output and select one of the 32K x 8 memory boundaries when the Eliminator settings compare to the levels on address lines A15 through A19. The 74HC688, which is used to decode the 32K x 8 block of NV SRAM, is driven by eight Eliminator outputs to the Q inputs. Since only five address lines are used on the P side, three inputs are tied to fixed levels. The Pin 2 input is connected to V_{CC}; pins 4 and 6 are grounded. The 74HC688, which is used to decode the 32K x 8 block of memory for cartridges or Cartridge Clips, is driven directly by only 6 Eliminator outputs to the Q inputs. One of the remaining Q inputs is connected to a read or write signal, which allows the identity comparator to only output a chip enable signal when a valid read or write cycle is occurring. The other Q input is unused and connected to a fixed high level. Again, only five address lines are connected to the P side. The remaining P inputs are tied to a fixed high level.

As mentioned earlier, only six Eliminator outputs were used by the 74HC688, which is used to decode the memory block for cartridges or Cartridge Clips. The other two outputs have special functions. The output on pin 22 of the Eliminator is used to lock out the write enable signal which goes to the NV RAM site. This allows a convenient way for software to write-protect the nonvolatile RAM. The other output on pin 20 of the Eliminator is used to lock out the DS1206 Phantom Serial Interface Chip by disabling the OE\ (Output Enable) signal after the Eliminator is set for proper system configuration.

Communications to the Eliminator that allow the system configuration to take place are handled by the DS1206, which is controlled by the 74HC151 data selector and software. Bus cycles that set proper address patterns on address lines A0, A1, A2 and A7 are clocked into the DS1206 using consecutive CE\ cycles. The CE\ for the DS1206 is generated under two different sets of conditions by the 74HC151 based on the state of MEMR\ and MEMW\. Initially, the DS1206 must receive 24 bits of data that must match exactly with the code embedded into the DS1206. (Consult the DS1206 data sheet for exact details on the DS1206 operation.) Prior to this condition, the DS1206 is a passive listener on the bus and will not output any signals to the Eliminator. During this time the CE\ input to the DS1206 from the 74HC151 will be active only when MEMW\ is active (see Table 1). Since write cycles can be accom-

plished to known memory addresses where ROM resides, no memory alterations occur and these cycles can be transparent to the rest of the system. However, as soon as the 24-bit pattern match is completed, the DS1206 will pass signals to the DS1292 from the address bus. Address line A0 will be passed through as the RST\ (Reset) signal; address line A1 becomes the CLK (clock); A2 defines whether data is to be read or written; and address A7 becomes the data input to the Eliminator. (Consult the DS1292 data sheet for exact details on Eliminator.)

The first requirement for entering data into the Eliminator is to set the RST\ input to a high level. This signal is also sent as an input to the 74HC151 data selector. This new input allows CE\ for the DS1206 to be active when MEMW\ is active and also when MEMR\ is active and either of the two 74HC688's is outputting a match signal, indicating that one of the two 32K x 8 blocks of memory is being accessed. This new set of circumstances allows the Eliminator status to be read back via the system bus DQ0 line. Bus contention is avoided from either of the two 32K x 8 memory blocks because the OE\ signal to the memory blocks is inhibited as long as the RST\ to the DS1292 is at a high level.

Data is passed back through the DS1206 by the feedback resistor that couples the Eliminator output back to the input. Once the Eliminator is set and verified, system configuration can be terminated and locked by making sure the bit that is output on pin 20 of the Eliminator is set to logic one when the RST\ signal is driven low. The Eliminator can always be put back in an unconfigured state by depressing the CLR\ (Clear) button, which forces all of the Eliminator outputs low.

DS1206 ENABLE Table 1

RST\	MEMW\	MEMR\	MATCH\	ENABLE\
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

RST\	MEMW\	MEMR\	MATCH\	ENABLE\
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

DS6010 PC PORT SPECIFICATION (\ Denotes Condition Low)

Organization:	Two 32K x 8 Memory Blocks
Input Connection:	IBM PC/XT/AT Expansion Bus
Output Connection:	JEDEC 28-Pin Bytewide Sockets
Access Time:	1 μS per Byte Maximum*
Temperature Range:	0°C to 70°C
Size:	$^1/_2$ Length I/O Card 5.5 Inches Long x 3.2 Inches High
Real Time Clock Accuracy:	± 1 Minute/Month @ 25°C
Software:	PC DOS-Compatible
Power Consumption:	500 MW Maximum
Address Map Range:	1 Megabyte

*Performance can be enhanced by lowering the value of the cycle stretch delay line.

ELECTRICAL OPTIONS

The DS6010 has provisions for mechanical DIP switches and pull-up resistors that can be used in place of the Eliminator. While the DS6010 is not shipped with these components, they can be added if needed for a specific application (see Figure 4). If DIP switches and pull-up resistors are used, the Eliminator should be removed from its socket. The DS6010 can also be optioned with the Dallas Semiconductor DS1204U Electronic Key for software protection and access control. Under special contract with Dallas Semiconductor, these options can be supplied to customer specifications. Contact Dallas Semiconductor for ordering information.

INSTALLATION

Prior to installing the DS6010, test the computer to ensure it is operating properly. Disconnect any peripheral equipment and unplug AC power. Remove the computer cabinet and install the DS6010 in any available I/O slot except PC/XT slot B. It is a good idea to connect the ribbon cable that will connect either the cartridge or the Cartridge Clip to the appropriate 28-pin socket. If the cartridge or Cartridge Clip is mounted within the computer cabinet, the horizontal 28-pin socket on the top of the PC board is the proper choice (see Figure 3). When mounting the cartridge or Cartridge Clip external to the computer, use the vertical 28-pin socket. The data sheet on the DS9020 Cartridge Clip provides mounting dimensions.

The Cartridge Clip will fit in the place of any half-high disk drive. If a DS1217 Nonvolatile Read/Write Cartridge is being used, consult the data sheet for mechanical dimensions. Mechanical hardware for mounting the DS1217 is not supplied by Dallas Semiconductor. However, the DS9000 Bytewide Cable Harness ribbon cable is available to provide electrical connection between the cartridge and the DS6010. Pin 1 on the ribbon cable must match Pin 1 on the 28-pin socket. Figure 3 identifies the Pin 1 locations on the 28-pin sockets. Pin 1 is on the opposite end of a color stripe on the ribbon cable. (See the DS9020 data sheet.) When using the DS9000 ribbon cable with a cartridge, Pin 1 is on the same end as the color stripe. ***NOTE:*** *Improper connection of the ribbon cable can damage the Cartridge Clip, cartridge, and PC Port.*

After the installation is complete, replace the computer cabinet and reconnect the peripheral devices. When power is applied to the computer, it should function the same as before the DS6010 was installed. Install the supplied software to make the PC Port operational.

SOFTWARE INSTALLATION

The floppy disk provided with the PC Port contains both the software and instructions for installation. Insert the floppy disk marked "DS6010 Software" into the default disk drive and type "TYPE DS6010.MEM". The print command can be used to make a hard copy. Read the manual carefully while installing the software. After installation is complete, the system will respond to all DOS commands, and the IBM PC Port, cartridge, and Cartridge Clip will appear to behave as added disk storage.

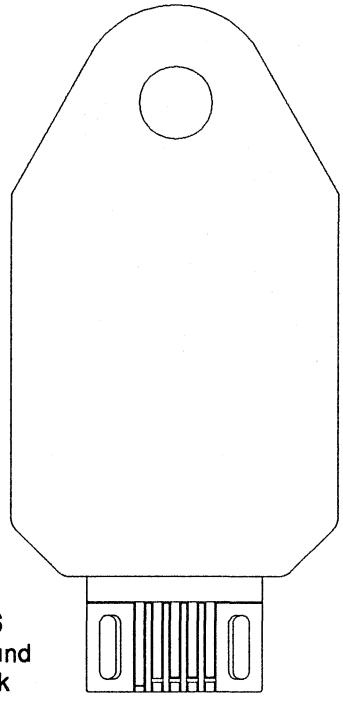
DALLAS SEMICONDUCTOR

DS620x CyberKey

FEATURES

- Greater than 50,000 cycle connector life
- Durable and rugged
- Ground pin makes first and breaks last
- 3-wire serial interface (DQ, CLK, and RST\) simplifies microprocessor interconnect
- Guided entry on mating connector overcomes orientation problems
- Greater than10 years of data retention with no limitations or restrictions on write cycles
- Low-power CMOS circuitry
- Applications include software authorization, computer identification, system access control, calibration, data storage, automatic system setup, and travelling work record

PACKAGE/PIN DESCRIPTION



PIN NAMES

1	Ground
2	Clock
3	Data
4	RST\
5	V_{CC}

DESCRIPTION

CyberKeys are minature electronic memories with self-contained lithium energy sources. Depending upon the memory device internal to the CyberKey, secure, non-secure, time-related, and combinations of these functions are available. Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLK (clock), RST\ (reset), and DQ (data). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user. CyberKeys are designed to be rugged and durable enough to withstand normal handling with a life expectancy of over ten years. Small, lightweight construction makes the devices suitable for carrying in a pocket or direct attachment to an object. Figure 1 lists the memory devices utilized in the different CyberKeys. For further information please see the referenced data sheet.

CYBER KEY DEVICES Figure 1

CYBERKEY	DESCRIPTION	RELATED DATA SHEET
DS6200	64-bit unique serial number with CRC Checking	DS2400
DS6201	1024 bits non-secure static RAM	DS1200
DS6204	128-bit secure static RAM: 64-bit password and 64-bit ID	DS1204
DS6205	3 secure 384-bit sub-keys, 512-bit scratch-pad	DS1205
DS6207	384-bit secure static RAM: Internal Time Key (1 to 512 days)	DS1207

DALLAS SEMICONDUCTOR

DS630x
CyberCard

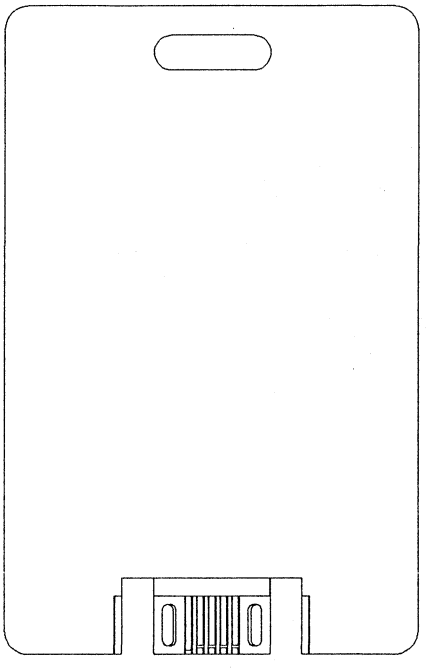
FEATURES

- Greater than 50,000 cycle connector life
- Durable and rugged
- Ground pin makes first and breaks last
- 3-wire serial interface (DQ, CLK, and RST\) simplifies microprocessor interconnect
- Guided entry on mating connector overcomes orientation problems
- Greater than10 years of data retention with no limitations or restrictions on write cycles
- Low-power CMOS circuitry
- Applications include software authorization, computer identification, system access control, calibration, data storage, automatic system setup, and travelling work record

DESCRIPTION

CyberCards are credit card-shaped electronic memories with self-contained lithium energy sources. Depending upon the memory device internal to the CyberCard, secure, non-secure, time-related, and combinations of these functions are available. Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfers with only three signals: CLK (clock), RST\ (reset), and DQ (data). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered when a conventional integrated circuit package is inserted by the end user. Cyber-

PACKAGE DESCRIPTION



PIN NAMES

1	Ground
2	Clock
3	Data
4	RST\
5	V_{CC}

Cards are designed to be rugged and durable enough to withstand normal handling with a life expectancy of over ten years. Small, lightweight construction makes the devices suitable for carrying in a pocket or direct attachment to an object. Figure 1 lists the memory devices utilized in the different CyberCards. For further information please see the referenced data sheet.

CYBERCARD DEVICES Figure 1

CYBERCARD	DESCRIPTION	RELATED DATA SHEET
DS6301	1024 bits non-secure static RAM	DS1200
DS6304	128-bit secure static RAM: 64-bit password and 64-bit ID	DS1204
DS6305	3 secure 384-bit sub-keys, 512-bit scratch-pad	DS1205
DS6307	384-bit secure static RAM: Internal Time Key (1 to 512 days)	DS1207

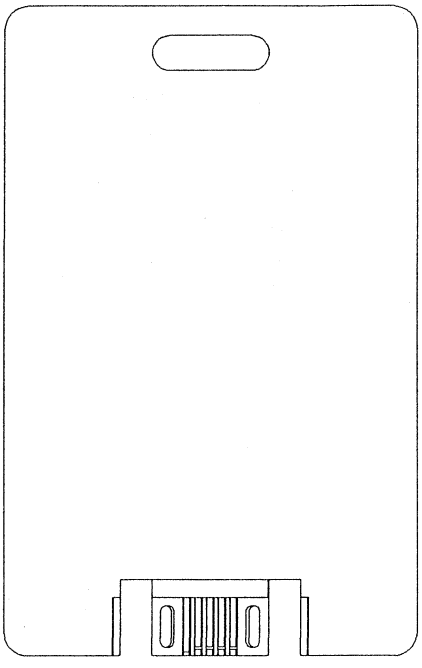
DALLAS SEMICONDUCTOR

DS6417
CyberCard EV 4M-Bit NV SRAM

FEATURES

- Greater than 50,000 insertion connector life
- Durable and rugged
- Ground pin makes first and breaks last
- User-insertable memory
- Capacities from 256K bits to 4M bits of nonvolatile memory
- Up to 1 million bits per second transfer rate
- Automatic write protection circuitry safeguards against data loss
- Cyclic redundancy check monitors serial data transmission for errors
- Compact size and shape
- Wide operating temperature range of 0°C - 70°C

PIN DESCRIPTION



PIN NAMES

Pin 1	Ground
Pin 2	Clock
Pin 3	Data
Pin 4	RST\
Pin 5	V_{CC}

DESCRIPTION

The DS6417 CyberCard EV is a nonvolatile serial access RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 256K bits to 4M bits. Data is transferred to and from the RAM through a standard 3-wire interface which is comprised of a data, RST\, and clock pin. The serial port requires a 6-byte protocol to set up memory transfers. A cyclic redundancy check circuitry is included to monitor the serial data transmissions for errors.

PIN DESCRIPTION OVERVIEW

RST\ - this pin controls all communications to the DS6417. When this signal is LOW, all communications to the serial port are inhibited. When high, data can be clocked into or out of the serial port.

CLK - this input signal is used to input or extract data from the serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven onto the 3-wire bus after a falling edge during a read cycle and latched into the port on the rising edge during a write cycle.

DQ - this signal is the biderectional data signal for the 3-wire port.

OPERATION

The block diagram of Figure 1 illustates the main elements of the DS6417. As shown, the DS6417 has two major section; the static RAM array and the 3-wire to bytewide converter. The 3-wire to bytewide converter controls the static RAM through the use of the control/address/data latches and multiplexor.

The 3-wire to bytewide converter uses a 56-bit protocol to determine the action to be done and the starting address in RAM to be used. Data is entered while RST\ is high on the low to high transition of the CLK signal provided the data is stable on the DQ line for the proper setup and hold times.

The last 8 bits of the 56-bit protocol contains the cyclic redundancy check byte that ensures that all bits of the protocol have been transmitted correctly. If the 56-bits of protcol have not been received properly, the transaction will be aborted. The CRC check byte can catch up to three bit errors within the 56-bit protocol and can also be used on incoming and outgoing data streams to check the integrity of the data being read or written.

PROTOCOL

The 3-wire bus protocol can cause eight different actions to be taken by the DS1517 (see Table 1).

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action to be taken involves a read or a write. A read function is defined by the binary pattern [11101000]. This pattern is applicable to commands 1,3,5, and 6 of Table 1. A write function is defined by the binary pattern [00010111]. This pattern is applicable to commands 2,4,7, and 8 of Table 1. Any other pattern which is entered into this read/write field will cause the transaction to be terminated. Additional differentation as to which read or write command is determined by the last five bits of the third byte of the third byte field of protocol referred to as the command field. The control field bits are shown as the binary values in Table 1 above.

A burst read uses a 19 bit address field which consists of the second, third, and the first three bits of the fourth byte of the protocol to determine the starting address of the information to be read from the RAM. The byte of data that has been accessed is transferred to the 3-wire bus a bit at a time. LSB first, by driving the DQ line on the falling edge of the next eight clocks.

A burst write uses the same 19 bit address field to determine the starting address of information to be written in RAM. Data is shifted from the DQ line into an eight bit shift register on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immeaditely after the rising edge of the eighth clock. Burst reads and writes will continue on a byte by byte basis automatically incrementing the selected address by one location for each succisive byte.

Termination of a current transaction will occur at

PROTOCOL COMMANDS Table 1

1) [00110 binary] burst read
2) [10001 binary] burst write
3) [00101 binary] read protocol select bits
4) [01110 binary] write protocol select bits
5) [11XXX binary] burst read masking portions of the protocol select bits
6) [00011 binary] read the CRC register
7) [10110 binary] set arbitration byte address (NA)
8) [01001 binary] read arbitration byte (NA)

any time the RST\ signal is taken low. If a byte of data has been loaded into the shift register a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when the RST\ signal goes low, no writing occurs. Reads can be terminated at any point since there is no potential for the corruption of RAM data.

The read CRC command provides a method for checking the intgrety of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the 56-bit protocol. The eight bit CRC value is valid for both the 56-bit protocol and also all data that is read or written from the RAM. After a burst read or write has finished and RST\ has gone low, the final value of the CRC is stored in an internal register of the DS6417. If a read CRC register command is issued, the stored CRC value is driven onto the DQ signal line by the first eight clock cycles after the 56-bit protocol is received. The CRC value generated by the DS6417 should match the value generated by the host system which is transmitting or receiving data on the other end of the 3-wire bus.

It should be noted that the CRC for a previous transaction can only be obtained if a read CRC command is issued immeaditely after the RST\ signal goes low to reset the DS6417, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever the RST\ signal goes low again.

Three commands are used to set the select bits in the protocol. Once the select bits ae set to a binary value they must be matched when protocol is sent or further activity is prevented. The bits allow for up to 65,536 different binary combinations. Therefore, multiple DS6417s can be connected on the same 3-wire bus and only the selected device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field. To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have a large number of DS6417s in use and uniquely identify each one. A read can occur successufully without knowing the select bits but a write cannot occur without matching the current select field.

A third command masking specific select bits provides a means for determining the identity of a specific DS6417 in the presence of many DS6417s. A read in the read/write field and a [11000 binary] in the command field will execute a mask read that ignores all select bits to determine the presence of any DS6417s. With the detection of at least one device, a search can

begin by masking all but a single pair of DS6417 select bits. A read in the read/write field and a [11001 binary] in the command field will unmask the first two LSB's of byte 4 of the select bits (Figure 3). With these two select bits unmasked, only an exact match of four possible combinations (00, 01, 10, or 11) of these two select bits will now allow access through the 3-wire port to RAM. Therefore, repeating the unmasking of the two bits of the select field up to four times will give the binary value of these select bits. Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of the four combinations can proceed as before. In fact, repetition of unmasking select bit pairs will yield an exact match of the one DS1517 out of the possible 65,536 in no more than 32 attempts.

CRC GENERATION

The logic involved in the CRC generation is shown in Figure 4. Bascilly, the scheme is comprised of an eight bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC generator while each byte is being assembled and at the same time, output data to the output (DQOUT). When input select CRC (SDCRC) is driven to an active level (high) data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as descrived earlier for operation of the 3-wire bus.

The reset signal (RSB) must be high while the CRC generator is being used as an inactive state will disable the eight bit shift register. This signal is the same as the reset described for the 3-wire bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS6417 CRC requirements.

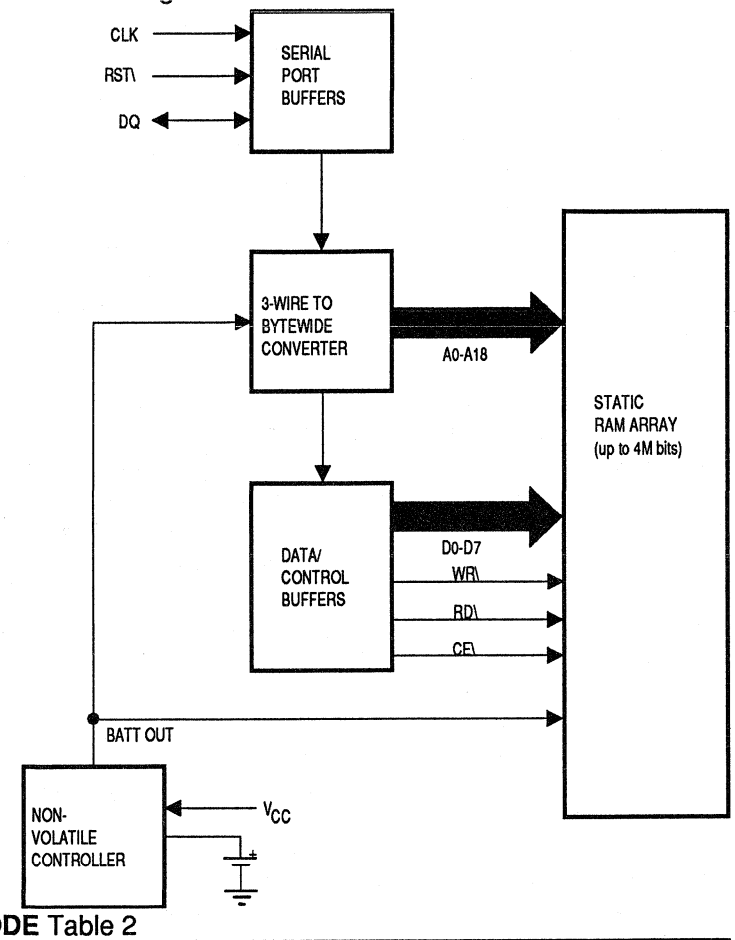
However, another approach is to generated the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Microcontroller. The assembly language procedure DO_CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

3-WIRE BUS

The 3-Wire bus is comprised of three signals. These are the RST\ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the RST\ input high. The RST\ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if the RST\ is low and the DQ pin goes to a high impedance state. When data transfers to the DS6417 are terminated by the RST\ signal going low, the transition of the RST\ going low must occur during a high level of the CLK signal. Failure to insure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfer are illustrated in Figures 5 and 6 for normal modes of operation.

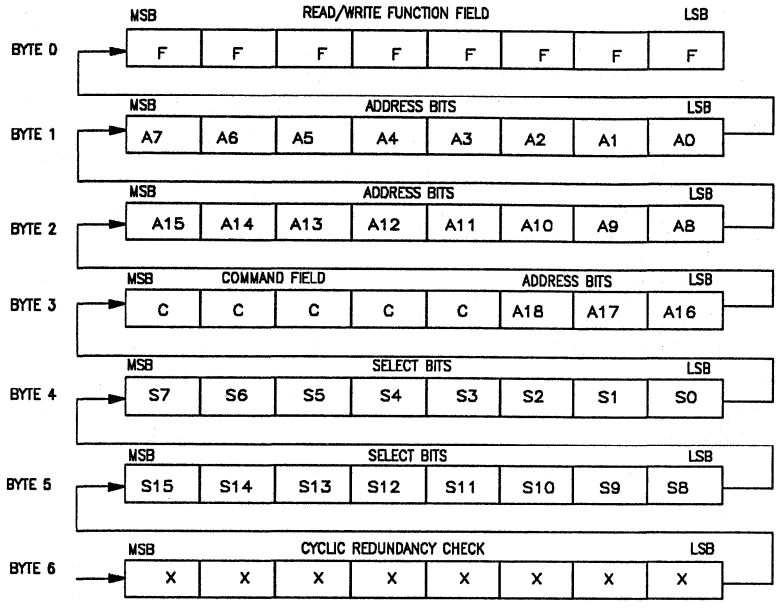
BLOCK DIAGRAM Figure 1



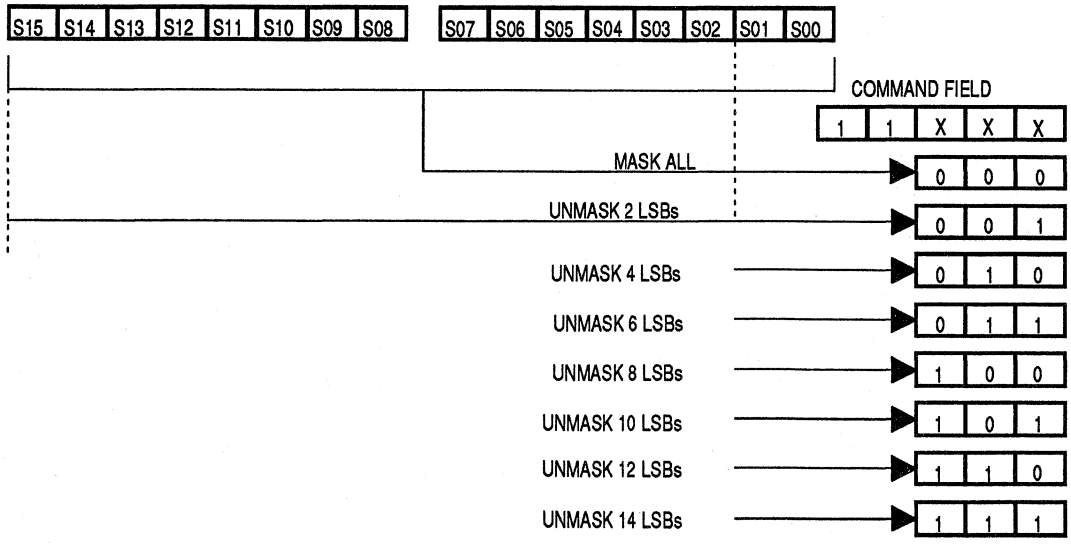
CRC CODE Table 2

```
DO_CRC:
        PUSH    ACC             ; Save the Accumulator
        PUSH    B               ; Save the B register
        PUSH    ACC             ; Save bits to be shifted
        MOV     B,      #8      ; Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC     ; Calculate DQIN xor CRCTO
        RRC     A               ; Move it to the last
        MOV     A,      CRC     ; Get the last CRC value
        JNC     ZERO            ; Skip if DQIN xor CRCTO = 0
        XRL     A,      0CCH    ; Update the CRC value
ZERO:
        RRC     A               ; Position the new CRC
        MOV     CRC,    A       : Store the new CRC
        POP     ACC             : Get the remaining bits
        RR      A               ; Position next bit in LSB
        PUSH    ACC             ; Save the remaining bits
        DJNZ    B,      CRC_LOOP ; Repeat for eight bits
        POP     ACC             ; Clean up the stack
        POP     B               ; Restore the B register
        POP     ACC             ; Restore the Accumulator
        RET                     ; Return
```

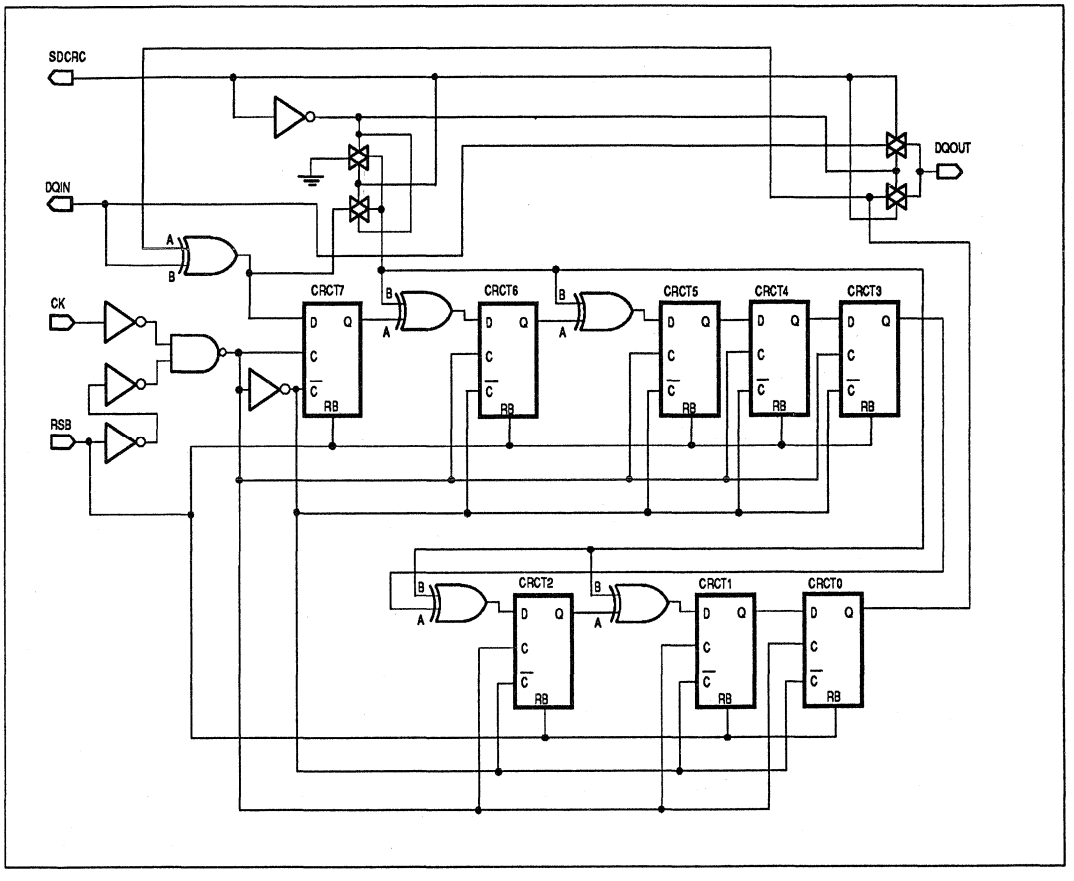
PROTOCOL Figure 2



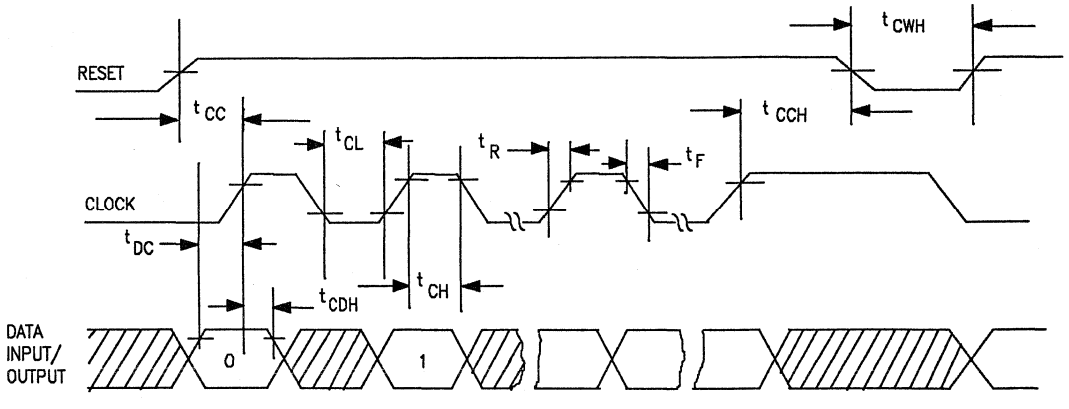
SELECT BITS MASK Figure 3



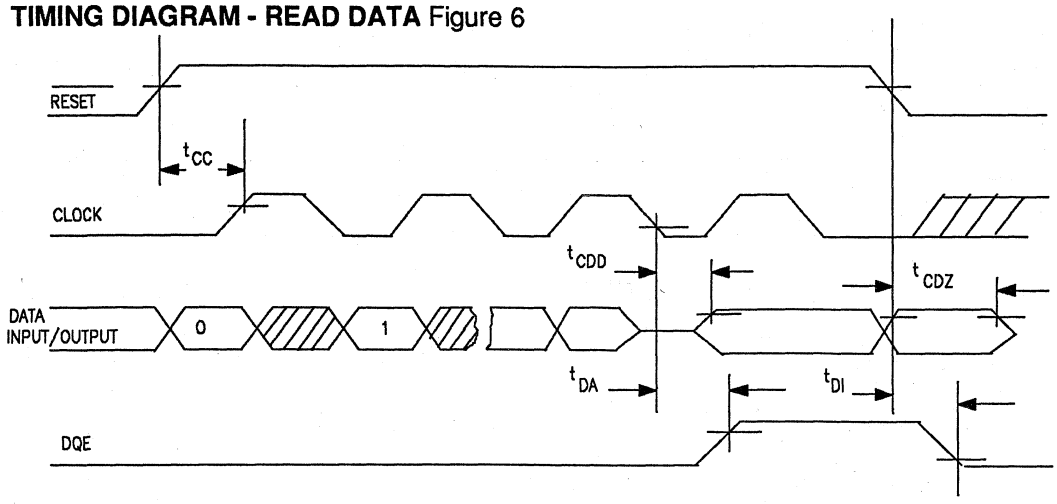
CRC GENERATION Figure 4



TIMING DIAGRAM - WRITE DATA Figure 5



TIMING DIAGRAM - READ DATA Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply	V_{CC}	-4.5	5.0	5.5	Volts	1
Input High Voltage	V_{IH}	2.2		V_{CC}	Volts	1
Input Low Voltage	V_{IL}	0.0		+0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-60		+60	uA	
I/O Leakage	I_{LO}	-10		+10	uA	
Output Current	I_{OH}	-1.0	-2.0		mA	2
Output Current	I_{OL}	2.0	3.0		mA	3
Operating Current	I_{OP}		60	120	mA	
Input Capacitance	C_{IN}		5		pF	
I/O Capacitance	C_{IB}		5		pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{cc} = 5V +/- 10%)

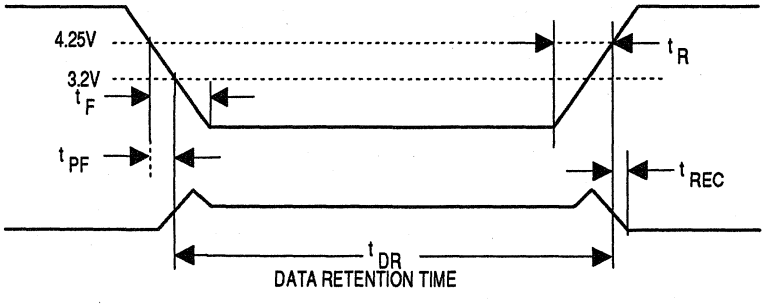
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CCI} Slew Rate	t_F	300			us	4
V_{CCI} Slew Rate	t_R	1			us	4
Power Down to PF\	t_{PF}	0			us	4
PF\ Recovery	t_{REC}			100	us	4

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V+/- 10%, 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
Data to CLK Hold	t_{CDH}	40			ns	2
Data to CLK Delay	t_{CDD}			125	ns	2,3,5
CLK Low Time	t_{CL}	500			ns	2
CLK High Time	t_{CH}	500			ns	2
CLK Frequency	f_{CLK}	DC		1	MHz	2
CLK Rise & Fall Time	t_R t_F			500	ns	
RST\ to CLK Setup	t_{CC}	1			us	2
CLK to RST\ Hold	t_{CCH}	40			ns	2
RST\ Inactive Time	t_{CWH}	125			ns	2
RST\ to D/Q High Z	t_{CDZ}			50	ns	2

NOTES:
1. All voltages are referenced to ground.
2. @ 2.4 volts.
3. @ 0.4 volts.
4. See Figure 7.

POWER-DOWN/POWER-UP CONDITION Figure 7

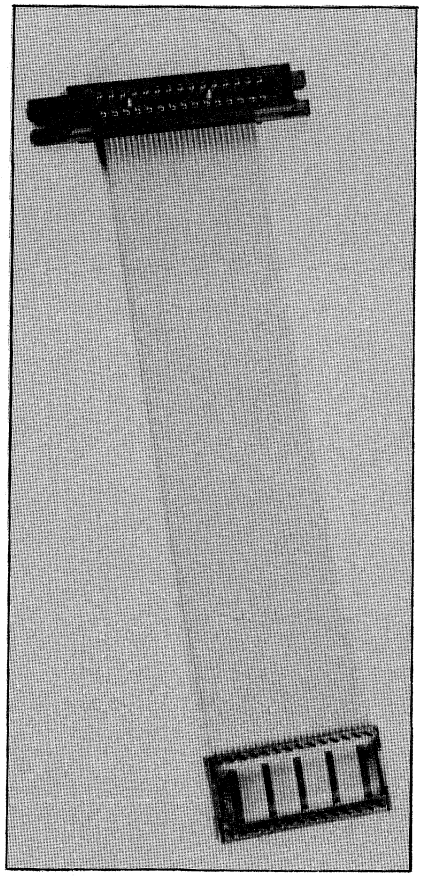


DALLAS SEMICONDUCTOR

DS9000
Bytewide Cable Harness

FEATURES

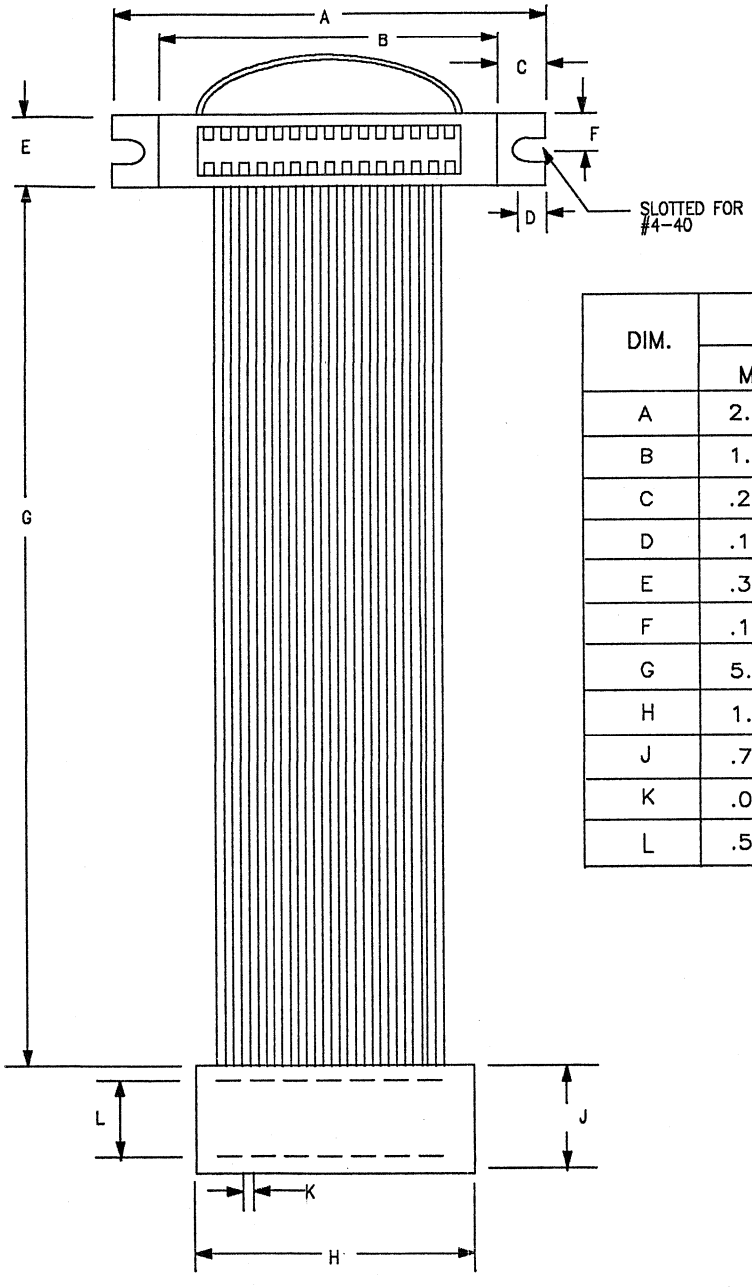
- Converts 30-position card edge to popular bytewide 28-pin DIP socket
- Bifurcated cantilever beam card edge design provides redundant contact
- Mechanical keys provide proper insertion and withdrawal of Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges
- 28-position DIP plug inserts into any standard 28-position IC DIP socket
- Color stripe indicates pin one on 28-pin DIP plug
- Standard six-inch cable length
- Interfaces directly to the DS6010 PC Port



DESCRIPTION

The DS9000 Bytewide Cable Harness is a specially designed cable harness which converts Dallas Semiconductor DS1217 Nonvolatile Read/Write Cartridges or any other 30-position card edge to the popular bytewide 28-pin DIP socket. An additional ground lead and dual key positions allow for proper insertion and withdrawal of Nonvolatile Read/Write Cartridges. A six-inch cable length allows for flexibility in end applications but does not substantially affect the performance characteristics of the DS1217.

DS9000
Bytewide Cable Harness



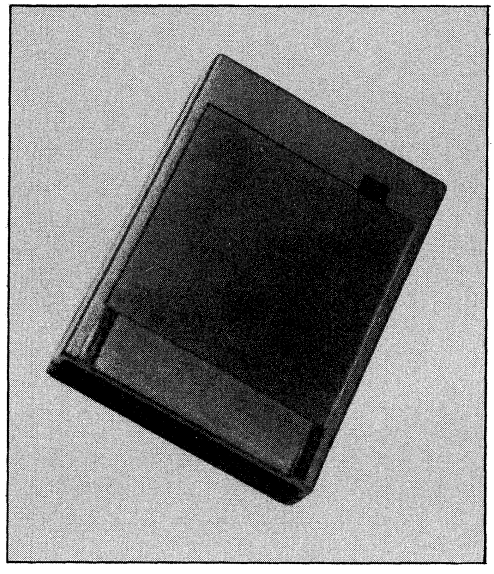
DIM.	INCHES	
	MIN.	MAX.
A	2.480	2.520
B	1.940	1.980
C	.260	.280
D	.160	.175
E	.395	.415
F	.195	.205
G	5.25	5.65
H	1.470	1.500
J	.715	.735
K	.090	.110
L	.590	.610

DALLAS SEMICONDUCTOR

DS9002
Cartridge Housing

FEATURES

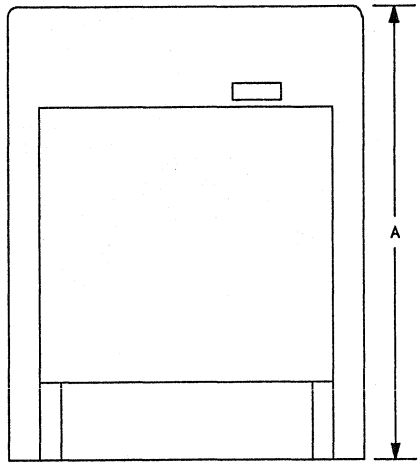
- Two-piece, snap together construction
- Matches form factor of Dallas Semiconductor DS1217 Nonvolatile Read/ Write Cartridges
- Made of rugged, flame-retardant ABS plastic
- Accepts DS9003 Cartridge Proto Board
- Opening for switch or jumper
- Component clearance of .175" solder side, .200" circuit side using .062" PCB



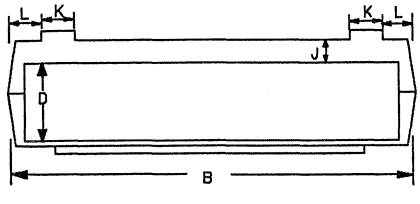
DESCRIPTION

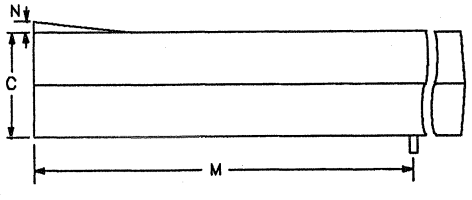
The DS9002 Cartridge Housing is a rugged, two-piece snap together cartridge housing designed for use in any portable cartridge application. Components can be either through-hole mounted or surface mounted on both sides depending upon density requirement and board design. The outside profile of the PCB should match the DS9003 Cartridge Proto Board. Applications include nonvolatile static RAM, ROM, or EPROM memory cartridges.

DS9002
CARTRIDGE HOUSING



DIM.	INCHES	
	MIN.	MAX.
A	3.020	3.040
B	2.280	2.300
C	.590	.610
D	.440	.460
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060



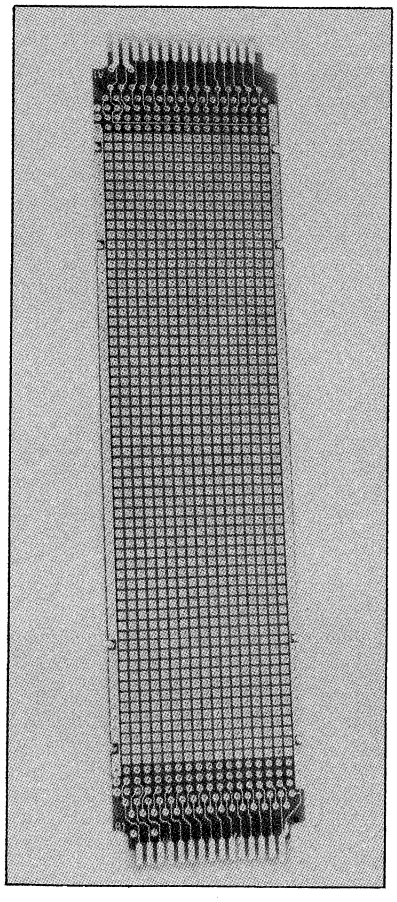


DALLAS SEMICONDUCTOR

DS9003
Cartridge Proto Board

FEATURES

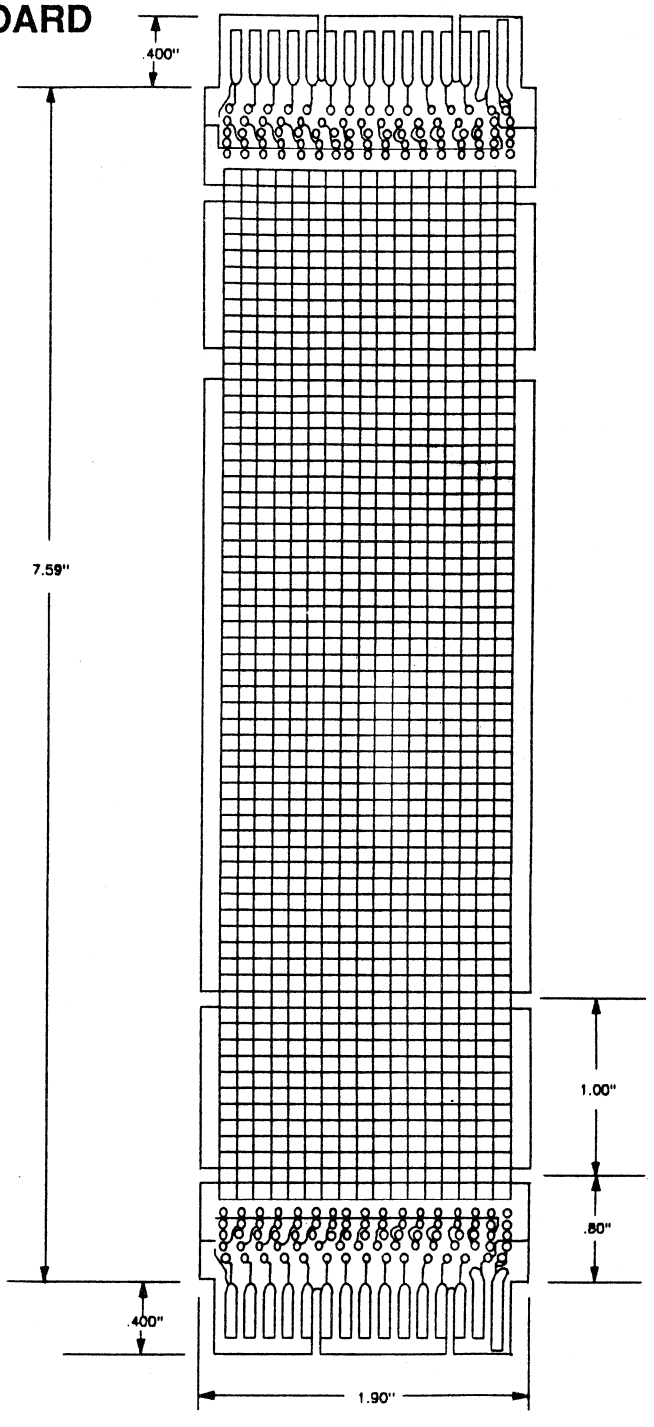
- Matches profile of DS1217 Nonvolatile Read/Write Cartridges
- Plated through-hole pattern for wire wrap or solder mount development
- Allows for a single double-size cartridge or two standard-size cartridges
- Gold-plated card edge fingers
- Connects to standard 28-pin DIP socket via DS9000 Bytewide Cable Harness
- Key slots provide for proper insertion and removal
- Separate full length power and ground buses for ease of layout



DESCRIPTION

The DS9003 Cartridge Proto Board is a developmental printed circuit board for prototyping portable hand-held cartridges. The gold-plated card edge connections conform to the popular 28-pin bytewide DIP socket pinout when used with the DS9000 Bytewide Cable Harness. The card profile matches that of the DS1217 Nonvolatile Read/Write Cartridges and can be used with the DS9002 Cartridge Housing.

DS9003
CARTRIDGE PROTO BOARD



DALLAS SEMICONDUCTOR

DS9020
Cartridge Clip

FEATURES

- Holds up to eight 1217M Nonvolatile Read/ Write Cartridges
- Fits within the panel opening of a half-height 5¼" disk drive
- Mounts with same brackets as disk drive
- Accepts cartridges ranging from 16K to 4M bits for capacity up to 4M bytes
- Four user-insertable cartridges plug into the front
- Four removable cartridges plug into the rear
- Standard bytewide pinout connects to JEDEC 28-pin DIP socket via ribbon cable
- Software-controlled banks maintain 32K x 8 JEDEC pin compatibility
- Indicator illuminates red while data is transferring
- Rugged and durable construction
- Wide operating temperature range of 0°C to 70°C

DESCRIPTION

The DS9020 Cartridge Clip is a housing with circuitry designed to interface up to eight nonvolatile read/write memory cartridges to a computer memory bus. The complete unit will fit in the same space that could otherwise hold a standard 5¼" half-height floppy or hard disk drive. Using a total of eight DS1217M-4 Nonvolatile Read/Write Cartridges in the DS9020 gives a density of four megabytes of transportable nonvolatile memory with the access time of static RAM. Four user-insertable memory cartridges plug into the front of the Cartridge Clip, while four removable cartridges plug into the rear. The Cartridge Clip connects to the computer via a ribbon cable into a standard bytewide JEDEC 28-pin DIP socket. Software-controlled bank switching techniques provide an expandable memory through a 32K x 8 window within the host computer's memory map. The DS9020 Cartridge Clip provides a rugged, solid-state storage alternative to rotating magnetic memory.

OPERATION

The DS9020 Cartridge Clip includes switching circuitry for up to 8 DS1217M cartridges. Connection to a computer memory bus is made via a 28-pin DIP adapter with the pinout as shown in Figure 1. Normal read and write memory cycles are directed through the 28-pin DIP and ribbon cable to one of eight cartridges. (See data sheets on the DS1217A and DS1217M Nonvolatile Read/Write Cartridges for normal read and write cycle timing.) A software-controlled switch selects only one cartridge at a time. An indicator on the front of the Cartridge Clip illuminates while the data is being transferred.

CARTRIDGE SELECTION

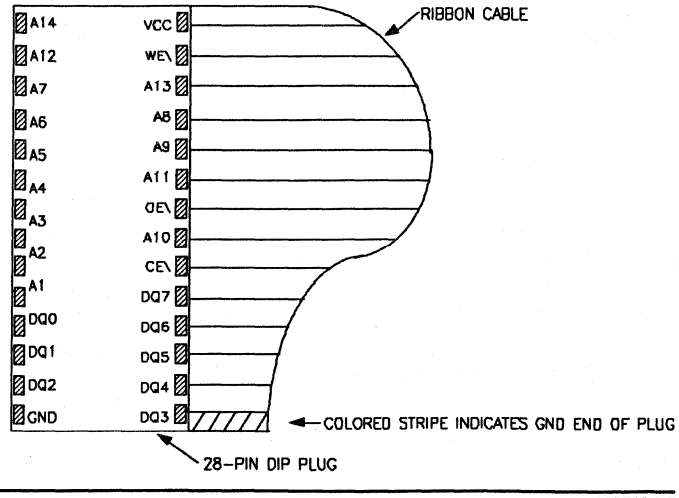
Initially, on power-up, all of eight possible cartridges in the Cartridge Clip are deselected. Cartridge selection is accomplished by matching a predefined pattern stored within the Cartridge Clip with a 16-cycle sequence on address lines A_0, A_1, A_2, and A_3. Prior to sending the 16-cycle sequence that will set the bank switch, a read cycle with bit pattern 1111 on address inputs A_0, A_1, A_2, and A_3 must be executed to initiate pattern entry. Each set of address inputs is clocked into the Cartridge Clip when the CE\ pin (Cartridge Clip Enable) is driven low. All 16 inputs to the Cartridge Clip must be consecutive read or write cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for address inputs A_1, A_2, and A_3; however, address line A_0 defines the cartridge number to be enabled as per Table 2.

Switching to a selected cartridge occurs on the rising edge of Cartridge Clip Enable when the last set of bits is input and a match has been established. After cartridge selection, subsequent Cartridge Clip Enables will be directed to the selected cartridge with an additional propagation delay of 150ns. (Note: this additional delay must be added to the respective DS1217 cartridge performance specifications when considering overall read and write cycle times. See Figure 3.) The selected cartridge position can be determined from Figure 2. Figure 4 is a block diagram and Figure 5 is an electrical wiring diagram of the DS9020. Figure 6 shows the mechanical and dimensional specifications of the Cartridge Clip.

ADDITIONAL ACCESSORY

Dallas Semiconductor offers the DS6010 PC Port, an I/O expansion board that connects the DS9020 into PCs, XTs, ATs, and compatible computers. For additional information contact Dallas Semiconductor.

CARTRIDGE CLIP Figure 1
28-Pin DIP Plug Interface Pinout



ADDRESS INPUT PATTERN Table 1

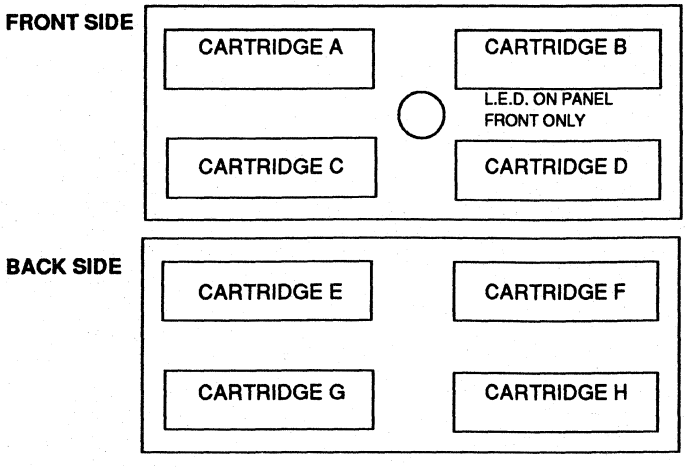
	Bit Sequence															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_0	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_1	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_2	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_3	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

x = See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	**A0 Bit Sequence**				
	11	**12**	**13**	**14**	**15**
All Cartridges Off	0	Don't Care	Don't Care	Don't Care	Don't Care
Cartridge A	1	0	0	0	0
Cartridge B	1	0	0	0	1
Cartridge C	1	0	0	1	0
Cartridge D	1	0	0	1	1
Cartridge E	1	0	1	0	0
Cartridge F	1	0	1	0	1
Cartridge G	1	0	1	1	0
Cartridge H	1	0	1	1	1

Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Pin 28 Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Level	V_{IH}	2.2		V_{CC}	V	1
Input Low Level	V_{IL}	0.0		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}		6	50	mA	2
Operating Current	I_{CC2}		15		mA	3
Operating Current	I_{CC3}		40		mA	4
Input Drive Low Level	I_{IL}			1.0	mA	5
Input Drive High Level	I_{IH}			0.5	mA	5
Output Drive @ 2.4V	I_{OH}	-1.0			mA	6
Output Drive @ 0.4V	I_{OL}	2.0			mA	6

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	500	750	pF	2
D/Q Capacitance	$C_{D/Q}$	500	750	pF	2

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Address Setup	t_{AS}	20			ns
Address Hold	t_{AH}	100			ns
Read Recovery	t_{RR}	80			ns

DS1217M CARTRIDGE TIMING WHILE INSTALLED IN THE DS9020

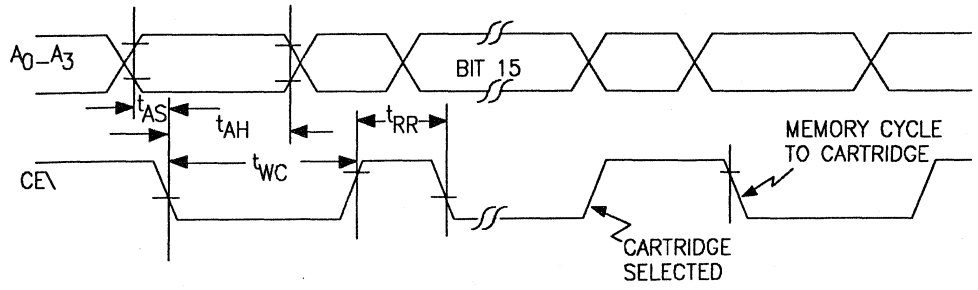
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Read Cycle Time	t_{RC}	440			ns
Access Time	t_{ACC}			400	ns
OE\ to Output Valid	t_{OE}			275	ns
CE\ to Output Valid	t_{CO}			400	ns
OE\ or CE\ to Output Active	t_{COE}	50			ns
Output High Z from Deselection	t_{OD}			125	ns
Output Hold from Address Change	t_{OH}	10			ns
Read Recovery Time	t_{RR}	40			ns
Write Cycle Time	t_{WC}	440			ns
Write Pulse Width	t_{WP}	350			ns
Address Setup Time	t_{AW}	40			ns
Write Recovery Time	t_{WR}	40			ns
Output High Z from WE\	t_{ODW}			100	ns
Output Active from WE\	t_{OEW}	10			ns
Data Setup Time	t_{DS}	280			ns
Data Hold Time from WE\	t_{DH}	25			ns

See DS1217M data sheet for timing diagrams.

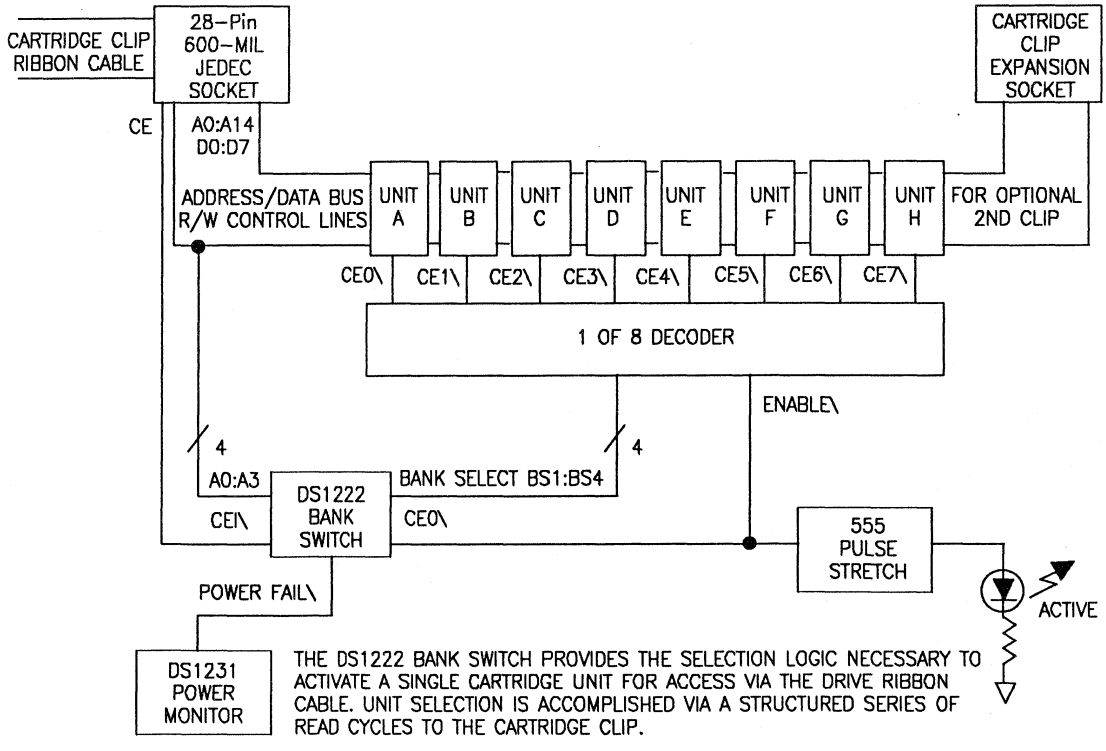
TIMING DIAGRAM—CARTRIDGE SELECTION Figure 3



NOTES:

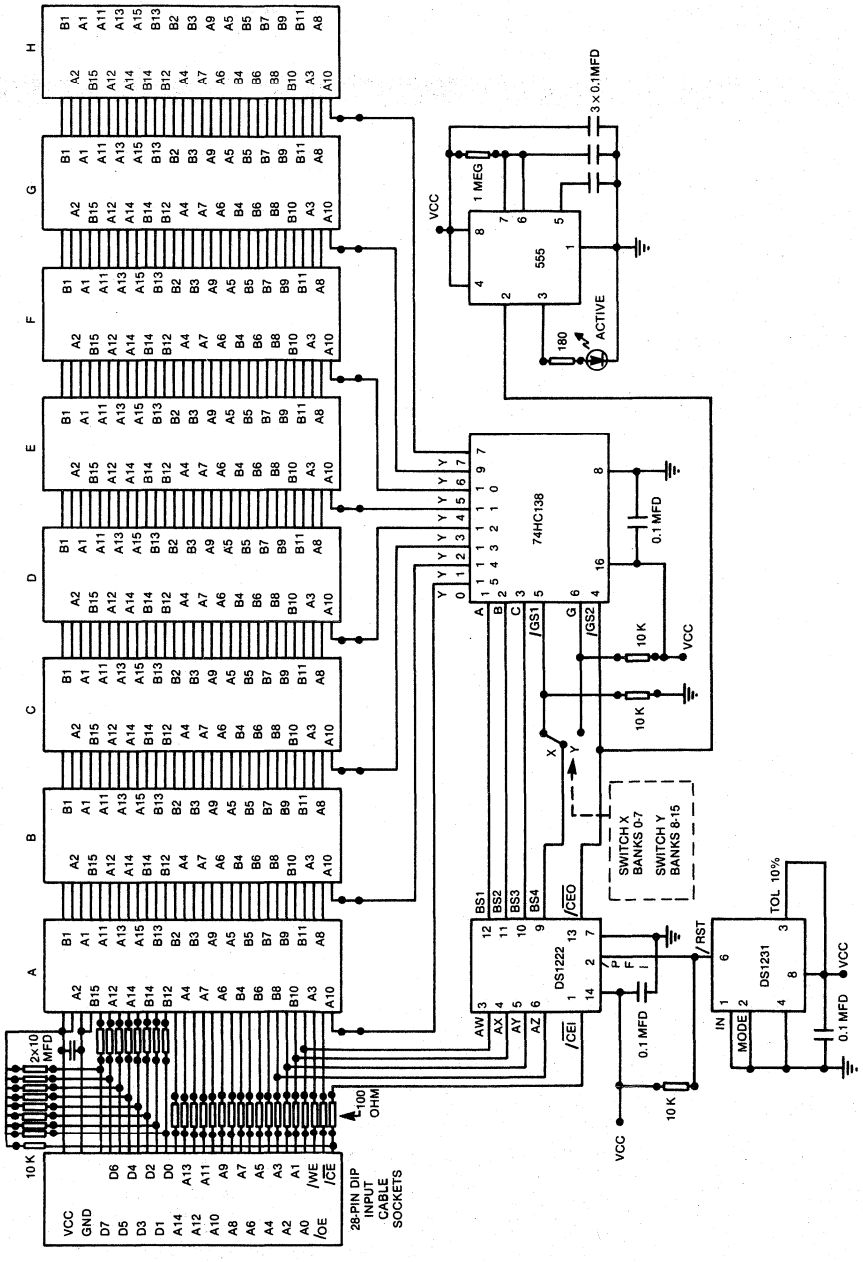
1. All voltages are referenced to ground (Pin 14).
2. Cartridge Clip empty.
3. Cartridge Clip loaded to capacity with CE\ at high level.
4. Cartridge Clip loaded to capacity with CE\ at low level.
5. Includes all address, data, and control lines.
6. Output drive comes from installed cartridge.

BLOCK DIAGRAM Figure 4



THE DS1231 POWER MONITOR PROVIDES FAIL DETECTION AND POWER–UP RESET FUNCTIONS. ACCESS TO THE CARTRIDGE UNITS IS DENIED WHEN POWER IS LOW AND UNTIL UNIT SELECTION PROTOCOL IS ACTIVATED ON SYSTEM POWER–UP.

Figure 5

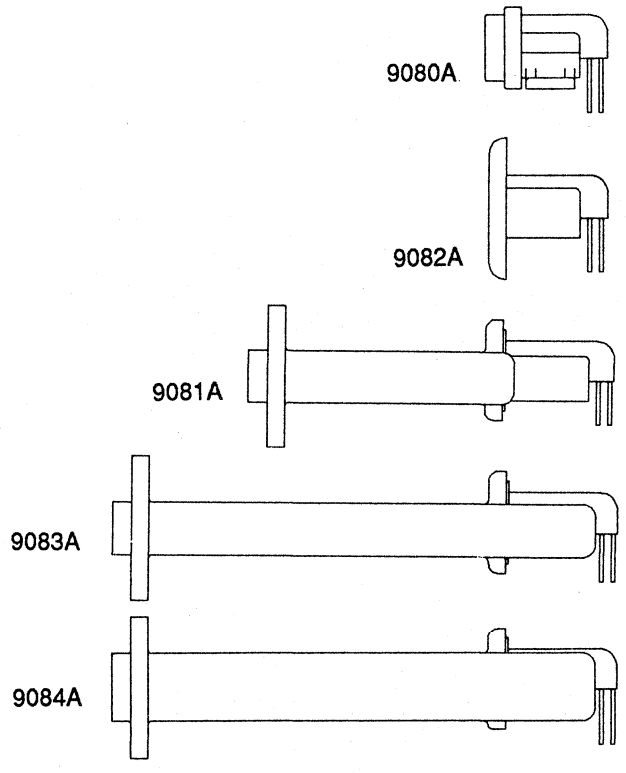

28-PIN DIP INPUT CABLE SOCKETS
VCC
GND
D7
D5
D3
D1
A14
A12
A10
A8
A6
A4
A2
A0
/OE
A11
A9
D6
D4
D2
D0
A13
/WE
/CE
10 K
2×10 MFD
100 OHM
74HC138
DS1222
DS1231
555
1 MEG
3×0.1MFD
ACTIVE
180
0.1 MFD
10 K
SWITCH X BANKS 0-7
SWITCH Y BANKS 8-15
TOL 10%
VCC

DALLAS SEMICONDUCTOR

DS908xx
CyberKey/Card Receptacles

FEATURES

- Solid base metal contacts
- Durable and rugged
- Guided entry on receptacle
- High insertion force
- Greater than 50,000 cycle life



PART NUMBER	DESCRIPTION
DS9080V	Flush mount CyberKey receptacle, vertical PCB mount
DS9080A	Flush mount CyberKey receptacle, right angle PCB mount
DS9081V	Recessed CyberKey receptacle, vertical PCB mount
DS9081A	Recessed CyberKey receptacle, right angle PCB mount
DS9082V	Flush mount CyberCard receptacle, vertical PCB mount
DS9082A	Flush mount CyberCard receptacle, right angle PCB mount
DS9083V	Recessed CyberCard receptacle, vertical PCB mount
DS9083A	Recessed CyberCard receptacle, right angle PCB mount
DS9084V	Recessed CyberCard EV receptacle, vertical PCB mount
DS9084A	Recessed CyberCard EV receptacle, right angle PCB mount

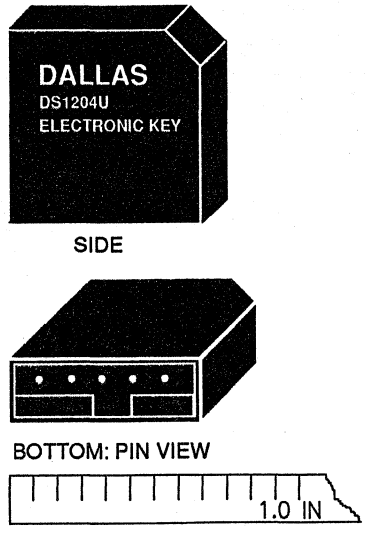
Security Products

DALLAS SEMICONDUCTOR

DS1204U
Electronic Key

FEATURES
- Cannot be deciphered by reverse engineering
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit security match code virtually prevents deciphering by exhaustive search with over 10^{19} possibilities
- 128 bits of secure read/write memory create additional barriers by permitting data changes as often as needed
- Rapid erasure of identification security match code and secure read/write memory can occur if tampering is detected
- Over 10 years of data retention with no limitations or restrictions on write cycle
- Low-power CMOS circuitry
- Four million bps data rate
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN DESCRIPTION



PIN NAMES(\ Denotes Condition Low)

Pin 1 -	V_{CC}	+5 Volts
Pin 2 -	RST\	Reset
Pin 3 -	DQ	Data Input/Output
Pin 4 -	CLK	Clock
Pin 5 -	GND	Ground

DESCRIPTION

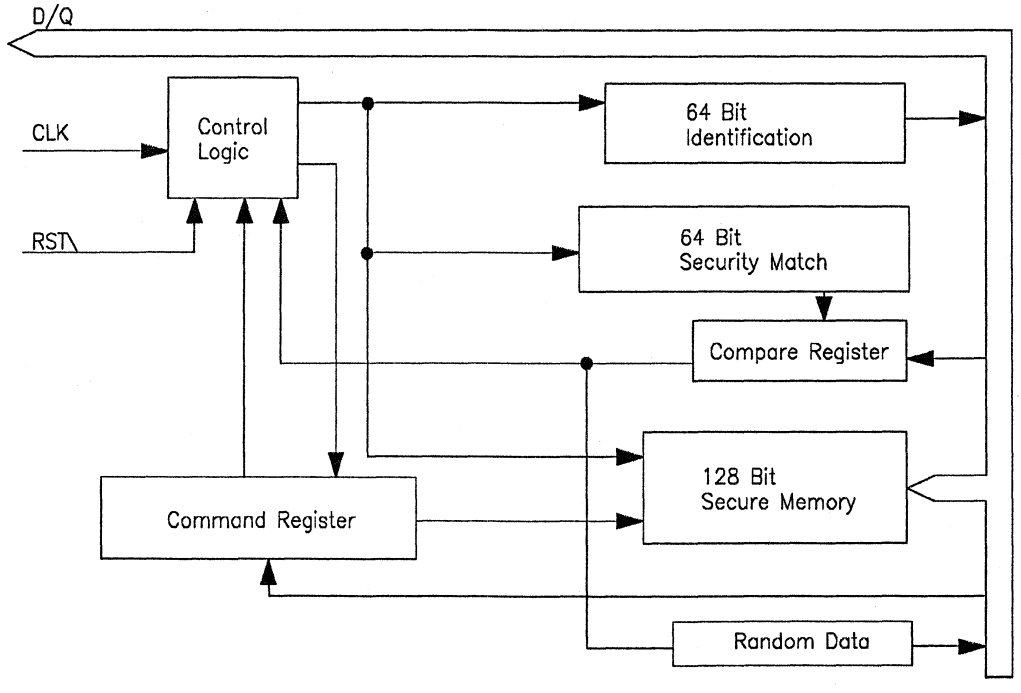
The DS1204U Electronic Key is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 128 bits of read/write nonvolatile memory. The 64-bit identification code and the security match code are programmed into the key via a special program mode operation. After programming, the key follows a procedure with a serial format to retrieve or update data. Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), Reset\ (RST\), and Data Input/Output (DQ).

Low pin count and a guided entry for mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

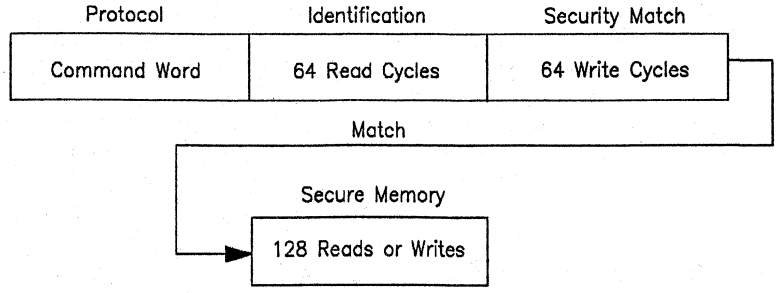
OPERATION - NORMAL MODE

The Electronic Key has two modes of operation: normal and program. The block diagram (see Figure 1) illustrates the main elements of the key when used in the normal mode. To initiate data transfer with the key, RST\ is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines normal operation for read or write, or communications are ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the key are reads. Data is clocked out of the key on the high-to-low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 2 is a summary of normal mode operation and Figure 3 is a flow chart of the normal mode sequence.

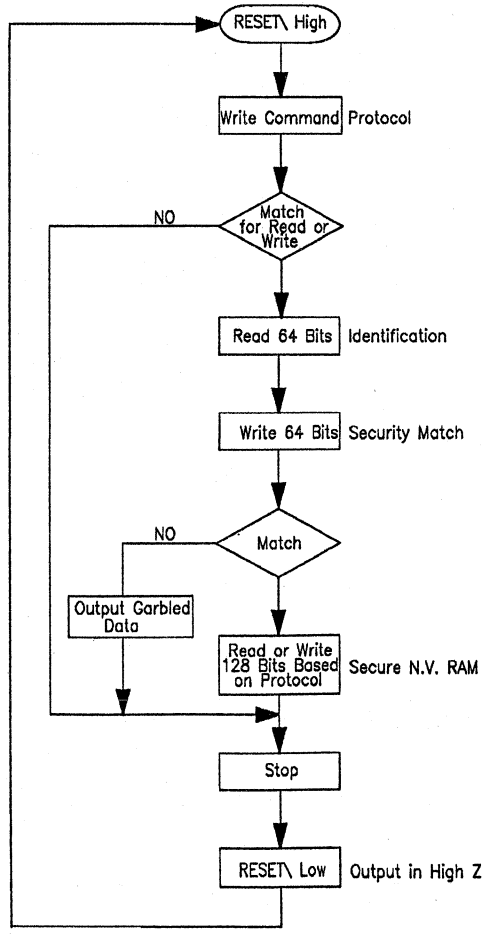
BLOCK DIAGRAM - NORMAL MODE Figure 1



SEQUENCE - NORMAL MODE Figure 2



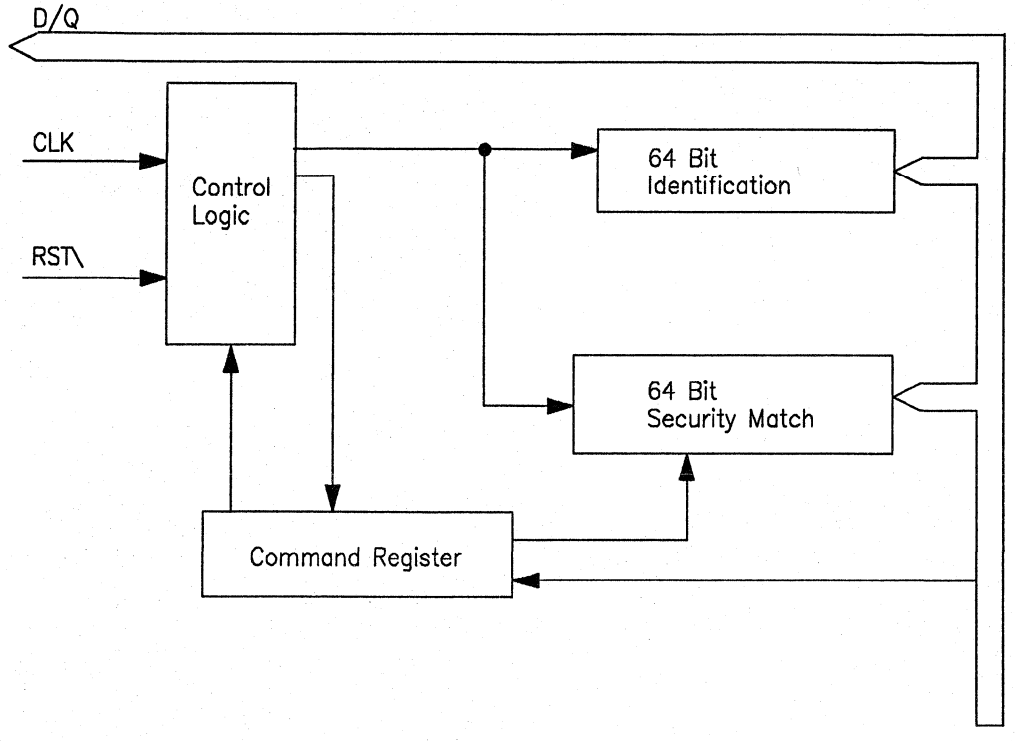
FLOW CHART - NORMAL MODE Figure 3



PROGRAM MODE

The block diagram in Figure 4 illustrates the main elements of the key when used in the program mode. To initiate the program mode, RST\ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact pattern that defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, then the 128 bits that follow are written to the identification memory and the security match memory. Figure 5 is a summary of program mode operation and Figure 6 is a flow chart of program mode operation.

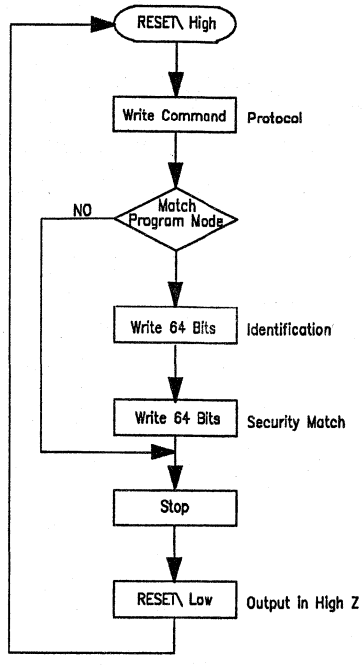
BLOCK DIAGRAM - PROGRAM MODE Figure 4



SEQUENCE - PROGRAM MODE Figure 5

Protocol	Identification	Security Match
Command Word	64 Write Cycles	64 Write Cycles

FLOW CHART - PROGRAM MODE Figure 6



COMMAND WORD

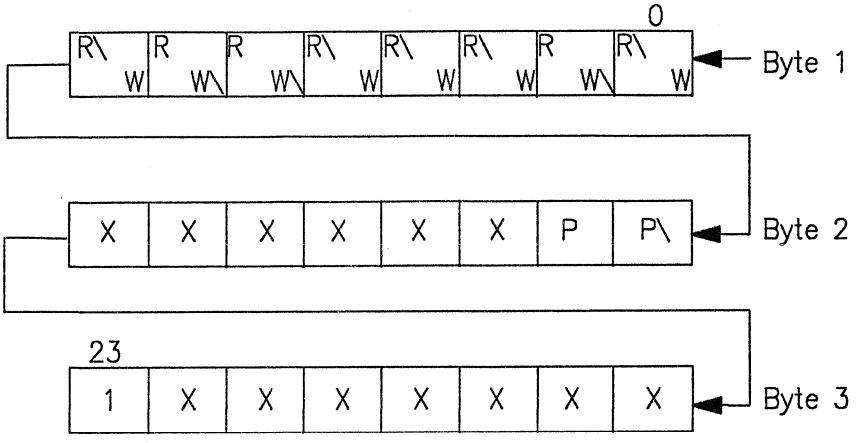
Each data transfer for the normal and program mode begins with a three-byte command word as shown in Figure 7. As defined, the first byte of the command word specifies whether the 128-bit nonvolatile memory will be written into or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

The 8 bit pattern for read is 01100010. The pattern for write is 10011101. The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern that selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining six bits of byte 2 and the first seven bits of byte 3 form unique patterns that allow multiple keys to reside on a common bus. As such, each respective code pattern must be written exactly for a given device or data transfer will abort. Dallas Semiconductor has five patterns available as standard products per the chart in Figure 7. Each pattern corresponds to a specific part number. Under special contract with Dallas Semiconductor, the user can specify any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

NOTE: Contact the Dallas Semiconductor sales office for a special command word code assignment that makes possible an exclusive blank key.

COMMAND WORD Figure 7



DS1204U-1	0	0	0	0	0	0	P	P\	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-2	0	0	0	0	0	1	P	P\	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-3	0	0	0	0	1	0	P	P\	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-4	0	0	0	0	1	1	P	P\	Byte 2
	1	0	1	0	0	0	0	0	Byte 3
DS1204U-5	0	0	0	1	0	0	P	P\	Byte 2
	1	0	1	0	0	0	0	0	Byte 3

RESET AND CLOCK CONTROL

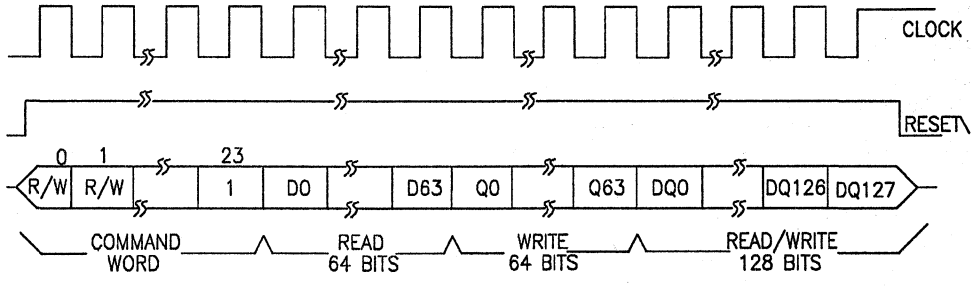
All data transfers are initiated by driving the RST\ input high. The RST\ input serves three functions. First, it turns on control logic, which allows access to the command register for the command sequence. Second, the RST\ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for RST\ of 2 mA @ 3.0 volts is required. However, if the V_{CC} pin is connected to a 5-volt source within nominal limits, the RST\ is not used as a source of power and input levels revert to normal V_{IH} and V_{IL} inputs with a drive current requirement of 500 uA. Third, the RST\ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the RST\ pin is low and the DQ pin goes to a high impedance state. When data transfer to the key is terminated using RST\, the transition of Reset\ must occur while the clock is at a high level to avoid disturbing the last bit of data. Data transfer is illustrated in Figure 8 for normal mode and Figure 9 for program mode.

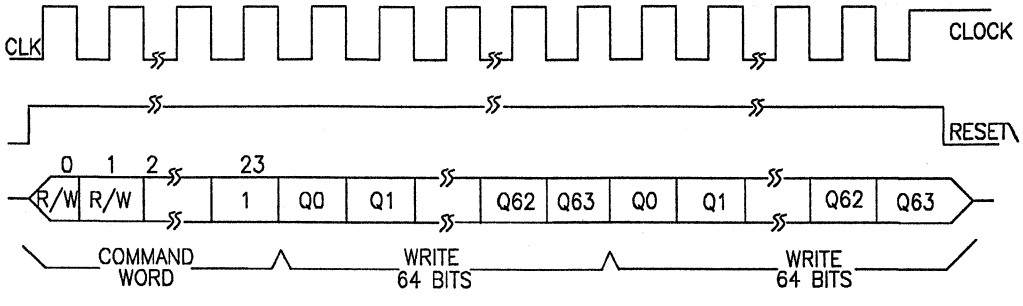
KEY CONNECTIONS

The key is designed to be plugged into a standard 5-pin, 0.1-inch center SIP receptacle. A guide is provided to prevent the key from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the key pins can be determined to ensure connection integrity before data transfer begins. CLK, RST\, and DQ all have internal 20K ohm pulldown resistors to ground that can be sensed by a reading device.

DATA TRANSFER - NORMAL MODE Figure 8



DATA TRANSFER - PROGRAM MODE Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1, 8, 10
Logic 0	V_{IL}	-0.3		+0.8	V	1
RESET\ Logic 1	V_{IHE}	3.0			V	1, 9, 11
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	*u* A	4
Output Leakage	I_{LO}			+500	*u* A	
Output Current @2.4V	I_{OH}	-1			mA	
Output Current @0.4V	I_{OL}			+2	mA	
RST\ Input Resistance	Z_{RST}	10		60	K ohms	
D/Q Input Resistance	Z_{DQ}	10		60	K ohms	
CLK Input Resistance	Z_{CLK}	10		60	K ohms	
RST\ Current @3.0V	I_{RST}			2	mA	6, 9, 13
Active Current	I_{CC1}			6	mA	6
Standby Current	I_{CC2}			2.5	mA	6

CAPACITANCE

(t_A=25°C)

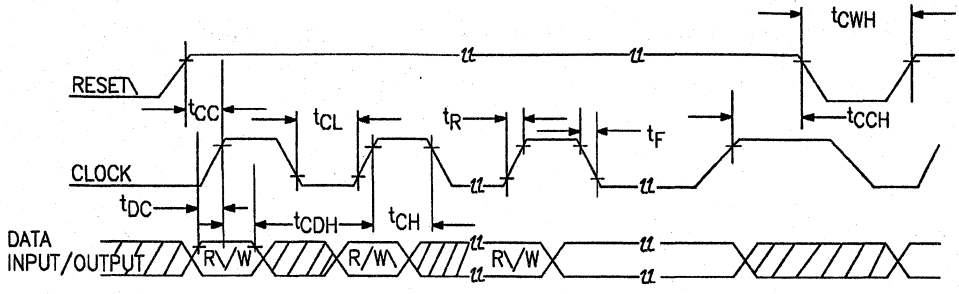
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

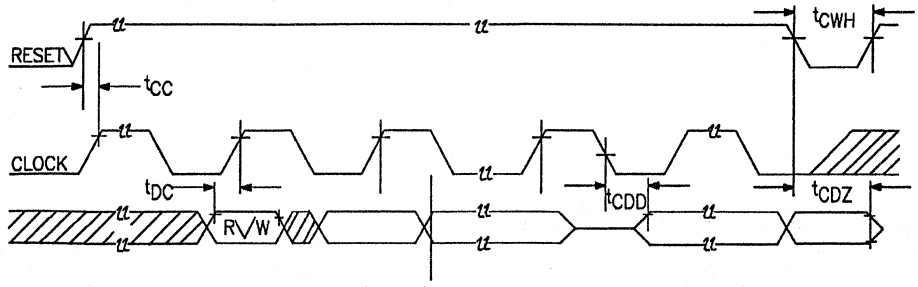
(0°C to 70°C, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2, 7
CLK to Data Hold	t_{CDH}	40			ns	2, 7
CLK to Data Delay	t_{CDD}			100	ns	2, 3, 5, 7
CLK Low Time	t_{CL}	125			ns	2, 7
CLK High Time	t_{CH}	125			ns	2, 7
CLK Frequency	f_{CLK}	D C		4.0	MHz	2, 7
CLK Rise & Fall	t_R, t_F			500	ns	2, 7
RST\ to CLK Setup	t_{CC}	1			ns	2, 7
CLK to RST\ Hold	t_{CCH}	40			ns	2, 7
RST\ Inactive Time	t_{CWH}	125			ns	2, 7, 14
RST\ to I/O High Z	t_{CDZ}			50	ns	2, 7

TIMING DIAGRAM - WRITE DATA



TIMING DIAGRAM - READ DATA



NOTES:

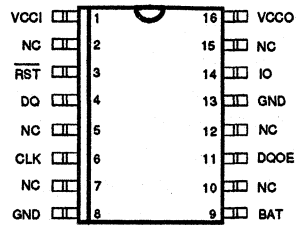
1. All voltages are referenced to GND.
2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10ns maximum rise and fall time.
3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
4. For CLK, D/Q, and RST\.
5. Load capacitance = 50 pF.
6. Measured with outputs open.
7. Measured at V_{IH} of RST\≥ 3.0V when RST\ supplies power.
8. Logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and RST\ + 0.3 volts if the RST\ pin supplies power.
9. Applies to RST\ when V_{CC} < 3.0V.
10. Input levels apply to CLK, DQ, and RST\ while V_{CC} is within nominal limits. When V_{CC} is not connected to the key, then RST\ input reverts to V_{IHE}.
11. RST\ logic 1 maximum is V_{CC} + 0.3 volts if the V_{CC} pin supplies power and 5.5 volts maximum if RST\ supplies power.
12. Each DS1204U is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
13. Average AC RST\ current can be determined using the following formula:
    $I_{TOTAL} = 2 + I_{LOAD\ DC} + (4 \times 10^{-3})\ (C_L + 140)^f$
    I_{TOTAL} and I_{LOAD} are in mA; C_L is in pF; f is in MHz.
    Applying the above formula, a load capacitance of 50 pF running at a frequency of 4.0 MHz gives an I_{TOTAL} of 5 mA.
14. When RST\ is supplying power t_{CWH} must be increased to100 ms average.

DALLAS SEMICONDUCTOR

DS1205
MultiKey Chip

FEATURES
- Four addressable read/write data partitions
- Three secure read/write data partitions of 384 bits each
- One non-secure read/write data partition of 512 bits
- Secure data cannot be deciphered by reverse engineering
- Supports a hierarchical privilege system
- Partitioned memory thwarts pirating
- 64-bit password and I.D. fields provide a barrier against accidental key erasure
- Maximum data transfer rate of 2 million bits/second
- Low-power CMOS circuitry
- 3-wire bus-compatible
- 1-wire "touch" bus-compatible
- Applications include software authorization, proprietary data, financial transactions, secure personnel areas, and systems access control.

PIN DESCRIPTION



16-PIN SOIC
(150 MIL)

PIN NAMES

VCCI	+5V Supply
RST \	Reset (3-Wire)
DQ	Data (3-Wire)
CLK	Clock (3-Wire)
GND	Ground
BAT	Battery (+)
DQOE	Data Avail (1-Wire)
IO	Data I/O (1-Wire)

DESCRIPTION

The DS1205 MultiKey is an enhanced version of the DS1204U Electronic Key which has both a standard 3-wire interface, data, clock, and reset, and a 1-wire "touch" interface. The DS1205 MultiKey has three secure read/write subkeys which are each 384 bits in length. In addition, there is a 512-bit read/write scratchpad which can be used as a non-secure data area or as a holding register for data transfer to one of the three subkeys. Each subkey within the part is uniquely addressable.

OPERATION

The writing of a command word to the DS1205 MultiKey specifies the operation to be performed and the subkey to be operated on. There are two classes of operations available for the DS1205 MultiKey. These are operations which access one of the three secure read/write subkeys and operations which access the read/write scratchpad (Figure 1).

COMMAND WORD

The 24-bit command word is grouped into three fields of eight bits each. These byte-sized fields specify the subkey which is to be accessed, the starting byte address for the data transfer operation, and the type of command to be performed. The starting byte address and the subkey identifier fields are required to be given in both true and complement form. If these values do not match, the access to the part will be terminated (Figure 2).

The first byte of the command word is made up of the complement of the 2-bit subkey code, identifying which subkey is being accessed, and the complement of the 6-bit address field, which specifies the starting byte address of the given subkey to be accessed. The second byte of the command word consists of the 2-bit subkey code and the 6-bit starting byte address. The third byte of the command word is the 8-bit function code which defines which of the six commands is to be executed. Each command is subkey- and address-specific and, as such, each command precludes the use of certain subkey codes and starting address locations. Figure 3 illustrates the subkey codes, starting address locations, and function codes that are valid for each of the six command operations.

SECURE SUBKEY COMMANDS

Each secure subkey within the DS1205 MultiKey is comprised of a 64-bit I.D. field, a 64-bit password field, and a 384-bit secured data field (Figure 4). The three commands which operate on the secure subkeys are as follows :

1) Set password
2) Set secure data
3) Get secure data

SET PASSWORD

The Set Password command is used to enter data into the I.D. field and the password field of the selected subkey. Upon recognition of the correct I.D., the DS1205 MultiKey will erase the entire contents of the selected subkey and proceed to rewrite the 64-bit I.D. field and the 64-bit password field. The flow sequence is shown in Figure 5.

SET SECURE DATA

The Set Secure Data command is used to enter data into the selected subkey. The first 64 bits of the data stream must contain the password for the selected subkey. If the received password does not match the password field for the selected subkey, the DS1205 MultiKey will terminate the transaction immediately. The flow sequence is shown in Figure 6.

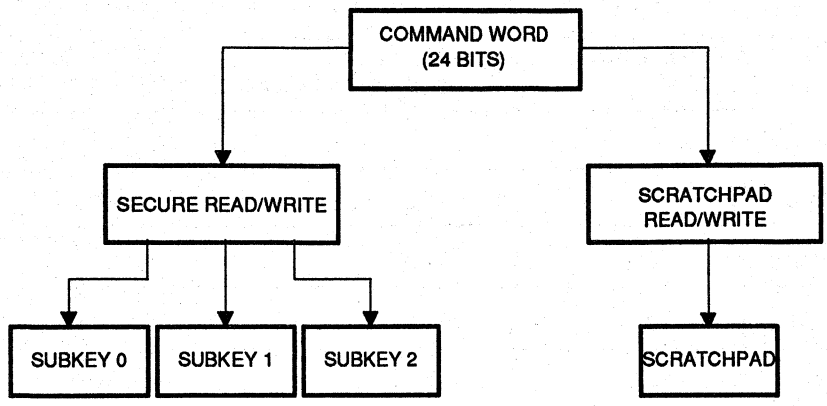
GET SECURE DATA

The Get Secure Data command is used to retrieve secured data from the selected subkey. The password for the selected subkey must be transmitted to the DS1205 MultiKey immediately after the command word. If the received password fails to match the password field for the selected subkey, the DS1205 MultiKey will output randomly generated data instead of the secured data. The flow sequence is shown in Figure 7.

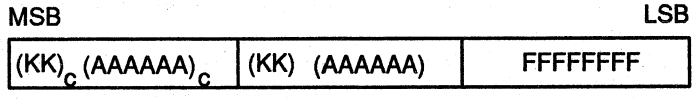
SCRATCHPAD READ/WRITE COMMANDS

The 512-bit Read/Write Scratchpad of the DS1205 MultiKey is not password-protected and is accessible beginning at any byte boundary. The scratchpad can be used to store unsecured data or it can be used to build up a data structure which can be verified and then

COMMAND OPERATIONS Figure 1



COMMAND WORD STRUCTURE Figure 2



(KK) = Two-bit number specifying which partition is to be accessed. 00 specifies subkey 0. 01 specifies subkey 1. 10 specifies subkey 2. 11 specifies the scratchpad.

$(KK)_C$ = Complement of (KK) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

(AAAAAA) = Address field containing address bits that define the starting byte address in the scratchpad and define the starting byte address in the secure data field for access to subkeys zero through three.

$(AAAAAA)_C$ = Complement of (AAAAAA) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

FFFFFFFF = Function code field. Specifies the action to be taken.

VALID SUBKEY CODES, STARTING ADDRESS LOCATIONS, AND FUNCTION CODES FOR EACH COMMAND WORD Figure 3

COMMAND	VALID SUBKEY CODE KK	VALID BYTE ADDRESS AAAAAA	VALID COMMAND CODE FFFF FFFF
Set Scratchpad	11	0 - 63	1001 0110
Get Scratchpad	11	0 - 63	0110 1001
Set Secure Data	00, 01, 10	16 - 63	1001 1001
Get Secure Data	00, 01, 10	16 - 63	0110 0110
Set Password	00, 01, 10	000000	0101 1010
Move Block	00, 01, 10	000000	0011 1100

transferred to a secure subkey. The three commands which operate on the read/write scratchpad are as follows :

1) Set scratchpad data
2) Get scratchpad data
3) Move block

SET SCRATCHPAD DATA

The Set Scratchpad Data command is used to enter data into the DS1205 MultiKey scratchpad. The command word must specify the starting byte address for the data transfer. Valid byte addresses are 0 through 63. The DS1205 MultiKey will write data to the scratchpad until byte 63 has been written or until the RST\ line goes to a logic low level. The flow sequence is shown in Figure 8.

GET SCRATCHPAD DATA

The Get Scratchpad data command is used to retrieve data from the 512-bit scratchpad. The command word must specify the starting byte address for the data retrieval. Valid byte addresses are 0 through 63. The DS1205 MultiKey will retrieve data from the scratchpad until byte 63 has been read or the RST line goes to a logic low level. The flow sequence is shown in Figure 9.

MOVE BLOCK

The Move Block command is used to transfer data, which has been previously entered into the scratchpad and verified, to one of the three secure subkeys. Data can be transferred as one large block of 512 bits or it can be transferred in blocks of 64 bits each (Figure 10). There are nine valid block selectors which are used to specify which block or blocks are to be transferred (Figure 11). As a further precaution against accidental erasure of a secure subkey, the password field of the block being transferred must match the password field of the selected secure subkey. If the passwords fail to match, the operation is terminated. The flow sequence is shown in Figure 12.

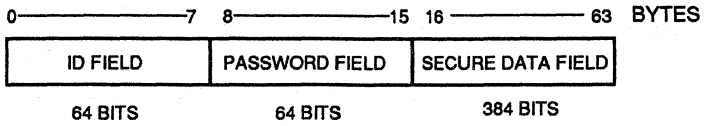
1-WIRE INTERFACE

When the "touch" interface is used, all communications to and from the DS1205 MultiKey are accomplished via a single interface lead. Data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

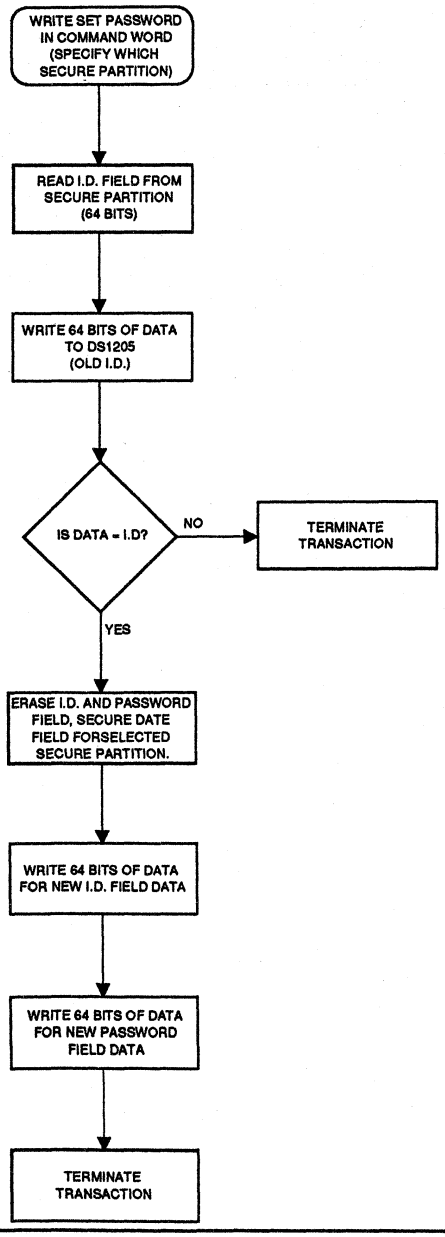
WRITE TIME SLOTS

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic

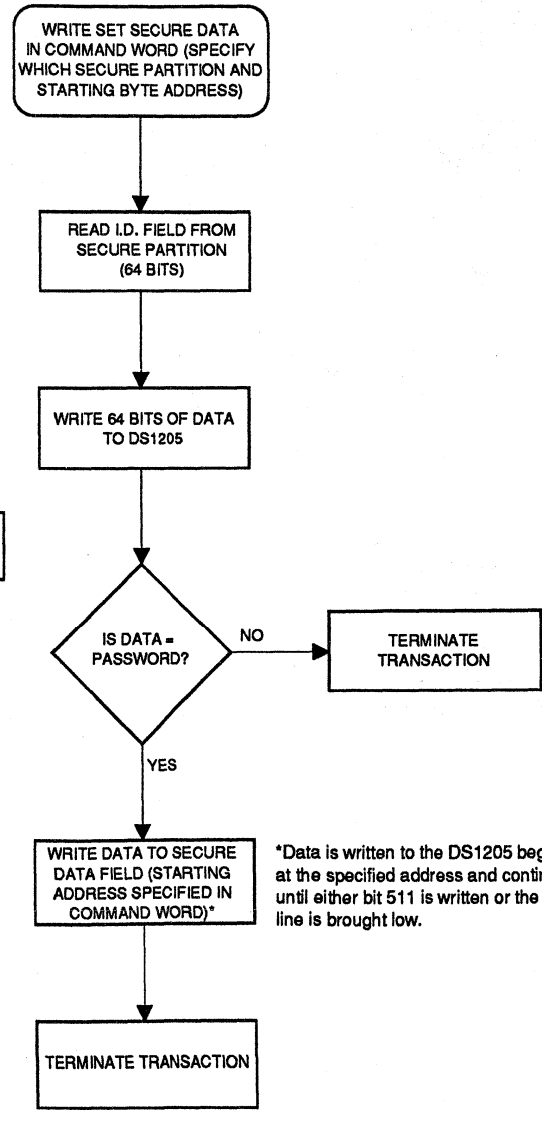
SUBKEY ORGANIZATION Figure 4



SET PASSWORD Figure 5

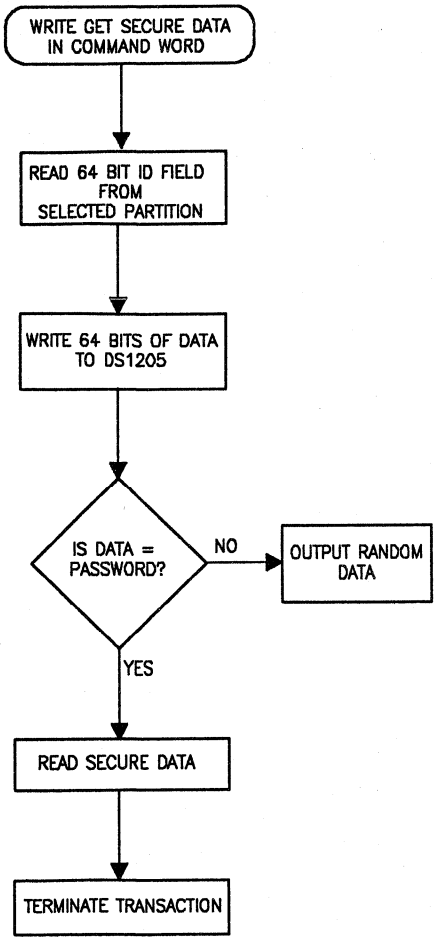


SET SECURE DATA Figure 6

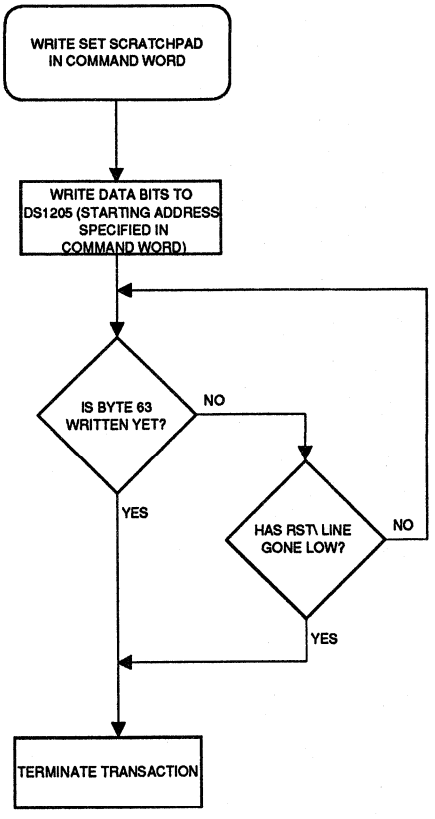


*Data is written to the DS1205 beginning at the specified address and continuing until either bit 511 is written or the RST line is brought low.

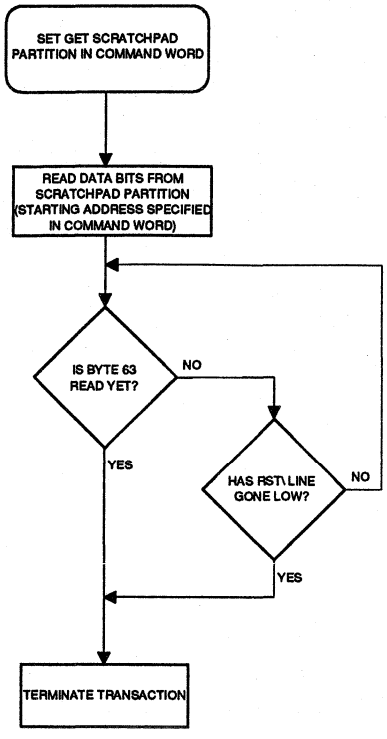
GET SECURE DATA Figure 7



SET SCRATCHPAD Figure 8



GET SCRATCHPAD Figure 9



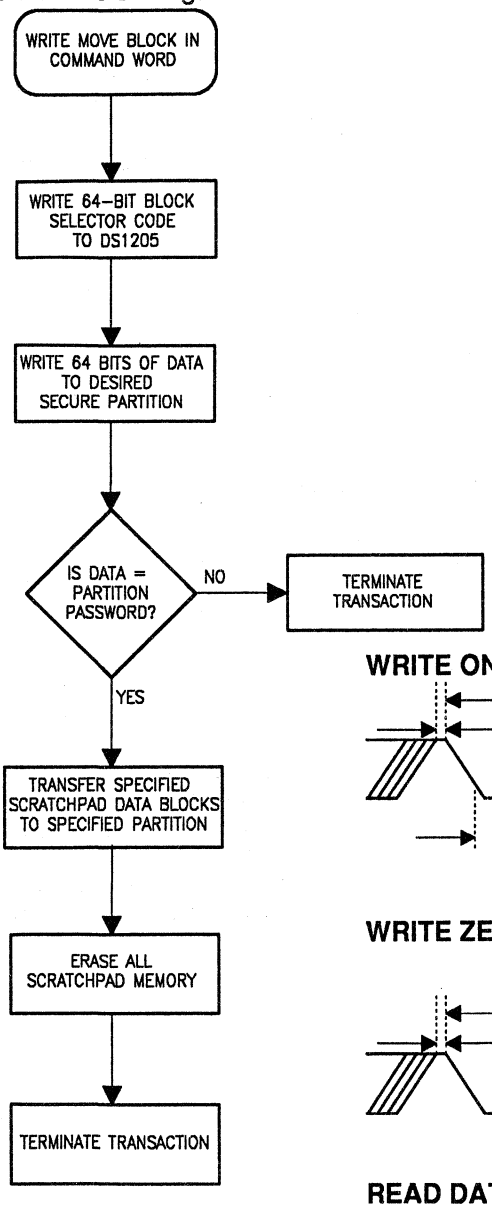
BLOCK SELECTIONS Figure 10

BLOCK NUMBER	BYTE ADDRESS IN: SCRATCHPAD	SUBKEY
0	0-7	0-7(ID)
1	8-15	8-15 (PASSWORD)
2	16-23	16-23 (PASSWORD)
3	24-31	24-31 (SECURED)
4	32-39	32-39 (SECURED)
5	40-47	40-47 (SECURED)
6	48-55	48-55 (SECURED)
7	56-63	(56-63 (SECURED)

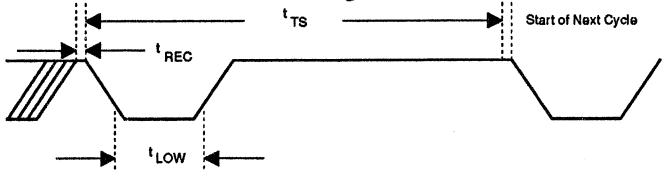
BLOCK SELECTOR CODES FOR MOVE BLOCK COMMAND Figure 11

BLOCK #	SELECTOR CODE
0	4C69 6E64 9DB3 9A9A (H)
1	4C69 919B 624C 9A9A (H)
2	4C96 6E9B 62B3 659A (H)
3	4366 616B 6D43 6A6A (H)
4	BC99 9E94 92BC 9595 (H)
5	B369 9164 9D4C 9A65 (H)
6	B396 6E64 90B3 6565 (H)
7	B396 919B 624C 6565 (H)
ALL BLOCKS	7FFA 5D57 517F 5656 (H)

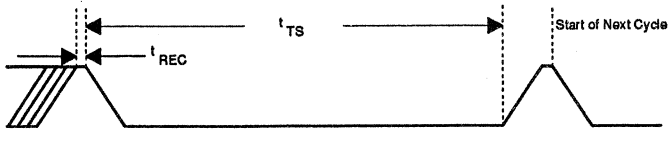
MOVE BLOCK Figure 12



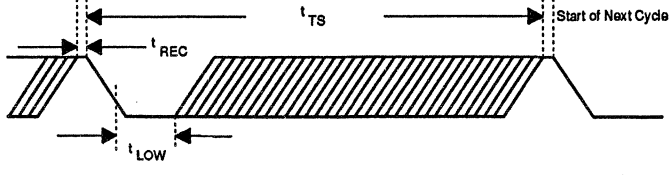
WRITE ONE TIME SLOT Figure 13



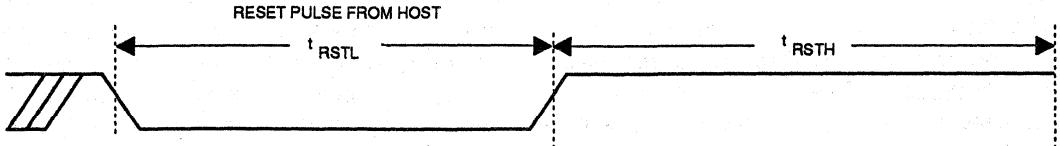
WRITE ZERO TIME SLOT Figure 14



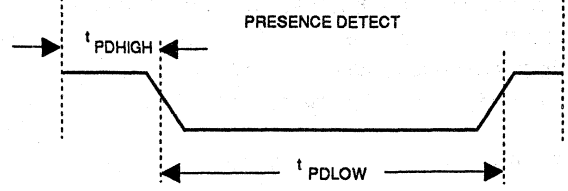
READ DATA TIME SLOTS Figure 15



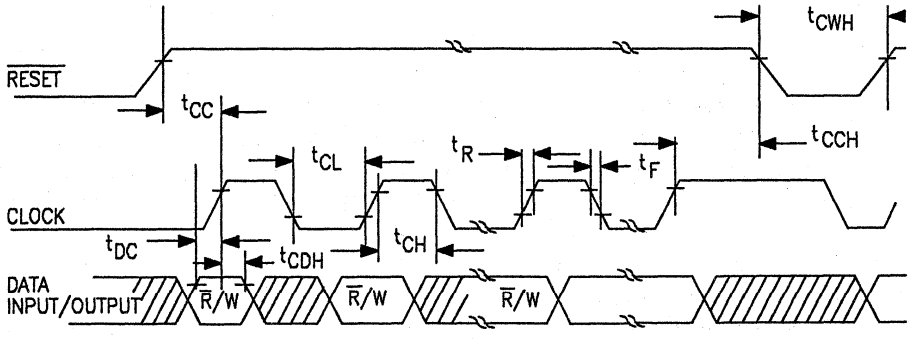
PRESENCE DETECT Figure 16



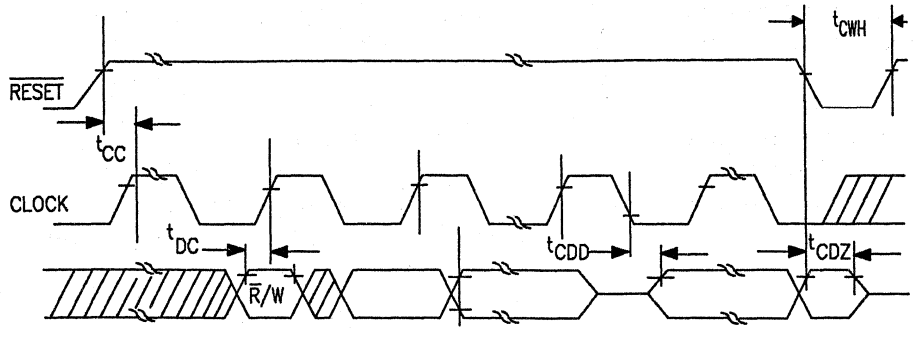
RESET PULSE Figure 17



WRITE DATA TIMING DIAGRAM Figure 18



READ DATA TIMING DIAGRAM Figure 19



level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds and a maximum of 120 microseconds in duration. There is a minimum of a 1 microsecond valid access recovery time between time slots.

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot (see Figure 13).

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot (see Figure 14).

READ TIME SLOTS

The host generates read time slots when data is to be read from the 1-wire interface. A read time slot is initiated when the host pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of one microsecond and a maximum of 15 microseconds. This maximum time of 15 microseconds includes the time required for the data line to pull up to a high level after it is released. The state of the 1-wire data line must be read by the host within 15 microseconds after the start of the read time slot. After this time, the state of the data is not guaranteed (see Figure 15). All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond valid access recovery time between individual read time slots.

1-WIRE PROTOCOL

The 1-wire protocol can be viewed as having three distinct layers. These layers are the Presence Detect layer, the Reset layer, and the Command layer.

PRESENCE DETECT

The presence detect layer is used to signal to a host device that a new device has been attached to the 1-wire port. The 1-wire port from the host remains at a logic high level during quiescent times between read and write time slots. This high time must be present for a minimum of 15 microseconds before the new device can assert a presence detect signal. The presence detect signal will be a logic low level asserted by the newly attached device which remains low for a maximum of 240 microseconds and is then released (see Figure 16). This low logic level can be detected by the host and used as an interrupt condition for the host processor.

DEVICE RESET

The Reset layer is used to reset the attached 1-wire devices. This allows the host to place the 1-wire device or devices into a known state at any time. The reset signal consists of a logic low level asserted by the host for a minimum of 480 microseconds. After this, the host must release the 1-wire signal line and allow it to rise to a logic high level. This high logic level must be maintained by the host for a minimum of 480 microseconds before any data can be exchanged. During this logic high time, any device present on the 1-wire signal line will assert its presence-detect waveform.

1-WIRE COMMANDS

There are four commands which can be issued by the host on the 1-wire port. These are:

1) [33 hex] read ROM data
2) [55 hex] match ROM data
3) [F0 hex] search ROM data
4) [CC hex] pass-through mode

READ ROM DATA

Upon recognition of the command word [33 hex], the DS1205 is ready to respond to the next eight read time slots with the Type Identifier number. This number is a hexadecimal 02 and is unique to the DS1205 part.

After receipt by the host of the Type Identifier number, the DS1205 is ready to output the unique 48-bit serial number contained within the device. The host must issue 48 read time slots to retrieve this number. Following the 48-bit serial number is an eight-bit Cyclic Redundancy Check (CRC) value. This CRC value has been calculated over the Type Identifier and Serial Number, 56 bits total, using the following polynomial:

$p_x = x^2 + x^3$, assuming x^0 => LSB

This calculated value is complemented and then lasered into the part at the time of manufacture. To read the CRC value, the host must issue eight additional read time slots.

MATCH ROM DATA

The Match ROM data command is used as a device select when multiple 1-wire devices are connected to a single bus. This command allows the host to address any one of the multiple 1-wire devices on an individual basis. To do a Match ROM data command, the host must issue the command [55 hexadecimal] to the device with eight write time slots. Following the command byte, the host must write the desired device's type identifier, serial number, and CRC byte. If all of these values match the data stored internally in the ROM, the DS1205 can now be accessed using the standard DS1205 commands and protocol. If any of the bit values transmitted by the host fail to match the ROM data pattern, the access will be terminated. To return from a pattern fail condition, the host must issue a Reset command:

| Type ID | 48 bit Serial Number | CRC |
transmit ---------->

SEARCH ROM DATA

The Search ROM data command allows the host 1-wire device to poll efficiently to determine the unique ROM address of all devices on the 1-wire bus. In this mode, each of the bits of the ROM data requires three time slots on the 1-wire bus. The first two time slots are read time slots in which the DS1205 transmits back to the host the value of the ROM bit followed by its complement. The third time slot is a write time slot in which the host supplies its desired value for the ROM bit. The DS1205 then compares the desired value with the actual ROM bit. If they disagree, the DS1205 will go to a high impedance state until a RESET is issued by the host. If the bits agree, the DS1205 increments its internal counter to point to the next bit in the ROM data and then repeats the same set of three time slots for the next bit. If all bits of the ROM are matched correctly, the host may access the DS1205 with the standard command structure for the part.

EXAMPLE OF A ROM SEARCH

The following example of the ROM search process assumes four different DS1205s are connected to the same 1-wire bus. The ROM data of the four DS1205s begins as shown:

ROM0- 00110101...
ROM1- 10101010...
ROM2- 11110101...
ROM4- 00010001...

The search process is as follows:

1) The host begins by resetting all devices present on the 1-wire bus. After this, the host will attempt to read the Type Identifier, Serial Number, and CRC value for the part.

2) The host will then issue the Search ROM Data command on the 1-wire bus.

3) The host executes two read time slots and receives two zero bits. This indicates that both one bits and zero bits exist as the first bit of the devices on the bus.

4) The host supplies a write zero time slot as the

third time slot. This deselects ROM1 and ROM2 for the remainder of this search pass, leaving only ROM0 and ROM3 connected to the 1-wire bus.

5) The host executes two read time slots and receives a zero bit followed by a one bit. This indicates that all devices still coupled to the 1-wire bus have zeros as their second ROM data bit.

6) The host supplies a write zero time slot as the third time slot to keep ROM0 and ROM3 coupled.

7) The host executes two read time slots and receives two zero bits. This indicates that both one bits and zero bits exist as the third bit of the ROM data of the attached devices.

8) The host supplies a write zero time slot as the third time slot. This deselects ROM0 leaving ROM3 as the only device connected.

9) The host reads the remainder of the ROM data bits for ROM3 and continues to access the part if desired. This completes the first ROM search pass and has identified one part uniquely on the 1-wire bus.

At this point, the host repeats the process described above to determine the addresses of the remaining devices on the 1-wire bus by repeating steps 1 through 7.

Note the following:

The host learns the unique address (ROM data pattern) of one 1-wire device on each ROM SEARCH operation. The time required to derive the part's unique address is:
960 us + 3 * (8 + 64) * 0.06ms = 13.92 milliseconds

The host is therefore capable of identifying 60 different 1-wire devices per second.

Additionally, the data obtained from the two read time slots of each set of three time slots have the following interpretations:

00 - There are still devices attached which have conflicting bits in this position.

01 - All devices still coupled have a zero bit in this bit position.

10 - All devices still coupled have a one bit in this bit position.

11 - There are no devices attached to the 1-wire bus (this is an error condition).

PASS-THRU MODE

The Pass-Thru command is used to allow a host connected to the 1-wire bus to gain access to the DS1205 directly. It can be used only when there is one DS1205 on the 1-wire bus. This command bypasses the serial number internal to the DS1205 and allows the host to directly control the DS1205 with the DS1205 commands and protocol.

3-WIRE BUS

The 3-wire bus is comprised of three signals. These are the RST\ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the RST\ input high. The RST\ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if the RST \ is low and the DQ pin goes to a high impedance state. When data transfers to the DS1205 are termi-

nated by the RST \ signal going low, the transition of the RST \ going low must occur during a high level of the CLK signal. Failure to ensure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figures 18 and 19 for normal modes of operation.

1-WIRE/3-WIRE ARBITRATION

The DS1205 can utilize both the 1-wire and the 3-wire busses simultaneously. Neither input bus has priority over the other. Instead, if both inputs are being used, the signal arriving first will take precedence. More simply, if the 1-wire interface becomes active before the 3-wire interface, all communications will take place on the 1-wire bus. The 3-wire bus will be ignored in this case. The same condition occurs for the 1-wire interface if the 3-wire interface becomes active first.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
RESET\ Logic 1		3.0			V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	uA	
Output Leakage	I_{LO}			+500	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
RST\ Input Resistance	Z_{RST}	10		40	K ohm	
D/Q Input Resistance	Z_{DQ}	10		40	K ohm	
CLK Input Resis.	Z_{CLK}	10		40	K ohm	
RST\ Current @ 3.0V	I_{RST}			2	uA	
Active Current	I_{CC1}			6	mA	5
Standby Current	I_{CC2}			2.5	mA	5

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CAPACITANCE

(t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4
CLK Low Time	t_{CL}	125			ns	2
CLK High Time	t_{CH}	125			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise & Fall	t_R,t_F			500	ns	2
RST\ to CLK Setup	t_{CC}	1			us	2
CLK to RST\ Hold	t_{CCH}	40			ns	2
RST\ Inactive Time	t_{CWH}	125			ns	2
RST to I/O High Z	t_{CDZ}			50	ns	2

NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.

AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(0°C to 70°C, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{TS}	60		120	uS	
Recovery Time	t_{REC}	1			uS	
Low Time	t_{LOW}	1		15	uS	
Reset Time High	t_{RSTH}	480			uS	
Reset Time Low	t_{LOW}	480			uS	
Presence Detect	t_{PDHIGH}	15		60	uS	
Presence Detect	t_{PDLOW}	60		240	uS	

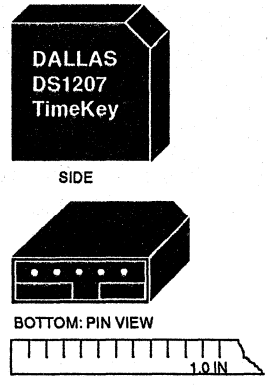
DALLAS SEMICONDUCTOR

DS1207
TimeKey

FEATURES

- Cannot be deciphered by reverse engineering
- Time allotment from one day to 512 days for trial periods, rentals, and leasing
- Partitioned memory thwarts pirating
- User-insertable packaging allows personal possession
- Exclusive blank keys on request
- Appropriate identification can be made with a 64-bit reprogrammable memory
- Unreadable 64-bit match code virtually prevents discovery by exhaustive search with over 10^{19} possibilities
- Random data generation on incorrect match codes obscures real accesses
- 384 bits of secure read/write memory creates additional barriers by permitting data changes as often as needed
- Rapid erasure of identification, security match code and secure read/write memory can occur if tampering is detected
- Durable and rugged
- Applications include software authorization, gray market software protection, proprietary data, financial transactions, secure personnel areas, and system access control

PIN DESCRIPTION



PIN NAMES (\ Denotes Condition Low)

Pin 1	NC	No connection
Pin 2	RST\	Reset
Pin 3	DQ	Data input/output
Pin 4	CLK	Clock
Pin 5	GND	Ground

DESCRIPTION

The DS1207 TimeKey is a miniature security system that stores 64 bits of user-definable identification code and a 64-bit security match code that protects 384 bits of read/write non-volatile memory. The 64-bit identification code and the security match code are programmed into the TimeKey via a special program mode operation. After programming, the TimeKey follows a procedure with a serial format to retrieve or update data. The Timekey is set to expire from one day to 512 days or infinity, as specified by the customer. The TimeKey starts its countdown from the first access by the end user.

Interface cost to a microprocessor is minimized by on-chip circuitry that permits data transfer with only three signals: Clock (CLK), Reset\ (RST\) and Data Input/Output (DQ). Low pin count and a guided entry for a mating receptacle overcome mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user-insertable.

OPERATION - NORMAL MODE

The TimeKey has two modes of operation: normal and program. The normal mode of operation provides the functions of reading and writing the 384-bit secure memory. The block diagram (Figure 1) illustrates the main elements of the TimeKey when used in the normal mode. To initiate data transfer with the TimeKey, RST\ is taken high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines normal operations with a function code of read or write. If one of these patterns is not matched, communications are ignored. If the command register is loaded properly, communications are allowed to continue. Data is clocked out of the TimeKey on the high-to-low transition of the clock. If the pattern matched in the command register calls for a normal read or write, the next 64 cycles following the command word are read and data is clocked out of the identification memory. The next 64 write cycles are written to the compare register (Figure 2). These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, if a normal read mode is selected, random garbled data is output for the next 384 cycles. If a normal write cycle is selected and a match is not achieved, the TimeKey will ignore any additional information. However, when a security match is achieved, access is permitted to write the 384-bit secure memory.

OPERATION - PROGRAM MODE

The program mode of operation provides the functions of programming the identification and security match memory, and setting and reading the amount of time the TimeKey can be used. The block diagram in Figure 3 illustrates the main elements of the TimeKey when used in the program mode. To initiate the program mode, RST\ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern that defines the program mode for the identification and security match bits or the program mode for setting and reading the amount of time for which the TimeKey can be used. If an exact match for one of the seven function codes of the program mode is not found, the remainder of the program mode is ignored. When the command register is properly loaded for programming the identification and security match bits, the next 128 bits are written to the identification and security match memory (Figure 4). When this mode of operation is invoked, all memory contents are erased.

SETTING AND READING TIME REMAINING

There are six functions of the program mode which are used to set or read the amount of time for which the TimeKey will allow full operation. To initiate any of the six functions of the program mode used for setting and reading time remaining, RST\ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. If the command register is properly loaded with the function code for reading the 20-bit day clock counter, the next 20 bits will be output (LSB first) as a binary count of the amount of time elapsed in the current day (see Figure 5). The time can be calculated by dividing this count reading by 2^{20} (20 bits is equal to 1,048,576 counts). One minus this result is the fraction of a day remaining. The 20-bit day clock counter is driven by an internal oscillator that has a period of 82.4 ms. If the command

register is properly loaded with the function code for reading the 9-bit number of days counter, the next 9 bits will be output (LSB first) as a binary count of the days remaining (see Figure 6). This count is decremented each time the day clock counter rolls over to zero. When the number of days remaining counter rolls through zero, normal and program mode write cycles are inhibited. If the program mode read cycle to the number of days counter is attempted, the nine bits will be returned as all ones.

If the command register is properly loaded with the function code for writing the 9-bit number of days counter, the next nine bits will be input (LSB first) as a binary count of the desired number of days in which the TimeKey will be fully functional (see Figure 7). The number of days counter can be changed by writing over an entered value as often as required until the lock command is entered. The lock command is given when the command register is properly loaded with the function code for locking up the number of days counter. The lock command consists of the 24-bit command word only (see Figure 8). Once the lock command is given, all future write cycles to the number of days register are ignored. After the correct value has been written and locked into the number of days counter, the DS1207 will start counting the time from the entered value to zero after the first access to the TimeKey is executed, provided the arm oscillator bit is set. The arm oscillator bit is set when the command register has been properly loaded with the function code for arming the oscillator. The arm oscillator command consists of the 24-bit command word only (see Figure 9). One other command is also available for use in setting and reading time remaining. A stop oscillator command is given when the command register is properly loaded with the function code for stopping the oscillator. The stop oscillator command consists of the 24-bit command word only (see Figure 10). This command will only execute prior to issuing a lock command. After the lock command is issued, stop oscillator commands are ignored.

A sequence for properly setting the expiration time of the DS1207 is as follows (see Figure 11). First, program the identification and security match bits to the desired value. Use normal mode operation to write the appropriate secure data. Second, write the number days remaining register to the desired value. This number can be immediately verified by reading the number of days remaining. Next, arm the oscillator by writing the appropriate command. Then do a normal mode read. This action will start the internal oscillator. Now read the 20-bit day clock counter several times to verify that the oscillator is running. After oscillator activity has been verified, issue the stop oscillator command. The lock command should be issued, followed by the arm oscillator command. The TimeKey will start the countdown to expiration on the next access. The oscillator verification portion of this sequence is not required and can be deleted when speed in setting time remaining is important.

COMMAND WORD

Each data transfer for normal and program mode begins with a 3-byte command word as shown in Figure 12. As defined, the first byte of the command word specifies the function code. Eight function codes are acceptable (Figure 13). If any one of the bits of the first byte of the command word fails to meet one of the exact patterns for function codes, the data transfer will be aborted.

The first two bits of the second byte of the command word specify whether the data transfer to follow is program or normal mode. The bit pattern for program mode is 0 in bit 0 and 1 in bit 1. The bit pattern for normal mode is a 1 in bit 0 and a 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause the transfer to abort. The program mode can be invoked with one of seven function codes: program identification and security match, read the 20-bit day clock counter, read the number of days count, write the number of days count, lock number of days count, arm oscillator, and stop oscillator.

The remaining six bits of byte 2 and the first four bits of byte 3 must be written to match one of the five patterns as indicated in Figure 12 or data transfer will abort. Under special contract with Dallas Semiconductor, these bits can be defined by the user as any bit pattern other than those specified as unavailable. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last four bits of byte 3 of the command word must be written 1011 or data transfer will abort. Table 1 provides a summary of the command words in hexadecimal as they apply to all function codes for both program mode and normal mode.

Note: Contact the Dallas Semiconductor sales office for special command word code assignment that makes possible an exclusive blank TimeKey.

RESET AND CLOCK CONTROL

All data transfers are initiated by driving the RST\ input high. The reset input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the RST\ signal provides a power source for the cycle to follow. To meet this requirement, a drive source for RST\ of 2 mA at 3.5 volts is required. Third, the RST\ signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of the clock cycle. Command bits and data bits are input on the rising edge of the clock. Data bits are output on the falling edge of the clock. The rising edge of the clock returns the DQ pin to a high impedance state. All data transfer terminates if the RST\ pin is low and the DQ pin goes to a high impedance state. Data transfer is illustrated in Figure 14 for normal mode and Figure 15 for program mode.

TIMEKEY CONNECTIONS

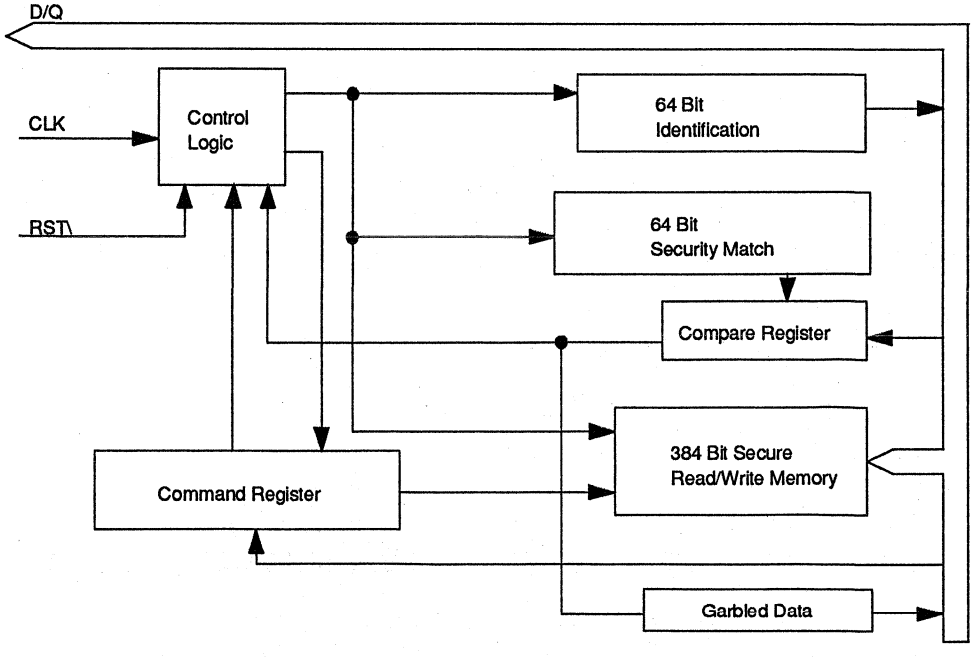
The TimeKey is designed to be plugged into a standard 5-pin 0.1 inch center SIP receptacle. A guide is provided to prevent the TimeKey from being plugged in backwards and aid in alignment of the receptacle. For portable applications, contact to the TimeKey pins can be determined to ensure connection integrity before data transfer begins. CLK, RST\, and DQ all have 20K ohm pulldown resistors to ground that can be sensed by a reading device.

COMMAND WORDS Table 1

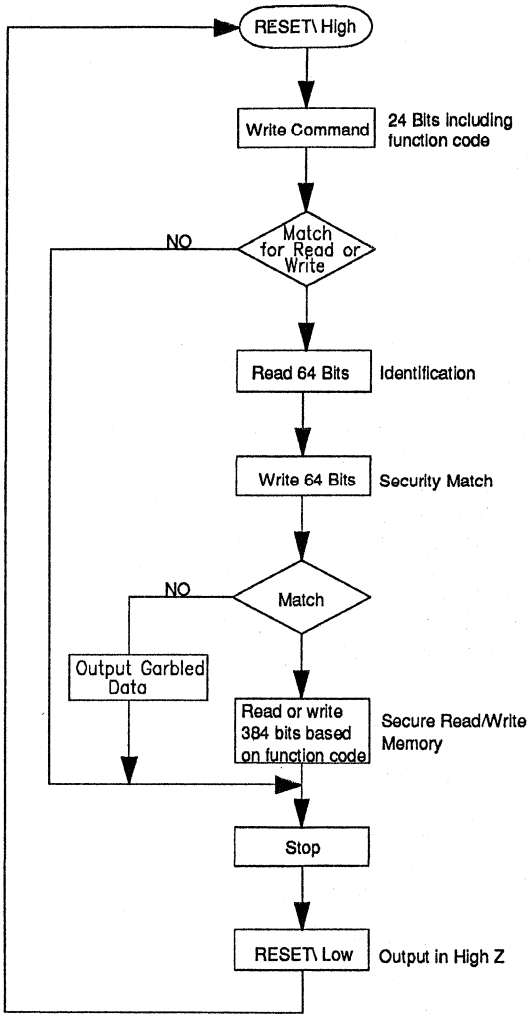
Summary of the command words in hexidecimal as they apply to all function codes for both program mode and normal mode for the DS1207-1 only.(See Figures 12 and 13 for detailed command words.)

MODE	FUNCTION	COMMAND WORDS MSB		LSB
NORMAL	READ	B0	01	62
NORMAL	WRITE	B0	01	9D
PROGRAM	WRITE	B0	02	9D
PROGRAM	READ DAY CLOCK COUNTER	B0	02	F1
PROGRAM	READ DAYS REMAINING	B0	02	F3
PROGRAM	WRITE DAYS REMAINING	B0	02	F2
PROGRAM	ARM OSCILLATOR	B0	02	F5
PROGRAM	LOCK NUMBER OF DAYS COUNT	B0	02	F6
PROGRAM	STOP OSCILLATOR	B0	02	F4

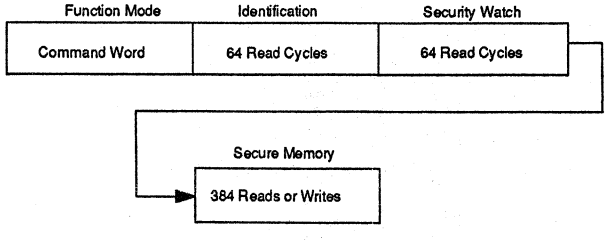
BLOCK DIAGRAM: NORMAL MODE Figure 1



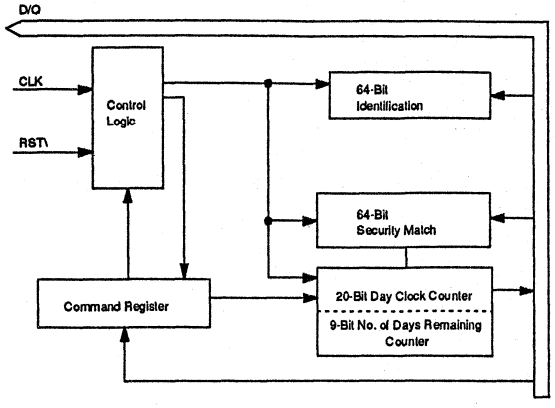
NORMAL MODE: READ OR WRITE SECURE READ/WRITE MEMORY Figure 2A



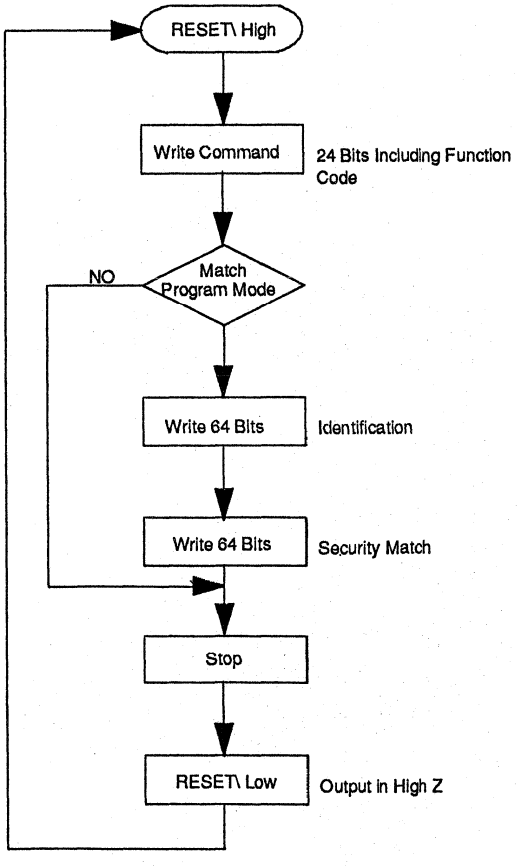
SEQUENCE: NORMAL MODE, READ OR WRITE SECURE MEMORY Figure 2B



BLOCK DIAGRAM: PROGRAM MODE Figure 3



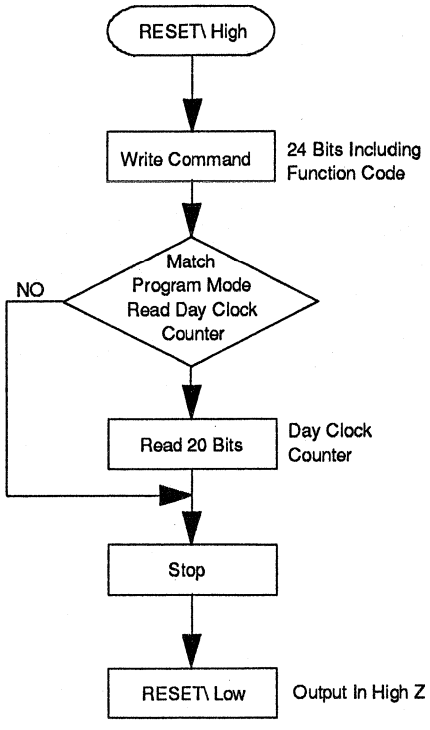
PROGRAM MODE: PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 4A



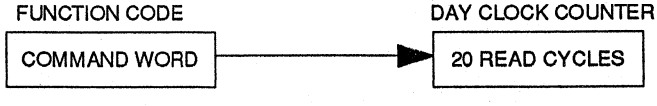
SEQUENCE: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH BITS Figure 4B

Function Mode	Identification	Security Watch
Command Word	64 Write Cycles	64 Write Cycles

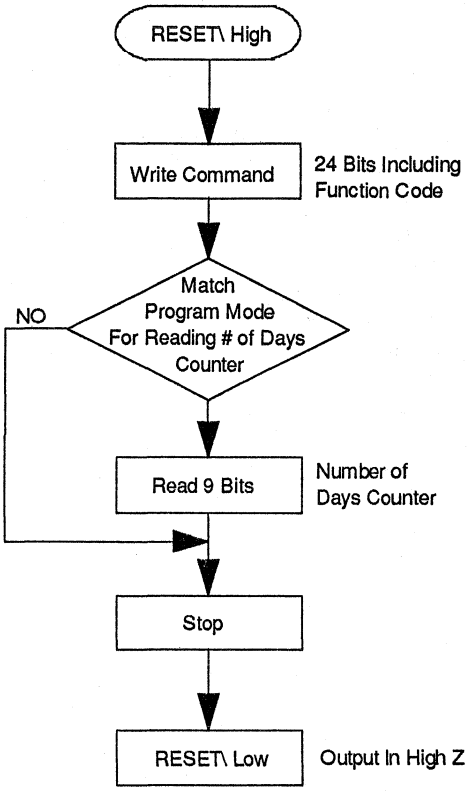
FLOW CHART: PROGRAM MODE, READING THE 20-BIT DAY CLOCK CALENDAR Figure 5A



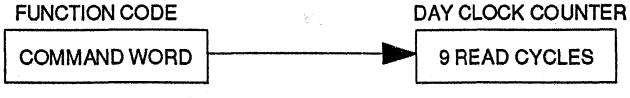
SEQUENCE: PROGRAM MODE, READING THE 20-BIT DAY CLOCK COUNTER Figure 5B



FLOW CHART: PROGRAM, READING THE 9-BIT NUMBER OF DAYS COUNTER
Figure 6A

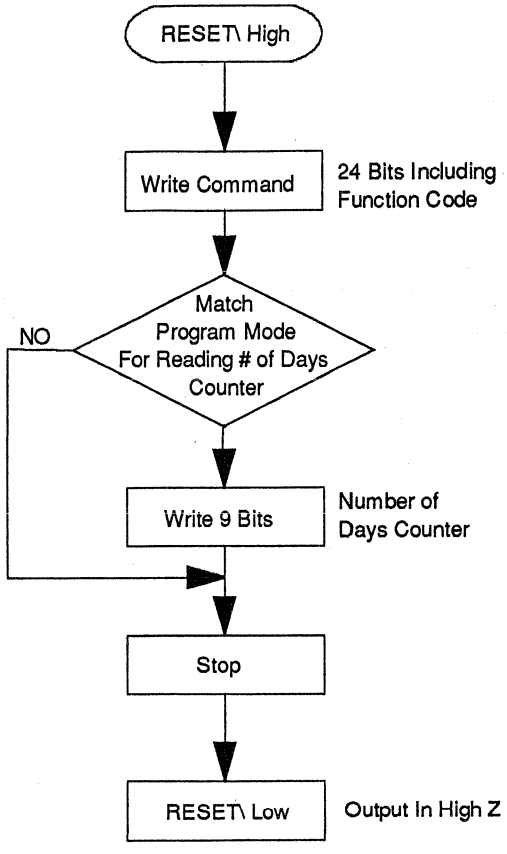


SEQUENCE: PROGRAM MODE, READING THE 9-BIT NUMBER OF DAYS COUNTER Figure 6B



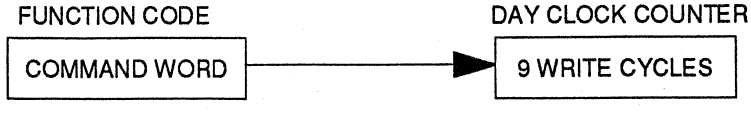
FLOW CHART: PROGRAM MODE, WRITING TO NUMBER OF DAYS COUNTER

Figure 7A

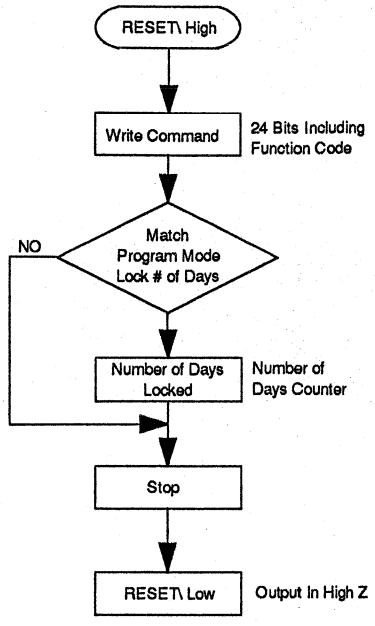


SEQUENCE: PROGRAM MODE, WRITING THE NUMBER OF DAYS COUNTER

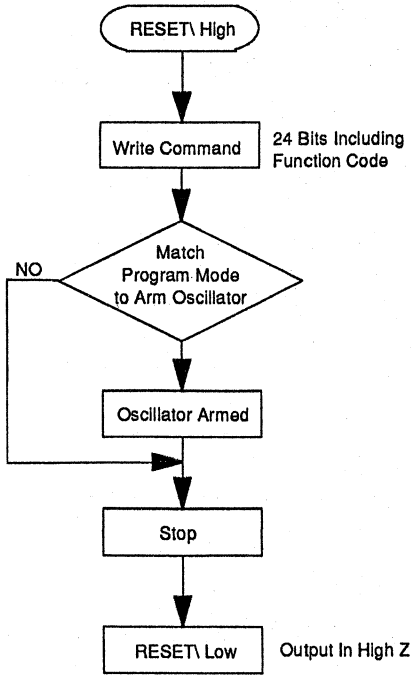
Figure 7B



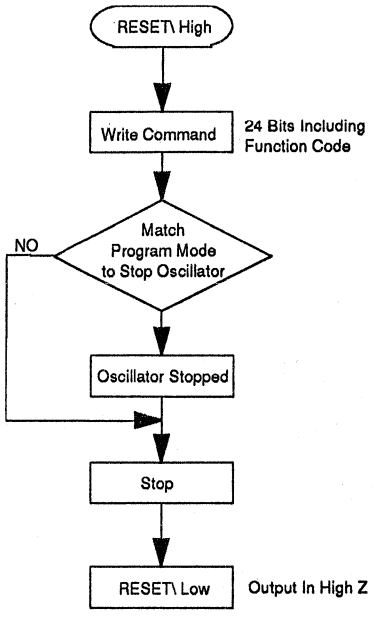
FLOW CHART: PROGRAM MODE, LOCK NUMBER OF DAYS REGISTER
Figure 8



FLOW CHART: PROGRAM MODE, ARM OSCILLATOR Figure 9



FLOW CHART: PROGRAM MODE, STOP OSCILLATOR Figure 10

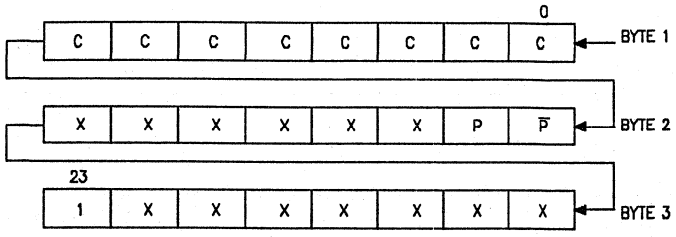


SETTING THE TIME UNTIL EXPIRATION OF THE DS1207 Figure 11

Step 1	Program identification memory Program security match bits Write normal mode secure data
Step 2	Program write the number of days remaining Program read the number of days remaining for verification
Step 3*	Issue arm oscillator command
Step 4*	Do a read of any kind
Step 5*	Program read the day clock counter several times (verify that the oscillator is running)
Step 6*	Issue the stop oscillator command
Step 7	Issue the lock command
Step 8	Issue the arm oscillator command (time of expiration will start on first access)

*Steps 3 through 6 are not required. Dallas Semiconductor tests and guarantees that the oscillator will start without verification.

COMMAND WORD Figure 12

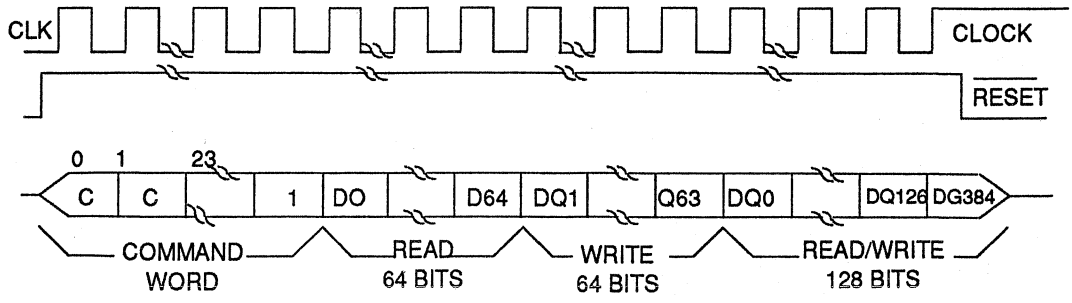


DS1207-1	0	0	0	0	0	0	P	P̄	BYTE 2
	1	0	1	1	0	0	0	0	BYTE 3
DS1207-2	0	0	0	0	0	1	P	P̄	BYTE 2
	1	0	1	1	0	0	0	0	BYTE 3
DS1207-3	0	0	0	0	1	0	P	P̄	BYTE 2
	1	0	1	1	0	0	0	0	BYTE 3
DS1207-4	0	0	0	0	1	1	P	P̄	BYTE 2
	1	0	1	1	0	0	0	0	BYTE 3
DS1207-5	0	0	0	1	0	0	P	P̄	BYTE 2
	1	0	1	1	0	0	0	0	BYTE 3

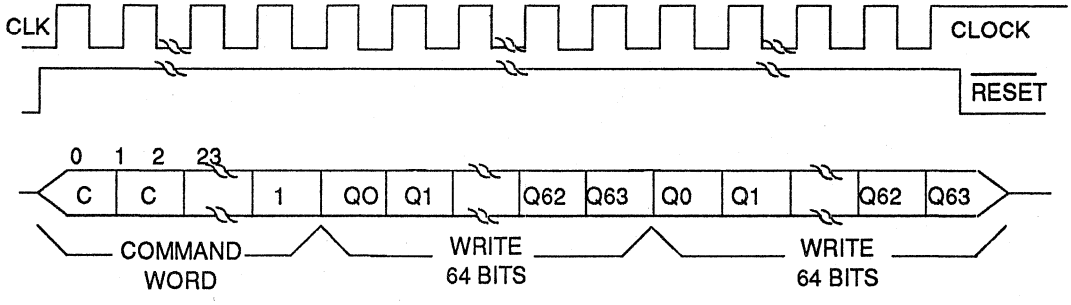
FUNCTION CODES: FIRST BYTE OF COMMAND WORD Figure 13

MSB							LSB	
0	1	1	0	0	0	1	0	READ
1	0	0	1	1	1	0	1	WRITE
1	1	1	1	0	0	0	1	READ DAY CLOCK COUNTER
1	1	1	1	0	0	1	0	WRITE NUMBER OF DAYS REMAINING
1	1	1	1	0	0	1	1	READ NUMBER OF DAYS REMAINING
1	1	1	1	0	1	0	0	STOP OSCILLATOR
1	1	1	1	0	1	0	1	ARM OSCILLATOR
1	1	1	1	0	1	1	0	LOCK NUMBER OF DAYS COUNT

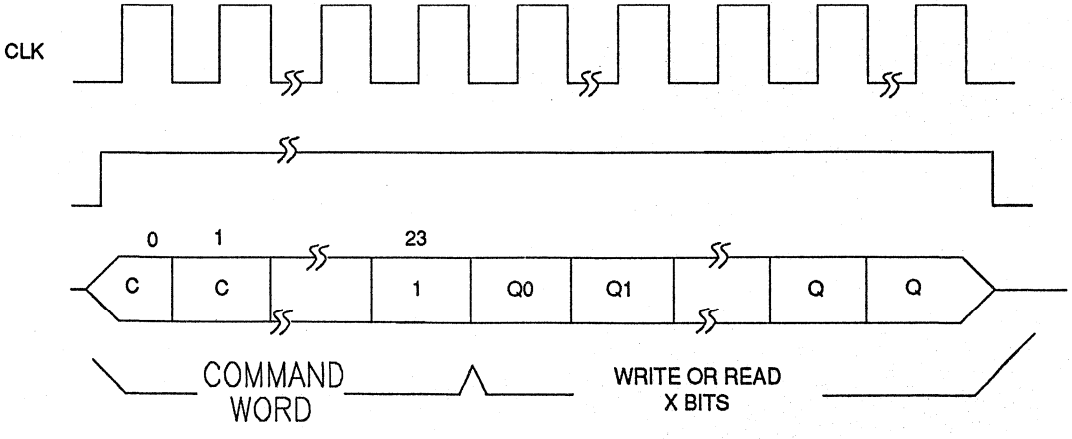
DATA TRANSFER: NORMAL MODE, READ OR WRITE SECURE READ/WRITE MEMORY Figure 14



DATA TRANSFER: PROGRAM MODE, PROGRAM IDENTIFICATION AND SECURITY MATCH MEMORY Figure 15A



DATA TRANSFER: PROGRAM MODE, DAY CLOCK, DAYS REMAINING AND OSCILLATOR CONTROL Figure 15B



NOTE: The number of bits which follow the command word will be either 0, 9, or 20 bits based on the function code.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
RESET\ Logic 1	V_{IHE}	3.5			V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; RST\ = 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	u A	4
Output Leakage	I_{LO}			+500	u A	
Output Current @2.4V	I_{OH}	-1			mA	
Output Current @0.4V	I_{OL}			+2	mA	
RST\ Input Resistance	Z_{RST}	10		60	K ohms	
D/Q Input Resistance	Z_{DQ}	10		60	K ohms	
CLK Input Resistance	Z_{CLK}	10		60	K ohms	
RST\ Current @3.5V	I_{RST}			2	mA	6, 9

CAPACITANCE (t_A=25°C)

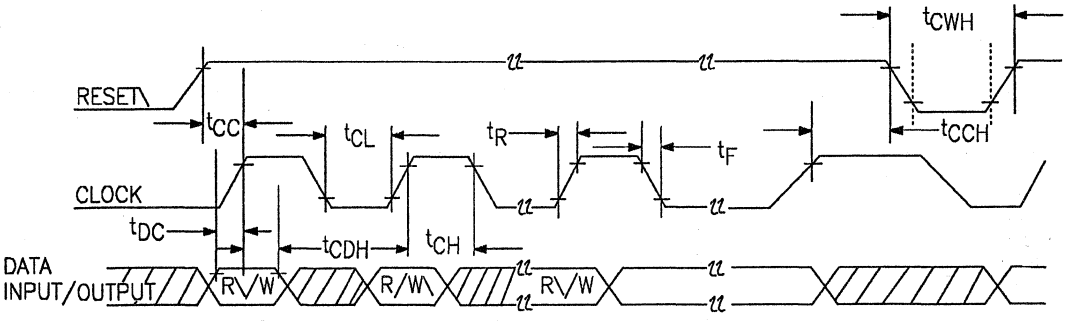
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

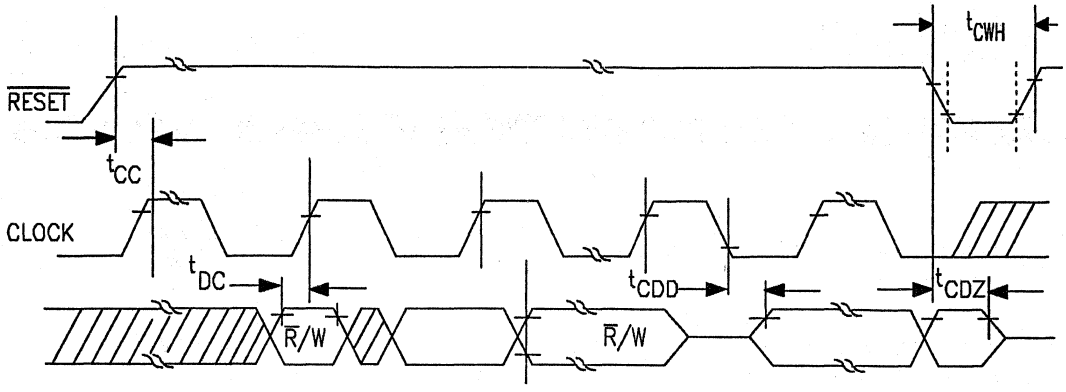
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data To CLK Setup	t_{DC}	50			ns	2, 7
CLK to Data Hold	t_{CDH}	70			ns	2, 7
CLK to Data Delay	t_{CDD}			200	ns	2, 3, 5, 7
CLK Low Time	t_{CL}	250			ns	2, 7
CLK High Time	t_{CH}	250			ns	2, 7
CLK Frequency	f_{CLK}	DC		2.0	MHz	2, 7
CLK Rise & Fall	t_R, t_F			500	ns	2, 7
RST\ to CLK Setup	t_{CC}	1			us	2, 7
CLK to RST\ Hold	t_{CCH}	60			ns	2, 7
RST\ Inactive Time	t_{CWH}	10			ms	2, 7,
RST\ To I/O High Z	t_{CDZ}			70	ns	2, 7

TIMING DIAGRAM - WRITE DATA



TIMING DIAGRAM: READ DATA



NOTES:

1. All voltages are referenced to GND.

2. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.

3. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.

4. For CLK, D/Q, and RST\.

5. Load capacitance = 50 pF.

6. Measured with outputs open.

7. Measured at V_{IH} of RST\ greater than or equal to 3.5 volts.

8. Each DS1207 is marked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.

9. Average AC RST\ current can be determined using the following formula:

$I_{TOTAL} = 2 + I_{LOAD}$ DC + $(4 \times 10^{-3})(C_L + 280)^f$
I_{TOTAL} and I_{LOAD} are in mA; CL is in pF; f is in MHz.

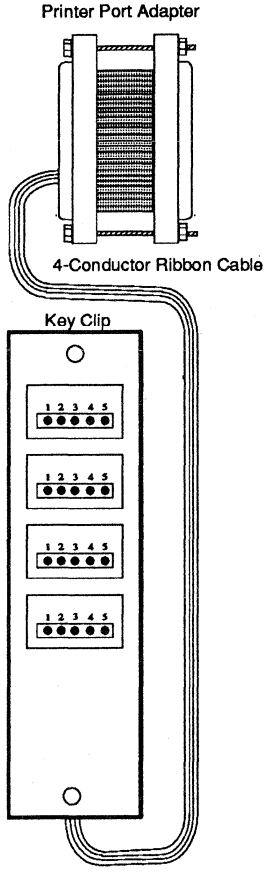
Applying the above formula, a load capacitance of 50 pF
running at a frequency of 2.0 MHz gives an I_{TOTAL} of 1.6 mA.

DALLAS SEMICONDUCTOR

DS1253
Printer Port KeyRing

FEATURES

- Low-cost add-on fixture for Electronic Keys, Tags, and TimeKeys
- Connects directly to IBM PC parallel printer port without affecting printer operation
- Plug-in installation
- Key, Tag, and TimeKey communications are totally controlled by software
- Up to four Keys, Tags, and TimeKeys can be resident at one time
- Normal computer operation is unaffected
- Applications include software security, identification, personalization, and portable memory



PIN NAMES (\ Denotes Condition Low)

Pin 1	V_{CC}	+5 Volts
Pin 2	RST\	RESET\
Pin 3	D/Q	DataIn/Out
Pin 4	CLK	CLOCK
Pin 5	GND	Ground

DESCRIPTION

The DS1253 Printer Port KeyRing adapts low pin count Electronic Keys (DS1204U), Tags (DS1201), and TimeKeys (DS1207) to the IBM PC parallel printer port without affecting the printer or computer operation. The KeyRing is installed onto any IBM PC or PC-compatible printer by simply disconnecting the printer, installing the printer port adapter, and reconnecting the printer to the connector on the printer port adapter. The emanating 4-conductor ribbon cable can be routed such that the key clip can be attached to the computer cabinet in a convenient location with the adhesive provided. Up to 4 keys and/or tags can be inserted into the key clip at the same time. Communications with keys and tags occur under software control of the parallel printer port. The three control signals (Reset\, Clock, and Data In/Out) for Tags, Keys, and TimeKeys are generated by consecutive I/O instructions which control the parallel printer port.

OPERATION

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals RST\, CLK, and DQ must be software controlled to duplicate the behavior as defined in the respective data sheet for Tags, Keys, and TimeKeys. Each signal is a function of a specific output or I/O line of the printer port. Pin 4 on the 25-Pin D connector of a specific output or I/O line of the printer port is called Data Out 2 (D2). This signal is used to provide RST\ for the KeyRing and must be kept at a high level when communicating with Tags, Keys, and TimeKeys. When RST\ is driven low, all communication to Tags, Keys, and TimeKeys is terminated. Pin 5 on the 25-Pin D connector parallel printer port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of Keys, Tags, and TimeKeys. Because the CLK signal provides timing, the relationship between both level and transition from one level to another is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to Keys, Tags, and TimeKeys, and a CLK transition is also required to output data. Because signals change state at the same time on the parallel printer port, setup and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will then guarantee that data is valid as the clock changes levels. Pin 17 on the 25 Pin D connector parallel printer port is called SLCTIN and is used as the data I/O signal for Keys, Tags, and TimeKeys. This is a bidirectional signal. Data is output from this port signal during write cycles, and input from Keys, Tags, and TimeKeys during read cycles. Pin 18 on the 25-Pin D connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, Tags, and TimeKeys, the parallel printer port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret Key, Tag, and TimeKey communications as print commands, the strobe signal (Pin 1 on the D connecter parallel printer port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the parallel printer port signals.

INSTALLATION

The parallel printer port KeyRing is installed by first removing the printer cable. If the parallel printer port is not used, this step is not necessary. The parallel printer port cable is removed by loosening the top and bottom mounting screws and unplugging the cable. Loosen the top and bottom mounting screws on the adapter and plug the male side of the adapter into the female printer port. The top and bottom screws should then be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the KeyRing. The top and bottom retaining screws should then be tightened to avoid accidental disconnection. After the printer port adapter has been secured, the key clip can be attached to a convenient spot on the computer cabinet with the supplied adhesive.

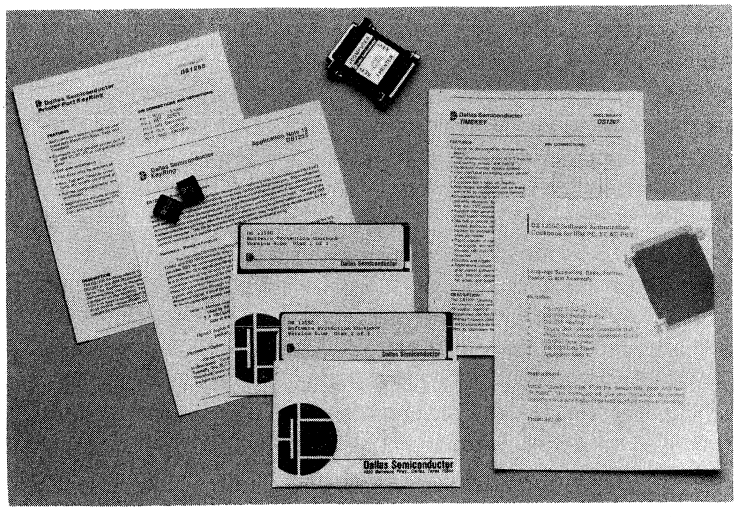
SOFTWARE

Dallas Semiconductor has demonstration software with source listing for assembly language and high level language for the IBM PC, XT, AT, or compatible computers. See the DS1255C Software Authorization Cookbook for details.

DALLAS SEMICONDUCTOR

DS1255C
Software Authorization Cookbook

INCLUDES
- DS1207 TimeKey
- DS1204U Electronic Key
- DS1255U Printer Port KeyRing
- Floppy Disk Labeled "Cookbook Disk 1"
- Floppy Disk Labeled "Cookbook Disk 2"
- DS1207 Data Sheet
- DS1204U Data Sheet
- DS1255U Data Sheet



DESCRIPTION
The DS1255C Software Authorization Cookbook serves as a cookbook for software protection. It provides step-by-step instructions for installing and testing the DS1204U Electronic Key and for modifying software so that it can be executed only when a correctly programmed electronic key is inserted in the DS1255Y Printer Port KeyRing.

The Dallas Semiconductor DS1204U Electronic Key provides an effective means to avoid the loss of revenue resulting from unauthorized duplication of software. The DS1207 TimeKey extends the capabilities of the Electronic Key by providing a continuously running timer which allows protected software to be used for a predetermined period of time up to 512 days.

Two Cookbook diskettes provide a simple set of instructions and examples that demonstrate how easily the Electronic Key and KeyRing interface can be integrated into an existing program written in one of the following popular high-level languages: C, Pascal, Fortran, Turbo Basic (Borland), and Basica (interpreter). This kit also provides a model assembly language subroutine for communicating directly with the key from an assembly language or high-level language program.

INSTRUCTIONS
Install "Cookbook Disk 1" in the default drive and type "RUN ME". This command will give instructions for printing document files which should be read carefully before proceeding.

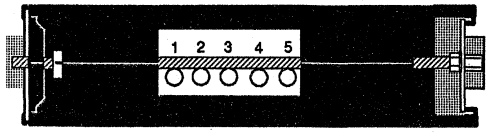
DALLAS SEMICONDUCTOR

DS1255U
Printer Port KeyRing

FEATURES

- Self-contained add-on fixture for user-insertable Electronic Keys, Tags, and TimeKeys
- Connects to the parallel printer port of an IBM XT, AT, RT, or compatible computer
- End user installation
- Machine screw SIPS ensure connection to DS1204U key pins
- Two keys may be resident at one time
- Transient suppression circuits protect against electrostatic discharge or accidental connection to serial port
- Key, Tag, and TimeKey communications are totally controlled by software
- Normal computer/printer operation is unaffected
- Applications include software authorization, computer site identification, and access control

PACKAGE DESCRIPTION



PIN NAMES(\ Denotes Condition Low)

Pin 1	V_{CC}	+5 Volts
Pin 2	RST\	RESET \
Pin 3	D/Q	Data In/Out
Pin 4	CLK	CLOCK
Pin 5	GND	GROUND

DESCRIPTION

The DS1255U Printer Port KeyRing adapts low-pin Electronic Keys (DS1204U), Tags (DS1201S), and TimeKeys (DS1207) to the IBM PC parallel printer port without affecting the printer or computer operations. The KeyRing is installed onto any IBM PC or IBM PC-compatible printer by simply disconnecting the printer, installing the KeyRing, and reconnecting the printer to the back connector on the KeyRing. Two Keys or Tags can be resident at the same time. Communication with Keys is established by software-controlled sequences to the parallel printer port. The three control signals (Reset\, Clock, and Data In/Out) for Keys are generated by the parallel port.

OPERATION

Keys, Tags, and TimeKeys have defined signal patterns which are required for communications. The signals RST\, CLK, and D/Q must be software-controlled to duplicate the behavior as defined in the respective data sheet for keys. Each signal is a function of a specific output or I/O line of the printer port (Figure 1). Pin 4 on the 25-pin D Connector parallel printer port is called Data Out 2 (D2). This signal is used to provide RST\ for the KeyRing and must be kept at high level when communicating with keys. When RST\ is driven low, all communication to keys is terminated. The RST\ signal is also used as a source of power for keys (see respective data sheets).

Pin 5 on the 25-pin D Connector parallel printer port is called Data Out 3 (D3). This signal is used to provide CLK for the KeyRing. The CLK signal times data into and out of keys. Because the CLK signal provides timing, the relationship between both level and transition is critical with respect to data. In fact, data must be valid when a CLK transition occurs which inputs data to keys, and a CLK transition is also required to output data. Because signals change state at the same time on the parallel printer port, setup and hold times do not normally exist. To compensate, two output cycles are required for each transition of the CLK signal. The first cycle is used to establish the correct CLK level. A second cycle will guarantee that data is valid as the CLK changes level.

Pin 17 on the 25-pin D connector parallel printer port is called SLCTIN\ and is used as the data I/O signal for keys. This is a bidirectional signal. Data is output from this port signal during write cycles and input from keys during read cycles. In addition, Pin 12 on the 25-pin D connector parallel printer port is called PAPER EMPTY and can be used to read data from the keys. This would be required for non-compatible printer ports, with Pin 17 as an output only. Pin 18 on the 25-pin D connector is ground (GND) and supplies ground for the KeyRing.

When communicating with Keys, the parallel printer port is being used as a general purpose I/O port. As such, software defines the appropriate commands. In order to avoid having the printer interpret key communications as printer commands, the strobe signal (Pin 1 on the 25-pin D connector parallel printer port) must be kept low when the data stream is not directed to the printer. The printer must also be kept on when using the KeyRing to avoid clamping the parallel printer port signals.

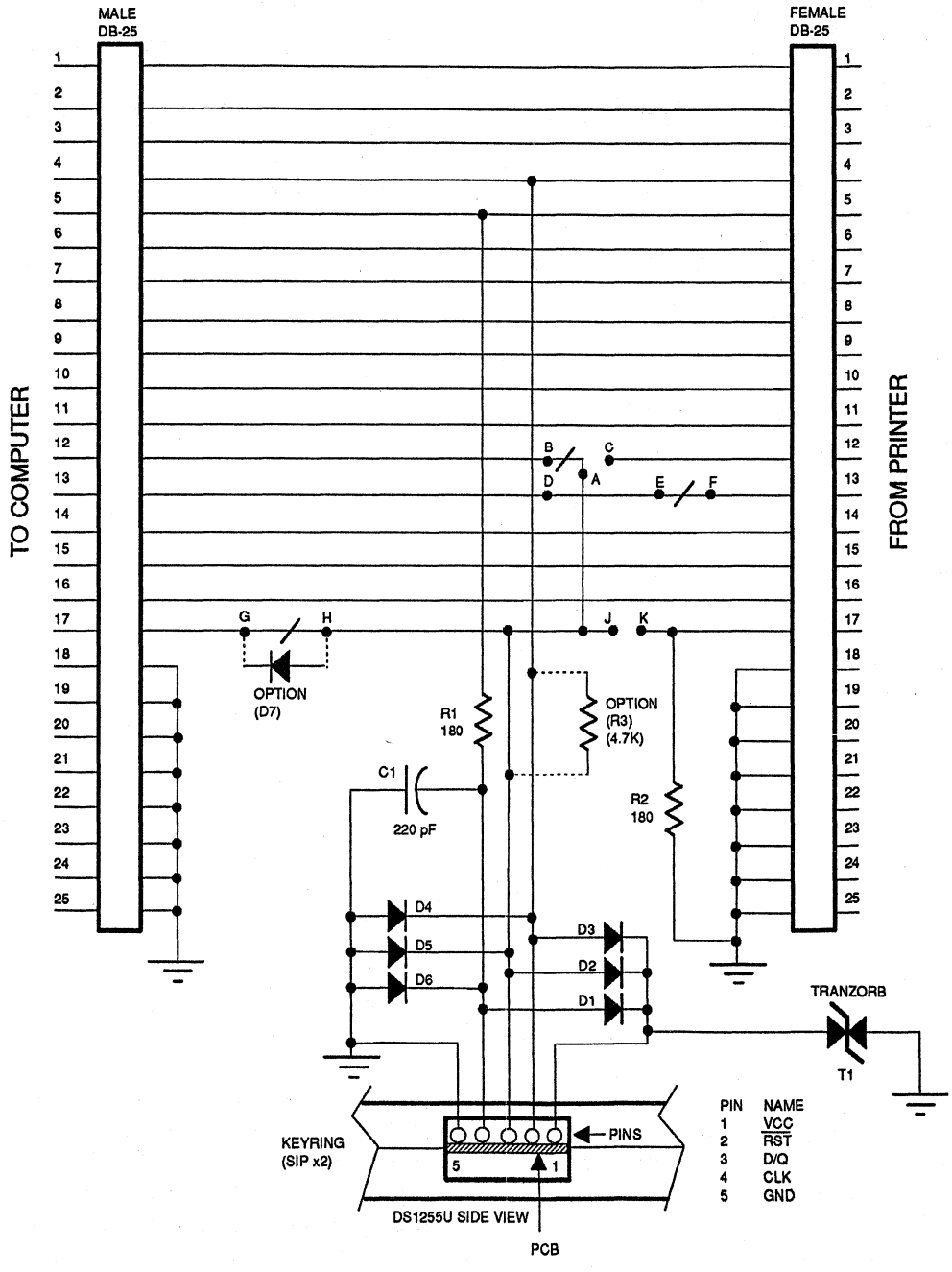
INSTALLATION

The parallel Printer Port KeyRing is installed by first removing the printer cable. If the parallel printer port is not being used, this step is not necessary. The printer cable is removed by loosening the top and bottom retaining screws and unplugging the cable. The next step is to install the KeyRing by plugging the male side of the KeyRing into the female printer port. The top and bottom retaining screws should be tightened to avoid accidental disconnection. Next, plug the printer cable into the female end of the KeyRing. The top and bottom retaining screws should then be tightened to avoid accidental disconnection. After the printer cable is secure, a Key, Tag, or TimeKey can be plugged into either of two receptacles and the computer and KeyRing are now ready for use.

SOFTWARE

Dallas Semiconductor has demonstration software with source listing for assembly language and high level language for the IBM PC, XT, AT, or compatible computers. See the DS1255C Software Authorization Cookbook for details.

DS1255U BLOCK DIAGRAM Figure 1



NOTE: An options list is available from Dallas Semiconductor which allows operation with some non-standard IBM PC printer ports.

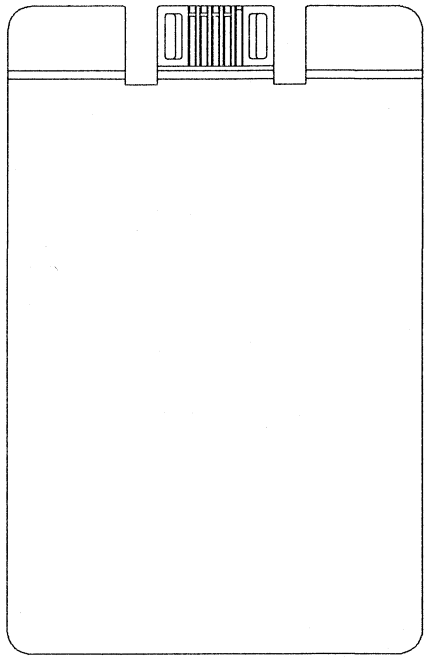
DALLAS SEMICONDUCTOR

DS6450/DS6450DES
CyberCard EV/DES

FEATURES

- Microprocessor, 32K byte NV RAM memory, and real-time clock in a credit card form factor
- Program downloading via 3-wire interface (DQ, CLK, and RST/)
- Completely crashproof: program/data RAM and all data registers are maintained in absence of power
- Program and data memory secure with a tamper-proof encrypter
- Compatible with industry-standard 8051 instruction set
- Optional DES encrypt/decrypt algorithms preprogrammed
- Greater than 50,000 cycle connector life
- Ground pin makes first and breaks last
- Durable and rugged

PIN DESCRIPTION



PIN NAMES

1	Ground
2	Clock
3	Data
4	RST\
5	V_{CC}

DESCRIPTION

The DS6450 CyberCard EV is a microprocessor, 32K bytes of nonvolatile static RAM, and a real-time clock all contained within a thick credit card sized-package. User-written programs can be downloaded into the DS6450 via the 3-wire serial interface (DQ, CLK, and RST/). As a result of sophisticated crashproofing circuitry, processing of a task can resume after power is reapplied to the DS6450. A built-in encrypter prevents unauthorized access to the resident application software. The DS6450DES is available with DES encryption/decryption algorithims already programmed into the device at the factory. For further technical information please see the DS5000T Time Microcontroller data sheet.

Integrated Battery Backup

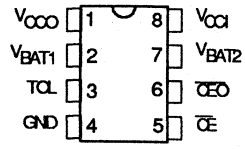
DALLAS SEMICONDUCTOR

DS1210
Nonvolatile Controller Chip

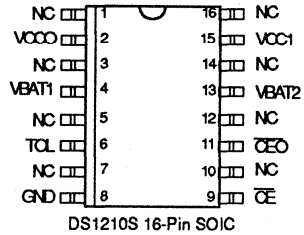
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1210 8-Pin DIP
(300 Mil.)



DS1210S 16-Pin SOIC
(300 Mil.)

PIN NAMES (\ Denotes Condition Low)

VCCO	RAM Supply
VBAT1	+ Battery 1
TOL	Power Supply Tolerance
GND	Ground
CE\	Chip Enable Input
CEO\	Chip Enable Output
VBAT2	+ Battery 2
VCCI	+ Supply
NC	No Connect

DESCRIPTION

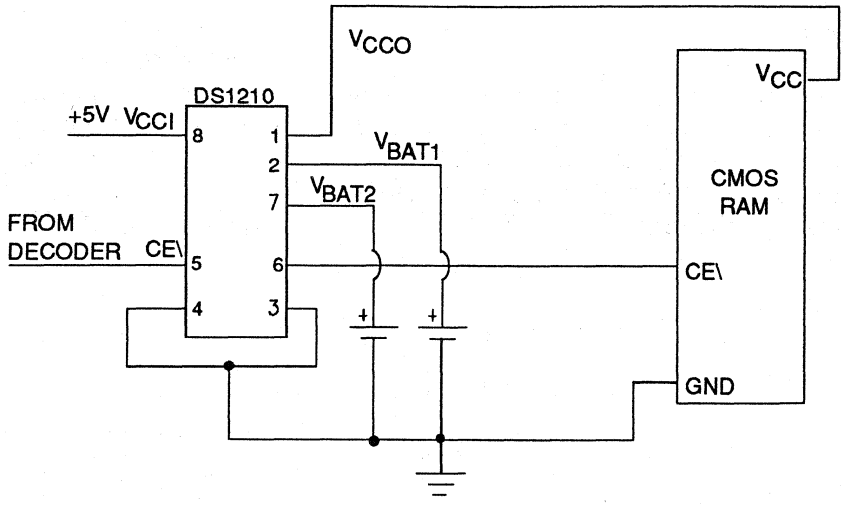
The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out- of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable (CEO\). The third function of write protection is accomplished by holding the CEO\ output signal to within 0.2 volts of the V_{CCI} or battery supply. If CE\ input is low at the time power fail detection occurs, the CEO\ output is kept in its present state until CE\ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions CEO\ will follow CE\ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V_{BAT2} pin will not activate a battery fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery back-up. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the CEO\ and V_{CCO} will be forced to V_{OL}. When the batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not provide battery back-up until V_{CCI} exceeds V_{CCTP}, as set by the T_{OL} pin, and then falls below V_{BAT}.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power-up to prevent spurious writes.

SECTION A - BATTERY BACKUP Figure 1

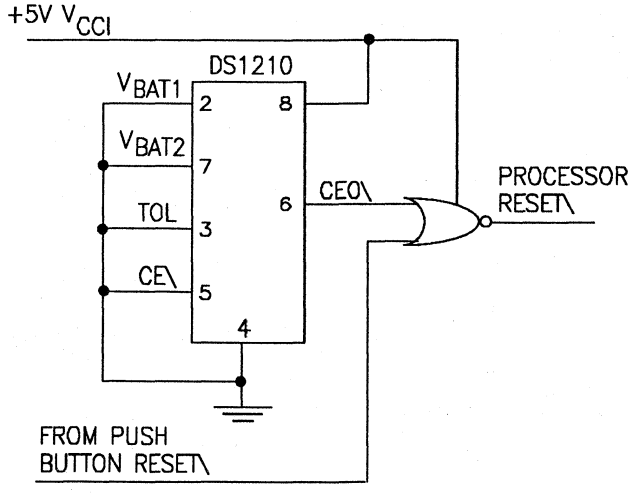


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	100 nA
RAM I_{CC02}	10 uA
Total Drain	10.1 uA

SECTION B - PROCESOR RESET



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)

DC ELECTRICAL CHARACTERISTICS

(V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
CEO\ Output @2.4V	I_{OH}	-1.0			mA	5
CEO\ Output @0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C, V_{CCI} = < V_{BAT})

CEO\ Output	V_{OHL}	V_{BAT} - 0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2,3
Battery Backup Current @ V_{cco} = V_{BAT} - 0.3V	I_{CCO2}			50	uA	6,7

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CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)
(V_{CCI} = 4.5 to 5.5V, Pin3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE\ Propagation Delay	t_{PD}	5	10	20	ns	5
CE\ High to Power Fail	t_{PF}			0	ns	

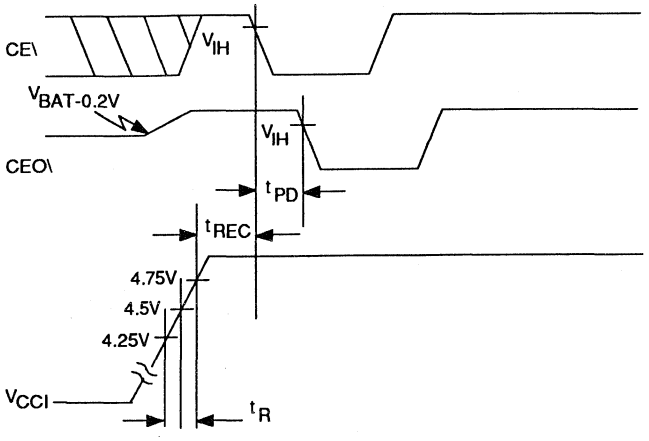
(0°C to 70°C, V_{CCI} <4.75V , Pin 3 = GND)
(V_{CCI} < 4.5 , Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7,8

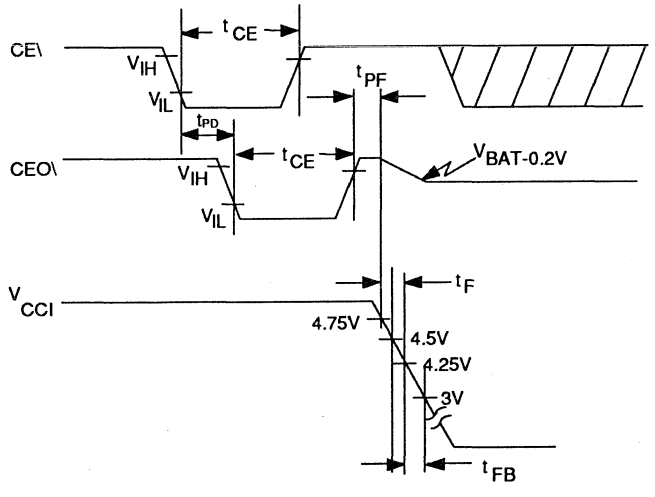
NOTES

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and CEO\ open.
4. I_{CC01} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CC02} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. CEO\ can only sustain leakage current in the battery backup mode.

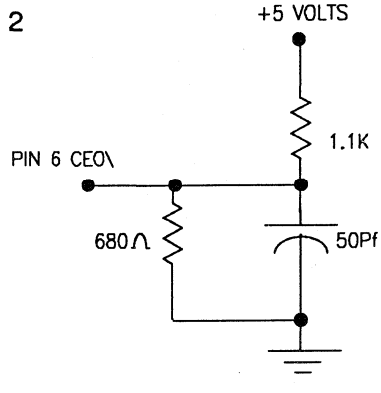
TIMING DIAGRAM - POWER UP



TIMING DIAGRAM - POWER DOWN



OUTPUT LOAD Figure 2



DALLAS SEMICONDUCTOR

DS1211
Nonvolatile Controller x 8 Chip

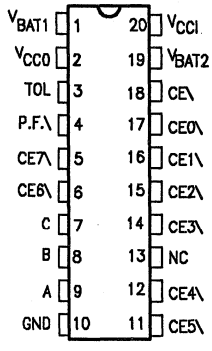
FEATURES

- Converts full CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 3 to 8 decoder provides control for up to eight CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 20-pin SOIC surface mount package

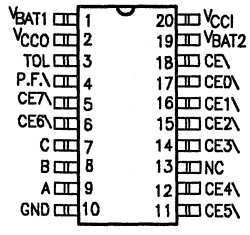
ORDERING INFORMATION:

DS1211	20-Pin DIP
DS1211S	20-Pin SOIC

PIN DESCRIPTION



20-PIN DIP (300 MIL)



20-PIN SOIC (300 MIL)

PIN NAMES (\ Denotes Condition Low)

A, B, C	Address Inputs
CE\	Chip Enable Input
CE0\ - CE7\	Chip Enable Outputs
GND	Ground
V_{BAT1}	+ Battery 1
V_{BAT2}	+ Battery 2
TOL	Power Supply Tolerance
V_{CCI}	+ 5V Supply
V_{CCO}	RAM Supply
P.F.\	Power Fail
N.C.	No Connection

DESCRIPTION

The DS1211 Nonvolatile Controller x 8 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption.

By combining the DS1211 nonvolatile controller/decoder chip and lithium batteries ten years of nonvolatile RAM operation can be achieved for up to eight CMOS memories.

See the data sheet for the DS1212 Nonvolatile Controller x 16 Chip for electrical specifications and operation.

DALLAS SEMICONDUCTOR

DS1212
Nonvolatile Controller x 16 Chip

FEATURES

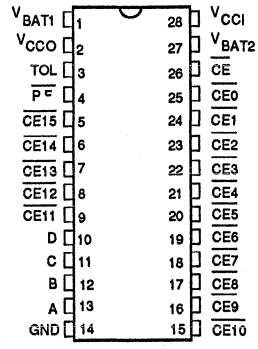
- Converts full CMOS RAM into nonvolatile memory
- Unconditionally write protects when V_{CC} is out of tolerance
- Automatically switches to battery when power fail occurs
- 4 to 16 decoder provides control for up to 16 CMOS RAMs
- Consumes less than 100 nA of battery current
- Tests battery condition on power-up
- Provides for redundant batteries
- Power fail signal can be used to interrupt processor on power failure
- Optional 5% or 10% power fail detection
- Optional 28-pin PLCC surface mount package

DESCRIPTION

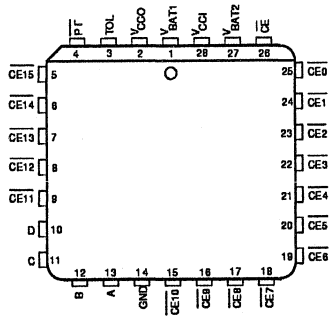
The DS1212 Nonvolatile Controller x16 Chip is a CMOS circuit that solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enables are inhibited to accomplish write protection and the battery is switched on to supply the RAMs with uninterrupted power. Special circuitry uses a low-leakage CMOS process that affords precise voltage detection at extremely low battery consumption.

By combining the DS1212 Nonvolatile Controller chip and lithium batteries, years of nonvolatile RAM operation can be achieved for up to 16 CMOS memories.

PIN DESCRIPTION



28-Pin DIP
(600 Mil)



28-Pin PLCC

PIN NAMES (\ Denotes Condition Low)

A, B, C, D	Address Inputs
CE\	Chip Enable
CE0\-CE15\	Chip Enable Outputs
GND	Ground
V_{BAT1}	+ Battery 1
V_{BAT2}	+ Battery 2
TOL	Power Supply Tolerance
V_{CCI}	+5V Supply
V_{CCO}	RAM Supply
PF\	Power Fail

OPERATION

The DS1212 performs six circuit functions required to decode and battery back up a bank of up to 16 RAMs. First, the 4 to 16 decoder provides selection of one of 16 RAMs. Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater. This switch has a voltage drop of less than 0.2V. The third function the DS1212 provides is power fail detection. It constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.75 volts, or 4.5 volts, depending on the level of tolerance Pin 3, a precision comparator outputs a power fail detect signal to the decoder/chip enable logic and the PF\ signal is driven low. The PF\ signal will remain low until V_{CCI} is back in normal limits.

The fourth function of write protection is accomplished by holding all chip enable outputs (CE0\-CE15\) to within 0.2 volts of V_{CCI} or battery supply. If CE\ is low at the time power fail detection occurs, the chip enable outputs are kept in their present state until CE\ is driven high. The delay of write protection until the current memory cycle is completed prevents corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with tolerance Pin 3 grounded. If Pin 3 is connected to V_{CCO}, then power fail occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 4-to-16 decoder, shown in Figure 1.

The fifth function the DS1212 performs is a battery status warning so that data loss is avoided. Each time the circuit is powered up, the battery voltage is checked with a precision comparator. If the battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0 volts and data is in danger of being corrupted.

The sixth function of the DS1212 provides for battery redundancy. In many applications, data

NONVOLATILE CONTROLLER/DECODER Figure 1

INPUTS					OUTPUTS															
CE\	D	C	B	A	CE0\	CE1\	CE2\	CE3\	CE4\	CE5\	CE6\	CE7\	CE8\	CE9\	CE10\	CE11\	CE12\	CE13\	CE14\	CE15\	PF\
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
<L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H

H = High Level
L = Low Level
X = Irrelevant

NOTE: V_{CCI} input is 250 mV lower when TOL PIN 3 = V_{CCO}.

integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1212 provides an internal isolation switch which allows the connection of two batteries during battery backup operation. The battery with the highest voltage is selected for use. If one battery should fail, the other will then assume the load. The switch to a redundant battery is transparent to circuit operation and the user. A battery status warning will only occur if both batteries are less than 2.0 volts. For single battery applications the unused battery input must be grounded.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
PIN 3 = V_{CCO} Supply Voltage	V_{CCO}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CCI}=4.75 to 5.5V, Pin 3 =GND) (0°C to 70°C, V_{CC} =4.5 to 5.5V, Pin3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Current @ V_{CCO}= V_{CCI}-0.2	I_{CCO1}			80	mA	1,4,10
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
CE0\-CE15\,PF\ Output @ 2.4V	I_{OH}	-1.0			mA	5
CE0\-CE15\,PF\ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

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(0°C to 70°C, V_{CCI}<V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE0\-CE15 Output	V_{OHL}	V_{BAT}-0.2			V	3,7
Battery Current	I_{BAT}			0.1	uA	2,3
Battery Backup Current @ V_{CCO}=V_{BAT1}-0.5V	I_{CC2}			100	uA	6,10,11

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

(0°C to 70°C, V_{CCI}=4.75 to 5.5V, Pin 3=GND)

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI}=4.5 to 5.5V, Pin 3=V_{CCO})

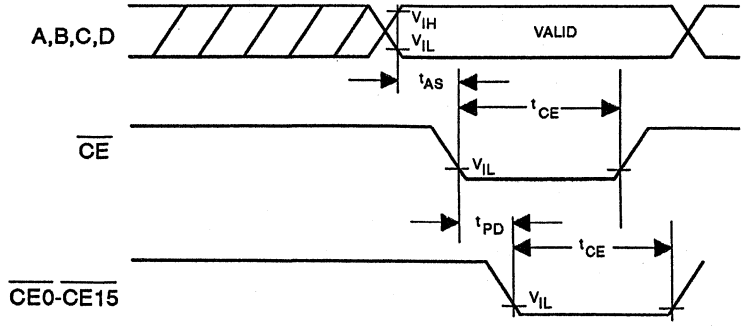
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE\ Propagation Delay	t_{PD}	5	10	20	ns	5
CE\ High to Power Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C, V_{CCI}<4.75V, Pin 3=GND)

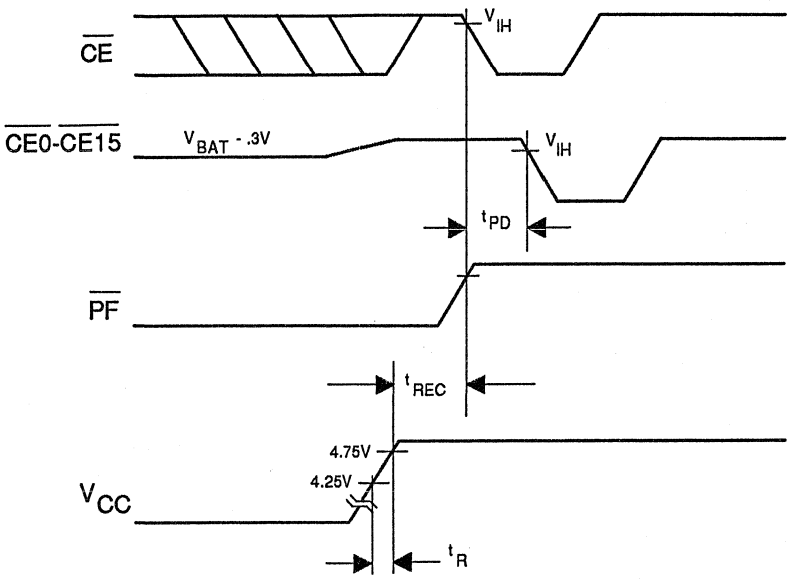
(0°C to 70°C, V_{CCI}<4.5V, Pin 3=V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power-Down	t_F	300			us	
V_{CC} Slew Rate Power-Down	t_{FB}	10			us	
V_{CC} Slew Rate Power-Up	t_R	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7,8
Power Fail to PF\ Low	t_{PFL}	300			us	

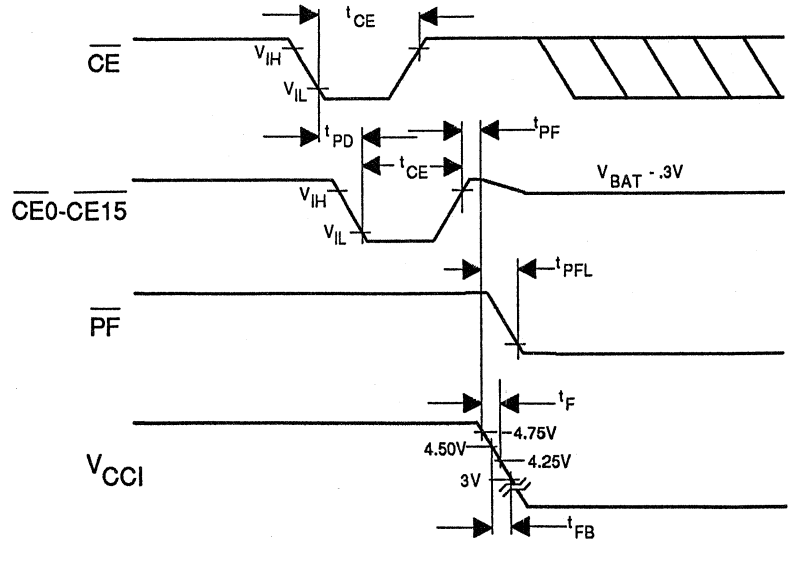
TIMING DIAGRAM - DECODER



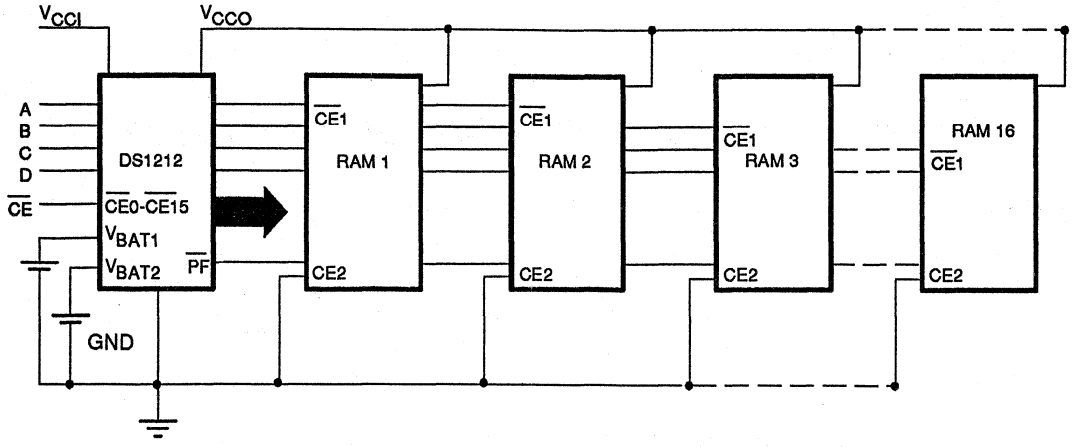
TIMING DIAGRAM - POWER UP



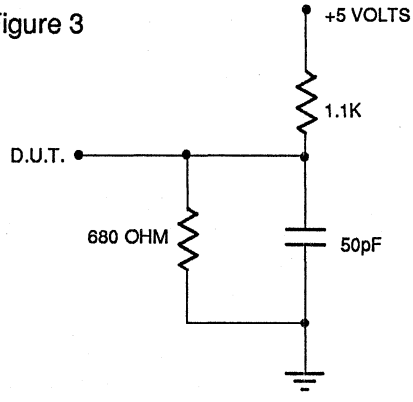
TIMING DIAGRAM - POWER DOWN



TYPICAL APPLICATION Figure 2



OUTPUT LOAD Figure 3



NOTES:

1. All voltages referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and CE0\-CE15\ open.
4. I_{CCO1} is the maximum average load which the DS1212 can supply to the memories.
5. Measured with a load as shown in Figure 3.
6. I_{CCO2} is the maximum average load current which the DS1212 can supply to the memories in the battery backup mode.
7. Chip enable outputs CE0\-CE15\ can only sustain leakage current in the battery backup mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While CE\ is low, the outputs (CE0\-CE15\) will be defined by inputs A through D with a propagation delay of t_{PD} from an A through D input change.
10. For applications where higher currents are required, please see the Battery Manager chip data sheet (DS1259).
11. The DS1212 has a 5K ohm resistor is series with the battery input. As current from the battery increases over 100 uA, the voltage drop will increase proportionately. The device cannot be damaged by higher currents in the battery path.

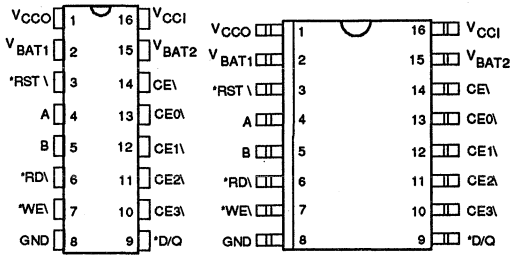
DALLAS SEMICONDUCTOR

DS1221/S
Nonvolatile Controller x 4 Chip

FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Data is automaticallly protected during power loss
- 2-to-4 decoder provides for up to 4 CMOS RAMs
- Provides for redundant batteries
- Test battery condition on power-up
- Full +/- 10% operating range
- Unauthorized access can be prevented with optional security feature
- 16-pin 0.3-inch DIP saves PC board space
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1221 16-Pin DIP (300 Mil)

DS1221S 16-Pin SOIC (300 Mil)

PIN NAMES (\ Denotes Condition Low)

A, B	Address Inputs
CE\	Chip Enable Inputs
CE0\ - CE3\	Chip Enable Outputs
V_{BAT1}	+ Battery 1
V_{BAT2}	+ Battery 2
*RST\	Reset
V_{CCI}	+5V Supply
V_{CCO}	RAM Supply
*RD\	Read Input
*WE\	Write Input
*D/Q	Data Input/Output

*Used with optional security circuit only and must be connected to ground in all other cases.

DESCRIPTION

The DS1221 Nonvolatile Controller x 4 Chip is a CMOS circuit which solves the application problem of converting CMOS RAMs into nonvolatile memories. Incoming power is monitored for an out-of-tolerance condition. When such a condition is detected, the chip enable outputs are inhibited to accomplish write protection and the battery is switched on to supply RAMs with uninterrupted power. An optional security code prevents unauthorized users from obtaining access to the memory space. The nonvolatile controller/decoder circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. By combining the DS1221 with up to four CMOS memories and lithium batteries, ten years of nonvolatile operation can be achieved.

CONTROLLER /DECODER OPERATION

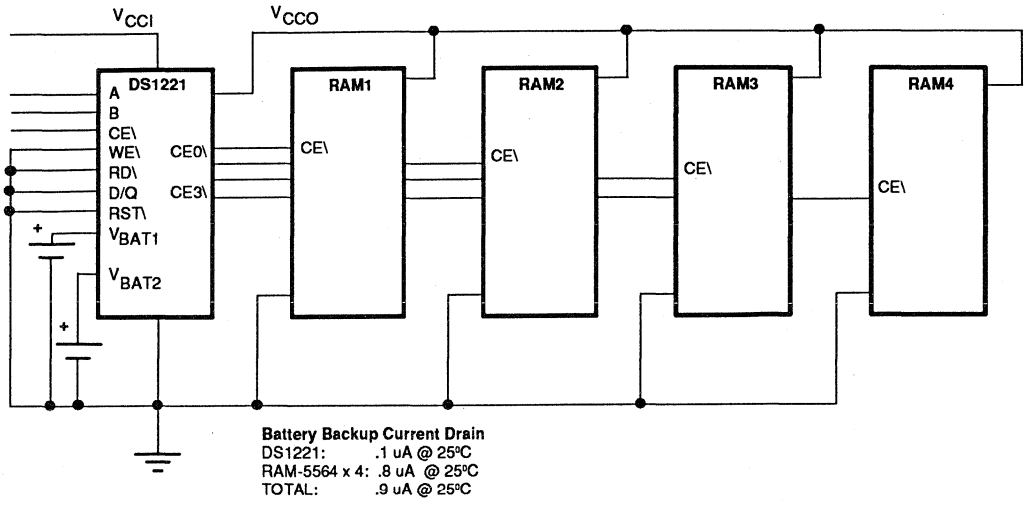
The DS1221 nonvolatile controller performs six circuit functions required to decode and battery back up a bank of up to four CMOS RAMs. First, a 2-to-4 decoder provides selection of one of four RAMs (see Figure 1). Second, a switch is provided to direct power from the battery or V_{CCI} supply, depending on which is greater, to the V_{CCO} pin. This switch has a voltage drop of less than 0.2V. The third function which the nonvolatile controller provides is power-fail detection. The DS1221 constantly monitors the V_{CCI} supply. When V_{CCI} falls below 4.5 volts, a precision comparator detects the condition and inhibits the RAM chip enables (CE0\ through CE3\). The fourth function of write protection is accomplished by holding all chip enable outputs (CE0\ through CE3\) to within 0.2 volts of V_{CCI} or battery supply. If the Chip Enable Input (CE\) is low at the time power-fail detection occurs, the chip enable outputs are kept in their present state until CE\ is driven high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power failure detection occurs in the range of 4.5 to 4.25 volts. During nominal supply conditions the chip enable outputs follow the logic of a 2-to-4 decoder. The fifth function the DS1221 performs is to check battery status to warn of potential data loss. Each time that V_{CCI} power is restored the battery voltage is checked with a precision comparator. If the connected battery voltage is less than 2 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location, altering the data. If the next read cycle fails to verify the written data, the contents of the memories are questionable. The sixth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1221 provides an internal isolation switch which provides for connection of two batteries. During battery back-up operation the battery with the highest voltage is selected for use. If one battery should fail, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur if both batteries are less than 2.0 volts. If only one battery is used, the second battery input must be grounded. Figure 2 illustrates the connections required for the DS1221 in a typical application.

NONVOLATILE CONTROLLER/DECODER Figure 1

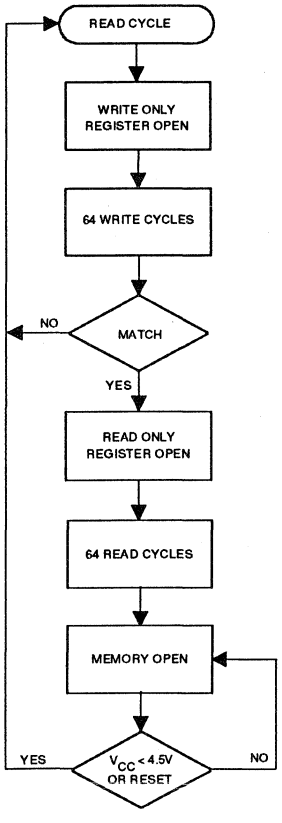
	INPUTS			OUTPUTS			
V_{CCI}	CE\	B	A	CEO\	CE1\	CE2\	CE3\
>=4.5	H	X	X	H	H	H	H
< 4.25	X	X	X	H	H	H	H
>=4.5	L	L	L	L	H	H	H
>=4.5	L	L	H	H	L	H	H
>=4.5	L	H	L	H	H	L	H
>=4.5	L	H	H	H	H	H	L

H = High Level
L = Low Level
X = Irrelevant

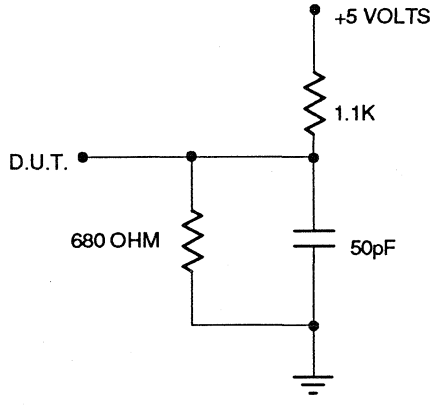
TYPICAL APPLICATION Figure 2



SECURITY SEQUENCE Figure 3



OUTPUT LOAD Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	20 mA

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1} V_{BAT2}	2.0		4.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC}-0.2			V	1
Supply Current	I_{CCO1}			80	mA	4, 10
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
CE0\-CE3\, DQ Output @ 2.4V	I_{OH}	-1.0			mA	5
CE0\-CE3\, DQ Output @ 0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1

(0°C to 70°C, V_{CC}< 4.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE0\-CE3\ Output	V_{OHL}	V_{CC}-0.2 V_{BAT}-0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			0.1	uA	3
Battery Backup Current @ V_{CCO} = V_{BAT} - 0.5V	I_{CCO2}			100	uA	6, 7, 10

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE\ Propagation Delay	t_{PD}	5	10	20	ns	5
CE\ High to Power-Fail	t_{PF}			0	ns	
Address Setup	t_{AS}	20			ns	9

(0°C to 70°C, V_{CC}< 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2	5	10	ms	
V_{CC} Slew Rate 4.5 - 4.25V	t_F	300			us	
V_{CC} Slew Rate 4.25 - 3V	t_{FB}	10			us	
V_{CC} Slew Rate 4.25 - 4.5V	t_R	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7, 8

NOTES:

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and CE0\ - CE3\ open.
4. I_{CCO1} is the maximum average load which the DS1221 can supply to the memories.
5. Measured with a load as shown in Figure 4.
6. I_{CCO2} is the maximum average load current which the DS1221 can supply to the memories in the battery back-up mode.
7. Chip enable outputs CE0\ - CE3\ can only sustain leakage current in the battery back-up mode.
8. t_{CE} max. must be met to ensure data integrity on power loss.
9. t_{AS} is only required to keep the decoder outputs glitch-free. While CE\ is low, the outputs (CE0\ - CE3\) will be defined by inputs A and B with a propagation delay of t_{PD} from an A or B input change.
10. For applications where higher currents are required, please see the DS1259 Battery Manager Chip data sheet.

SECURITY OPTION

When activated by Dallas Semiconductor, the security option prevents unauthorized access. A sequence of events must occur to gain access to the memories (Figure 3). First, a dummy read cycle or a 200 ns active low reset pulse is executed to initialize the sequence. Second, a 64-bit access code must be consecutively written to the DS1221 using the write enable signal (WE\), the chip enable signal (CE\), and the data input/output signal (DQ). The code is written to the DS1221 without regard to the address. Actual RAM locations are not written, as the security option is intercepting the data path until access is granted. Instead, a special 64-bit write only register is written. Following the 64 write cycles, the register is compared to a 64-bit pattern uniquely defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. This pattern can only be interrogated by an intelligent controller within the DS1221 and cannot be read by the user. If a read cycle occurs before 64 write cycles are completed, the security sequence is aborted. When a correct match for 64 bits is received, the third part of the security sequence begins by reading a 64-bit read only register. This register consists of 64 bits also defined by the user and programmed into the DS1221 by Dallas Semiconductor at the time of manufacture. For each of the 64 read cycles, one bit of the user-defined read only register is driven onto the DQ line. This phase also requires that the 64 read cycles be consecutive. The data being read from the read only register can be used by software to determine if the DS1221 will be permitted to be used with that particular system. After the 64th read cycle has been executed the DS1221 is unlocked and all subsequent memory cycles will be passed through and will become actual memory accesses based upon address inputs. If V_{CC} falls below 4.5 volts or the reset line is driven low, the entire security sequence must be executed again in order to access memory locations.

NOTE: Contact Dallas Semiconductor sales office for code assignments.

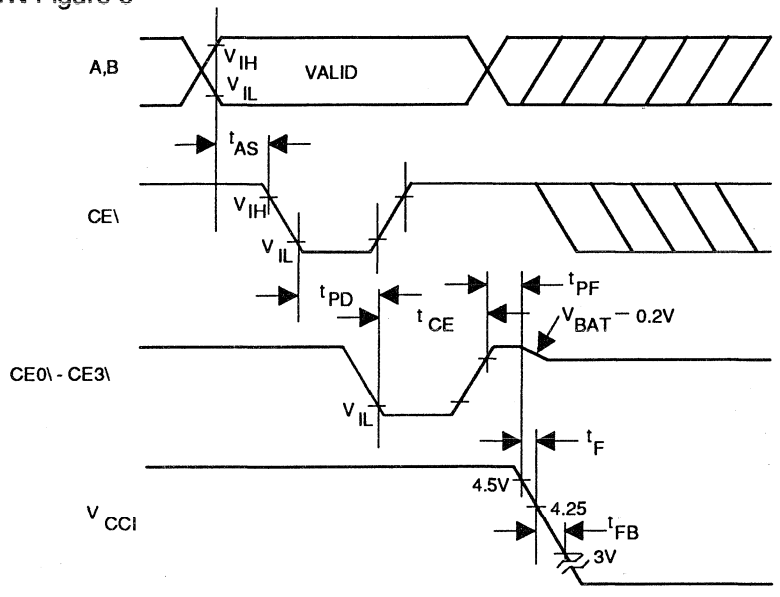
SECURITY OPTION

AC ELECTRICAL CHARACTERISTICS

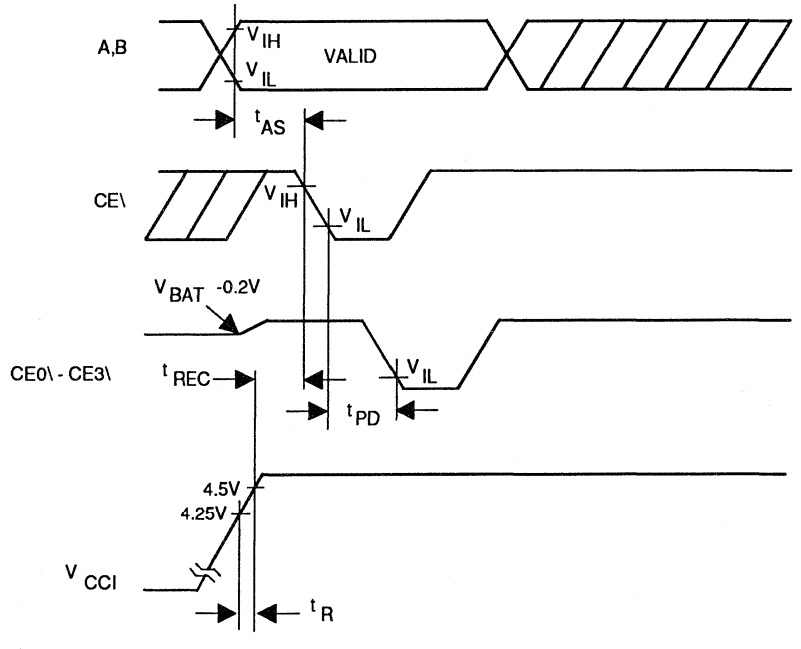
(0°C to 70°C, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
CE\ Access Time	t_{CO}			200	ns	
RD\ Access Time	t_{OE}			100	ns	
CE\ to Output Low Z	t_{COE}	10			ns	
RD\ to Output Low Z	t_{OEE}	10			ns	
CE\ to Output High Z	t_{OD}			100	ns	
RD\ to Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	
Data Setup	t_{DS}	100			ns	
Data Hold Time	t_{DH}	0			ns	
CE\ Pulse Width	t_{CW}	170			ns	
Reset Pulse Width	t_{RST}	200			ns	

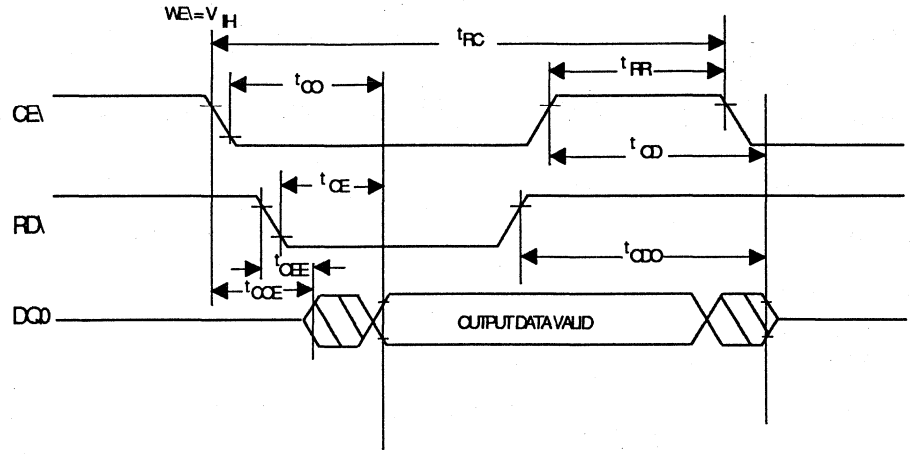
POWER-DOWN Figure 5



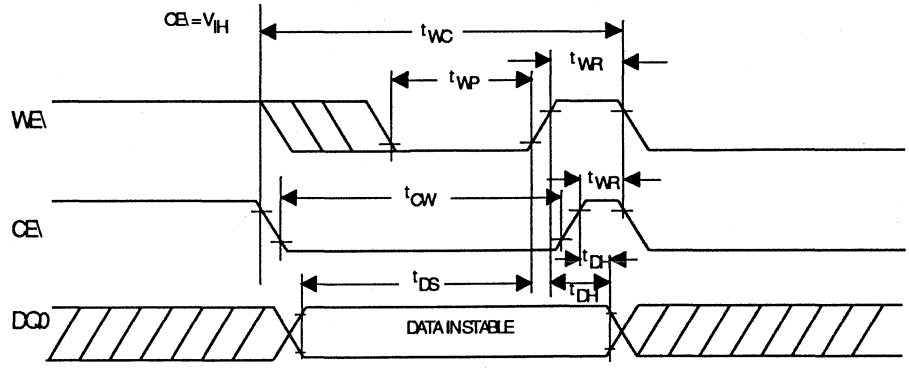
POWER-UP Figure 6



READ CYCLE TO SECURITY OPTION Figure 7

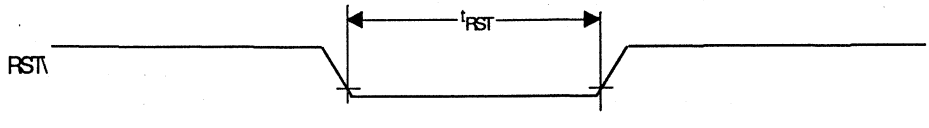


WRITE CYCLE TO SECURITY OPTION Figure 8



NOTES:
1. t_{DH} and t_{DS} are functions of the first occurring edge of WE\ or CE\.
2. t_{WR} is a function of the latter occurring edge of WE\ or CE\.

RESET FOR SECURITY OPTION Figure 9



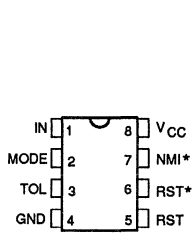
DALLAS SEMICONDUCTOR

DS1231/S
Power Monitor Chip

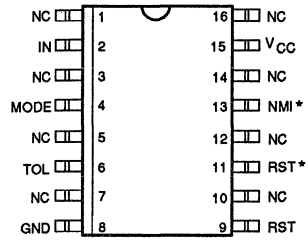
FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying non-volatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power-up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1231 8-Pin DIP
(300 Mil)



DS1231S 16-Pin SOIC
(300 Mil)

PIN NAMES (* Denotes Condition Low)

IN	-Input
MODE	-Selects input pin characteristics
TOL	-Selects 5% or 10% V_{CC} detect
GND	-Ground
RST	-Reset (Active High)
RST*	-Reset (Active Low, open drain)
NMI*	-Nonmaskable interrupt
V_{CC}	-+5 V Supply
NC	-No Connections

DESCRIPTION

The DS1231 Power Monitor Chip uses a precise temperature compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the Power Monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor detects out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and RST* (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and RST* signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC}, the RST and RST* signals become active as V_{CC} goes below 4.5 volts. The RST and RST* signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and RST* are kept active for a minimum of 150 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the NMI* signal (Pin 7) when the input threshold voltage (V_{TP}) falls to a level as determined by Mode (Pin 2). When the Mode pin is connected to V_{CC}, detection occurs at V_{TP}-. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the Mode pin is connected to ground, detection occurs at V_{TP}+. In this mode Pin 1 sources 30 uA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between NMI* and RST*. On power-up, NMI* is released as soon as the input threshold voltage (V_{TP}) is achieved and V_{CC} is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

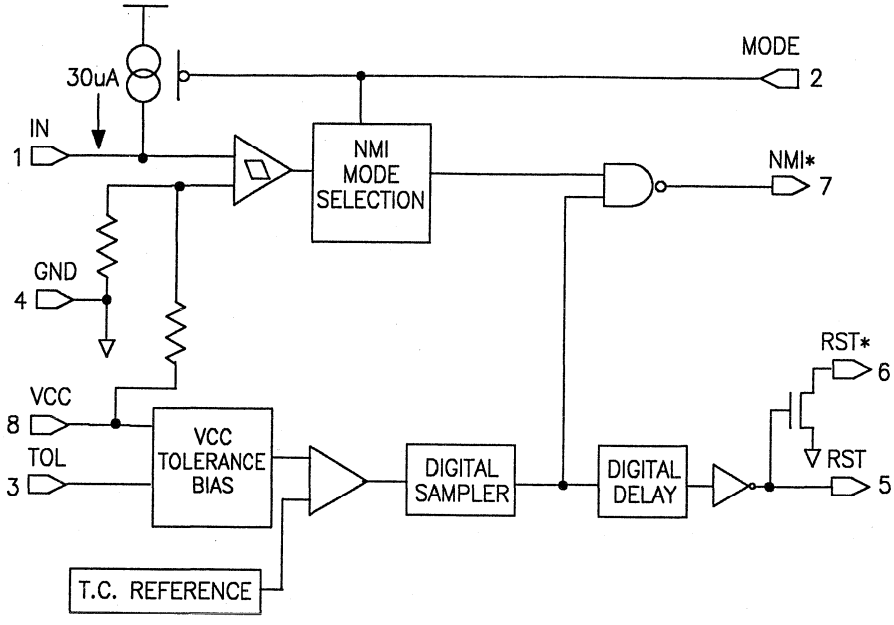
APPLICATION-MODE PIN CONNECTED TO V_{CC}

When the Mode pin is connected to V_{CC}, pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

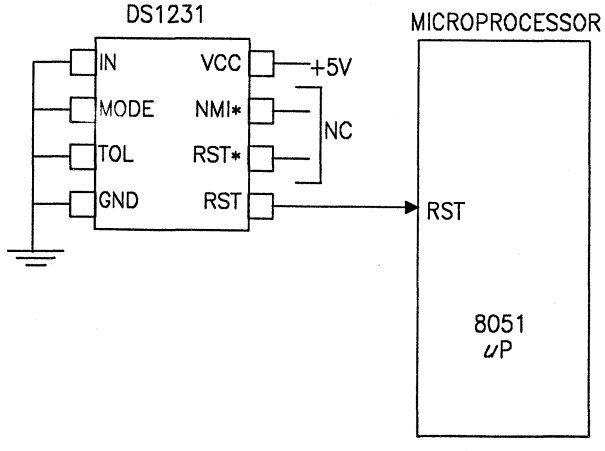
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1), which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point V_{TP}- is 2.3 volts (using the -20 device), and the maximum allowable voltage on pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0=.46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate NMI*.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high impedance to keep power consumption low and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC}.

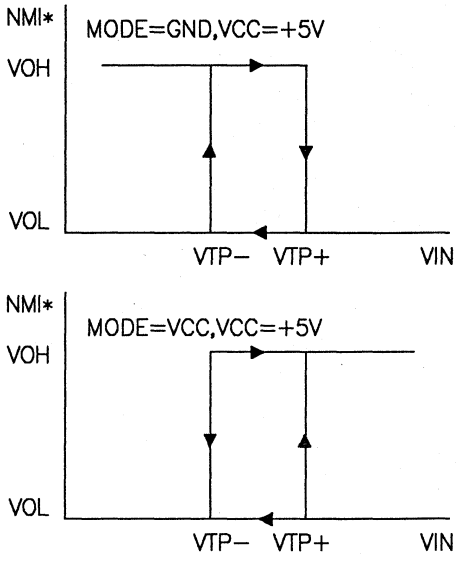
POWER MONITOR BLOCK DIAGRAM Figure 1



POWER-UP RESET Figure 2



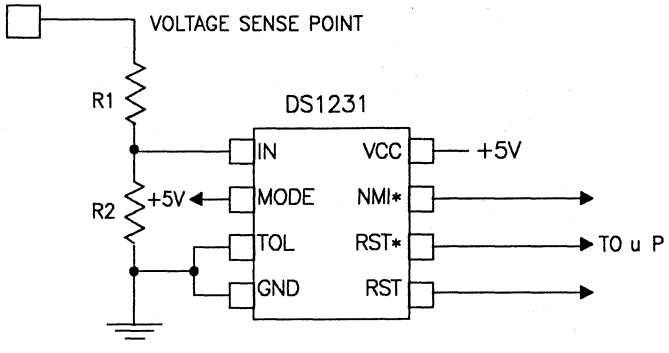
INPUT PIN HYSTERESIS Figure 3



	−20	−35	−50
VTP−	2.3	2.15	2.0
VTP+	2.5	2.5	2.5

NOTE: HYSTERESIS TOLERANCE IS +/−60mV

APPLICATION WITH MODE PIN CONNECTED TO V_{cc} Figure 4



$$V\ SENSE = \frac{R1 + R2}{R2} \times 2.3 \qquad V\ MAX = \frac{V\ SENSE}{VTP-} \times 5.0$$

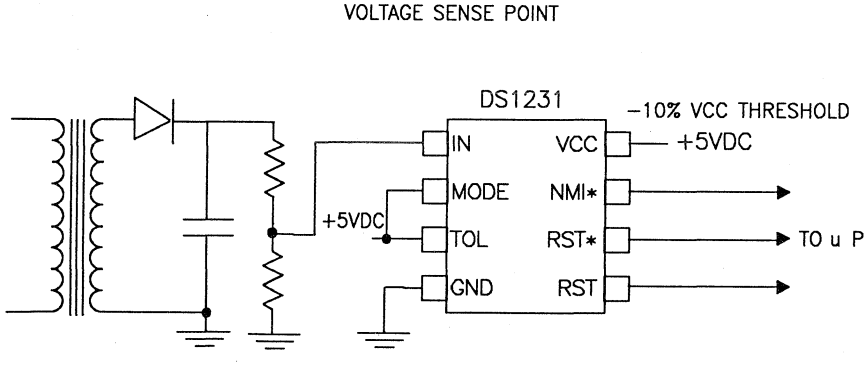
EXAMPLE: V SENSE = 8 VOLTS AT TRIP POINT AND A MAXIMUM VOLTAGE OF 17.5V WITH R2 = 10K

$$THEN\ 8 = \frac{R1 + 10K}{10K} \times 2.3 \qquad R1 = 25K$$

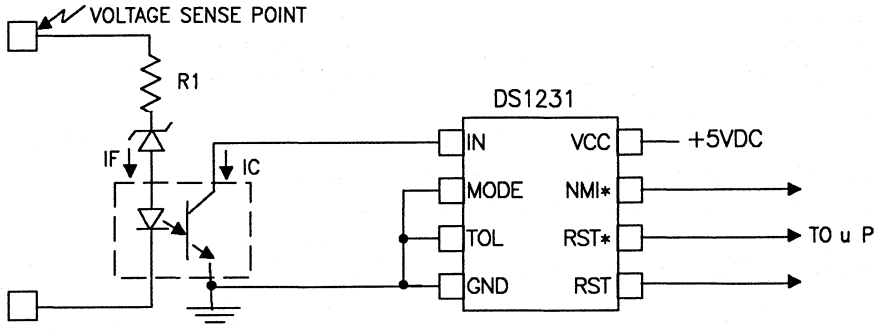
APPLICATION - MODE PIN CONNECTED TO GROUND

When the Mode pin is connected to ground, pin 1 is a current source of 30 uA with a VTP+ of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be low enough to allow the opto-isolator to sink the 30 uA of collector current required by pin 1 and still have enough resistance to keep the maximum current though the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



APPLICATION WITH MODE PIN GROUNDED Figure 6



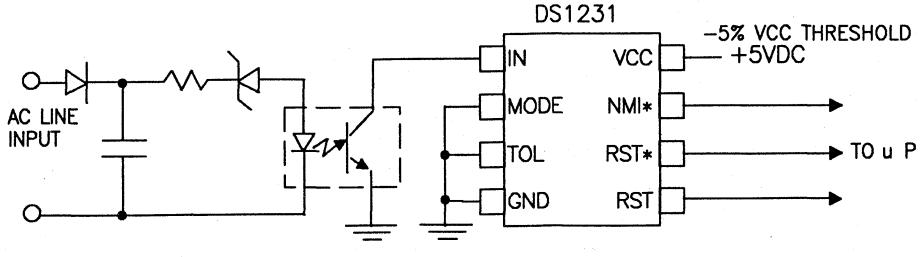
VOLTAGE SENSE POINT (TRIP VALUE) $= VZ + \frac{IC}{CTR} \times R1$

$CTR = \frac{IC}{IF}$ CTR = CURRENT TRANSFER RATIO
VZ = ZENER VOLTAGE

EXAMPLE: CTR = 0.2 IC = 30 uA IF = 150 uA
VOLTAGE SENSE POINT = 105 AND
VZ = 100 VOLTS

THEN $105 = 100 + \frac{30}{0.2} XR$ R1 = 33K

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC}= 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-10		+10	*u*A	2
Output Current @2.4V	I_{OH}	1.0	2.0		*m*A	5
Output Current @0.4V	I_{OL}	2.0	3.0		*m*A	
Operating Current	I_{CC}		0.5	2.0	*m*A	3
Input Pin 1 (Mode=GND)	I_C	15	25	50	uA	
Input Pin 1 (Mode=V_{CC})	I_C			0.1	*u*A	
IN Trip Piont (Mode=GND)	V_{TP}	See Figure 3				1
IN Trip Point (Mode=V_{CC})	V_{TP}					1
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

070290 7/9

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

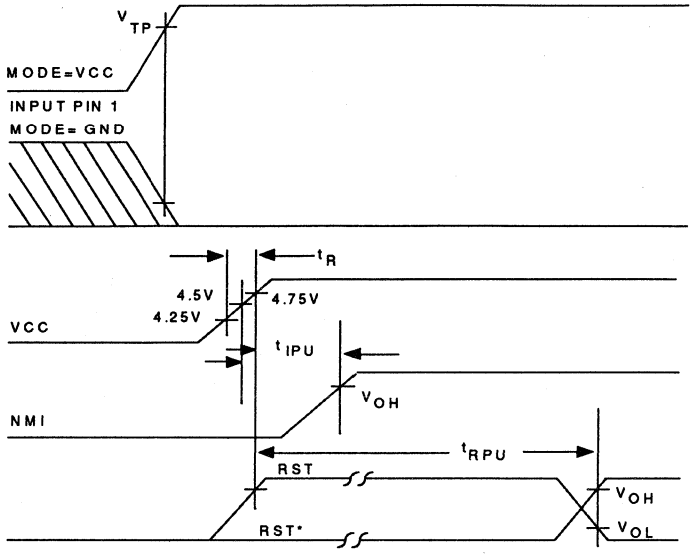
(0° to 70°C,V_{CC}=5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to NMI* Delay	t_{IPD}			1.1	us	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			us	
V_{CC} Detect to RST and RST*	t_{RPD}			100	ns	
V_{CC} Detect to NMI*	T_{IPU}			200	us	4
V_{CC} Detect to RST and RST*	t_{RPU}	150	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

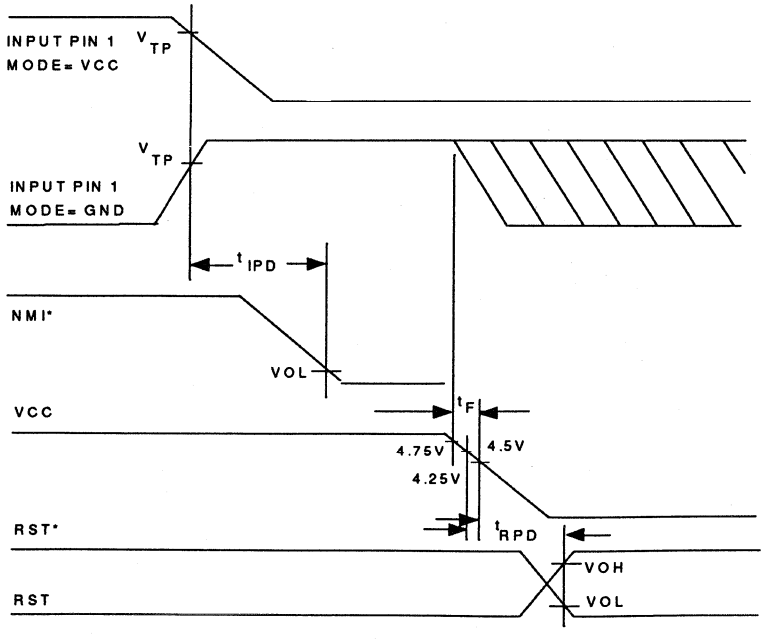
NOTES:

1. All voltages referenced to ground.
2. V_{CC} = +5.0 volts with outputs open.
3. Measured with outputs open.
4. t_R = 5us.
5. RST* is an open drain output.

TIMING DIAGRAM-POWER-UP



TIMING DIAGRAM-POWER-DOWN



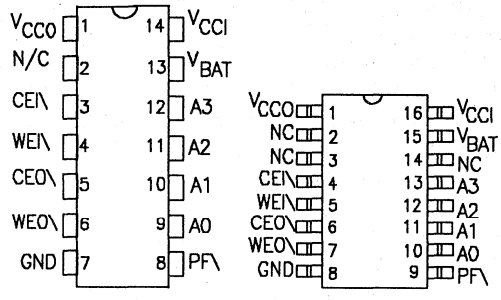
DALLAS SEMICONDUCTOR

DS1234
Conditional Nonvolatile Controller Chip

FEATURES

- Converts CMOS static RAMs into nonvolatile memories
- Software controlled write inhibit
- Software controlled battery disconnect extends battery life
- Unconditionally write protects when V_{CC} is out of tolerance
- Consumes less than 100 nA of battery current
- Power fail signal can be used to interrupt processor on power failure
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1234
14-Pin DIP (300 Mil)

DS1234S
16-Pin SOIC (300 Mil)

PIN NAMES (\ Denotes Condition Low)

Pin#	Pin Name	Description
1	V_{CCO}	RAM Supply
2	N/C	No Connection
3	CEI\	Chip Enable Input
4	WEI\	Write Enable Input
5	CEO\	Chip Enable to RAM
6	WEO\	Write Enable to RAM
7	GND	Ground
8	PF\	Power Fail Output
9-12	A0-A3	Address Inputs
13	V_{BAT}	Battery Input
14	V_{CCI}	+5V Supply

DESCRIPTION

The DS1234 is a CMOS circuit that converts CMOS RAM into nonvolatile memory and adds two software selectable switches. Incoming power is monitored for an out-of-tolerance condition. When such a conditions is detected, chip enable and write enable to the RAM are inhibited to accomplish write protection, and the battery is switched on to supply the memory with uninterrupted power. The two software selectable switches provided by the DS1234 are capable of inhibiting both the write enable to the RAM and the battery backup circuitry by a pattern recognition sequence across four address lines. Inhibiting the write enable to the nonvolatile RAM provides data integrity by isolating the memory contents from external change. The second switch provides added flexibility and increases battery life to the system by enabling/disabling the battery for shipment or storage, or when battery backup is not needed.

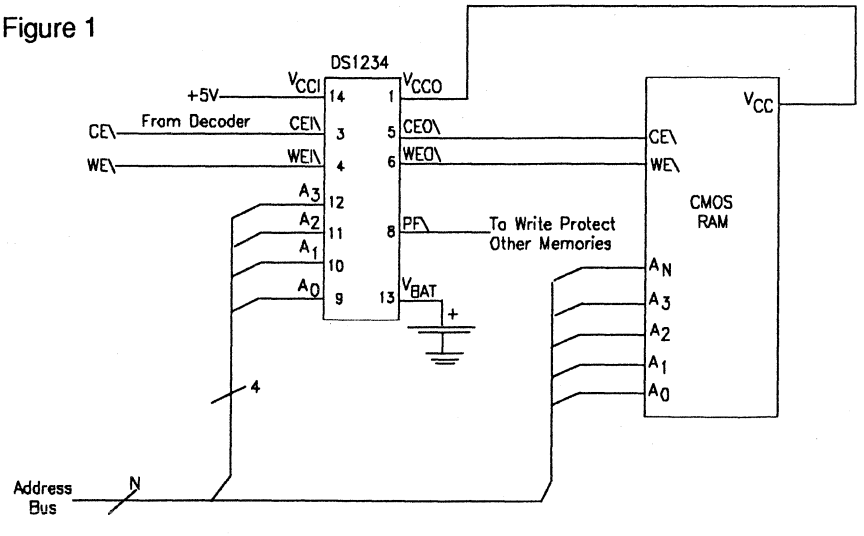
OPERATION

The DS1234 Conditional Nonvolatile Controller performs three circuit functions required to battery backup a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}), depending on which is greater. This switch has a voltage drop of less than 0.2V. The second function is power fail detection. The DS1234 constantly monitors the incoming supply. When the supply goes out-of-tolerance, a comparator detects power fail and inhibits chip enable and write enable. The threshold voltage, V_{TP}, at which power fail is detected is defined as 1.26 times V_{BAT}. The third function of write protection is accomplished by holding the CEO\ and WEO\ output signals to within 0.2 volts of the V_{CCI} or battery supply.

In addition to the nonvolatile controller functions, the DS1234 supplies two software selectable switches for master control of the write enable and the nonvolatile controller itself. The switches are controlled by a 16-cycle pattern recognition sequence across four address lines (see Tables 1 and 2). Prior to entering the pattern recognition sequence that will define the two switch settings, a read cycle of 1111 on address inputs A0 through A3 should be executed to initialize the compare pointer of clock zero. Each four-bit compare word is clocked into the DS1234 on the negative edge of CE\. A0, A1 and A2 must match the compare pattern on all 16 consecutive cycles while A3 must match only the first eleven; the last five are used to define the switch settings. The eleventh address cycle, starting at zero, defines the switch that inhibits the write enable to the RAM (WEO\). A logic one in this location allows read/write operations so that WEO\ will follow WEI\ and data can be updated. A zero on cycle eleven turns the RAM into a read-only memory (ROM). The next four address cycles, 12 thorough 15, define whether the nonvolatile controller operation is enabled or disabled. A bit pattern of 1010 activates the nonvolatile controller; data in the RAM is maintained on power loss. Any pattern other than 1010 will disable the nonvolatile controller operation.

At the completion of the 16th cycle, if the pattern recognition sequence is correct, the switch settings defined in cycles 11 though 15 are transferred and are active for the next memory cycle. When external battery power is applied for the first time, the DS1234 will come up with the nonvolatile controller off. Upon initial V_{CC} power, the write enable will be set in read/write operation (WEI\=WEO\).

Figure 1



ADDRESS INPUT PATTERN Table 1

	CYCLE NUMBER															
Address Inputs	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A3	1	0	1	0	0	0	1	1	0	1	0	*	*	*	*	*
A2	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A1	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

* See Table 2

CONTROL SELECT Table 2

WE\ Battery Control					**Operation**
11	**12**	**13**	**14**	**15**	
0	X	X	X	X	Read Only Operation
1	X	X	X	X	Read/Write Operation
X	1	0	1	0	Enables Nonvolatile Controller*

X = Don't Care

*Any other combination turns controller off

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	2
Supply Current @ $V_{CCO} = V_{CCI}$ - 0.2	I_{CCO}			80	mA	3
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	4.0			mA	4

(0°C to 70°C, $V_{CCI} < V_{BAT}$)

CE0\, WE0\ Output	V_{OHL}	V_{BAT}-0.2			V	6
Battery Current	I_{BAT}			0.1	uA	7
Battery Backup Current @ $V_{CCO} = V_{BAT}$ - 0.3V	I_{CCO1}			100	uA	5

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTIC

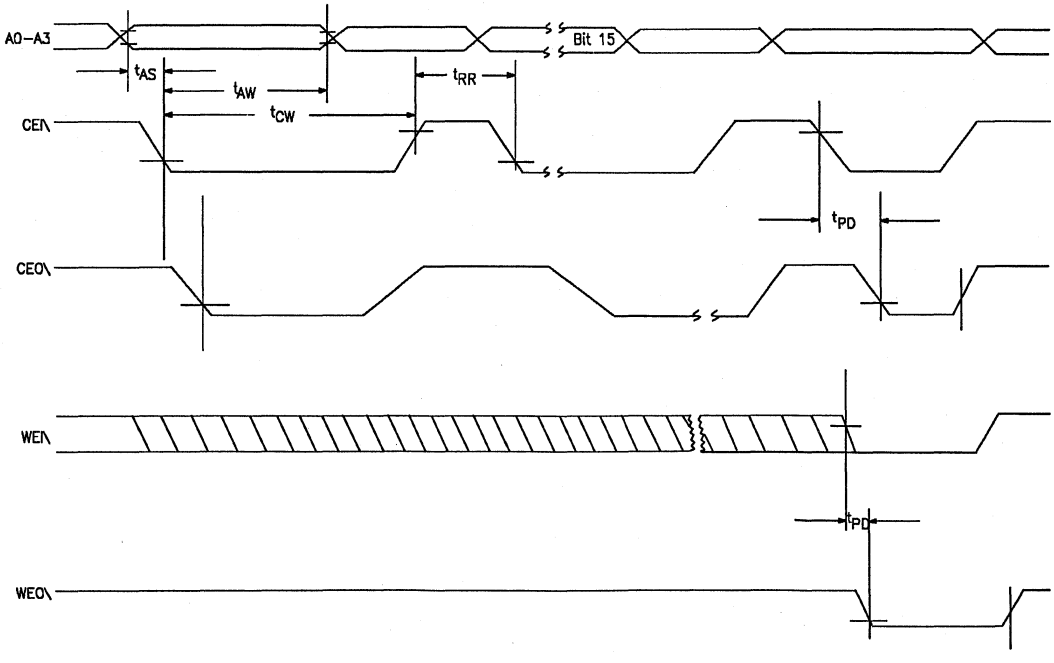
(0^oC to 70^oC, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
CE\ Pulse Width	t_{CW}	110			ns	
Propagation Delay	t_{PD}			20	ns	

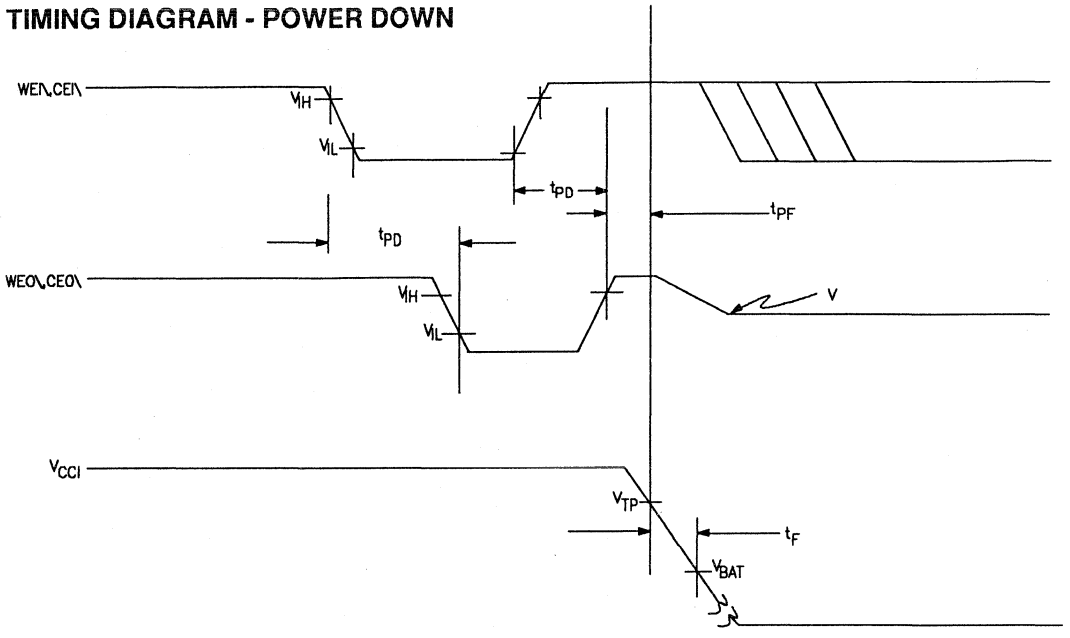
(0^oC to 70^oC, $V_{ccI} < V_{TP}$)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate Power Down	t_F	0			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
CE\ High to Power Fail	t_{PF}	0			ns	

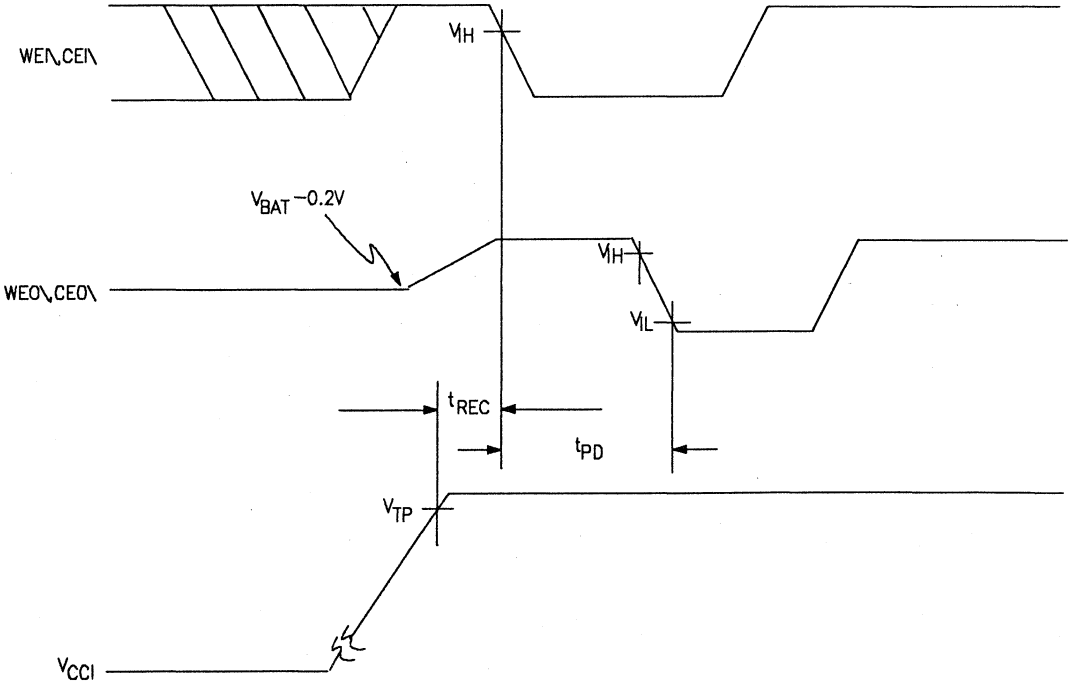
TIMING DIAGRAM - SWITCH SETTING



TIMING DIAGRAM - POWER DOWN



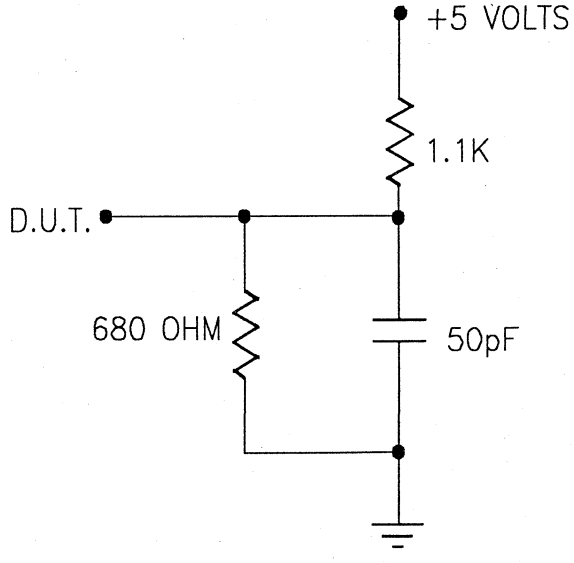
TIMING DIAGRAM - POWER UP



NOTES:

1. All voltages are referenced to ground.
2. Measured with V_{CCO}, CE0\ and WE0\ open.
3. I_{CCO} is the maximum average load which the DS1234 can supply to the memories.
4. Measured with a load as shown in Figure 2.
5. I_{CCO1} is the maximum average load current which the DS1234 can supply to the memories in the battery backup mode.
6. Chip Enable, CEO\, and Write Enable, WEO\, outputs can only sustain leakage current in the battery backup mode.
7. I_{BAT} is the total load current which the DS1234 uses from the battery input pin with V_{CCO}, CE0\, and WEO\ open.

OUTPUT LOAD Figure 2



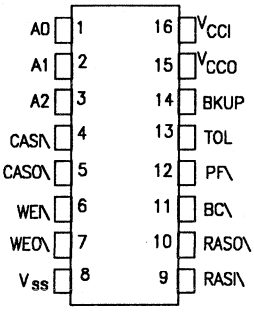
DALLAS SEMICONDUCTOR

DS1237
DRAM Nonvolatizer Chip

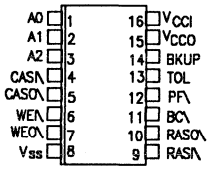
FEATURES
- Converts DRAM into nonvolatile RAM
- Controls any density of DRAM
- Wide backup supply voltage range
- Automatically refreshes when power fail detection occurs
- Power fail detection signal for hardwire interrupt
- Refresh is turned over to the processor after power-up under software control
- Space-saving 16-pin DIP and 16-pin SOIC for surface mounting
- Low-power CMOS
- Built-in backup condition circuit warns of impending backup supply failure
- Software-controlled backup supply disconnects switch for storage and shipment
- Software-controlled counter measures backup supply discharge time
- Optional refresh periods of 8 ms, 16 ms, 32 ms, and 64 ms are available to support extended refreshing at reduced power levels

DESCRIPTION
The DS1237 DRAM Nonvolatizer Chip is a CMOS circuit designed to control DRAMs such that information stored in memory is retained and protected during power failure. The DS1237 accomplishes this by monitoring the power supply for an out-of-tolerance condition. When such a condition occurs, DRAM is isolated from system control and the power supply for the DRAM is switched from V_{CC} to the backup supply. Refresh control is maintained by the DS1237 until the power is within specifications. At this time refresh is returned to the system after a highly structured serial sequence on address lines A0, A1, and A2. Other serial sequences are used to set switches which control a counter used to measure backup supply discharging and electrically connect or disconnect the backup supply.

PIN CONNECTIONS



DS1237 16-Pin DIP (300 Mil)



DS1237S16-Pin SOIC (300 Mil)

PIN NAMES (\ Indicates Condition Low)

BKUP	- Backup Supply
BC\	- Backup Condition
TOL	- V_{CCI} Trip Point Select
PF\	- Power Fail Output
A0-A2	- Address Inputs
Vss	- Ground
WEI\	- Write Enable Input
WEO\	- Write Enable Output
CASI\	- CAS\ Input from System
CASO\	- CAS\ Output to DRAM
RASI\	- RAS\ Input from System
RASO\	- RAS\ Output to DRAM
V_{CCO}	- V_{CC} Output to DRAM
V_{CCI}	- +5 Volt Input

OPERATION - NORMAL POWER CONDITIONS

Under normal operation system +5 volt power is supplied within the tolerance limits set by Pin 13 (TOL). If pin 13 is connected to V_{CCO}, the DS1237 will operate in the normal mode down to 4.75 volts. When pin 13 is grounded, the DS1237 will operate in the normal mode down to 4.5 volts. During normal operation the RAS\, CAS\, and WE\ inputs are directly routed to the respective outputs with a maximum propagation delay of 15 ns. The backup supply input is normally connected to either a chargeable capacitor or battery; however, any backup supply with a voltage input between the limits of 6.0 volts and 10 volts is suitable. The power fail output (PF\) is at high level and address inputs A0, A1, and A2 are monitored for software-driven sequences. The backup condition output BC\ will be in an inactive (high) state provided that the backup input level is greater than 5.5 volts and the backup counter has not reached zero.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5 volt V_{CC} power begins to drop, a precision band gap comparator senses this change. Depending on the level of the Tolerance Pin 13, a power fail signal will be generated as V_{CCI} falls below 4.75 volts or 4.5 volts. The power fail output signal is driven low at this time and will stay low until V_{CCI} is restored to normal conditions. When the data retention mode is turned on, the DS1237 isolates all control inputs and starts driving the RAS\, CAS\, and WE\ outputs. In addition, if RAS\ = 1, the DS1237 immediately takes control and issues the first refresh burst 62.5 uS later. If RAS\ = 0, the DS1237 will wait for RAS to go to a logic 1 level and then take control and issue the first refresh burst 62.5 uS later. If RAS\ = 0 and remains low for more than 10 uS after Power Fail Detect, the DS1237 will take control and drive RAS0\ = 1, then issue the first refresh burst 62.5 uS later. The V_{CCI} input is disconnected from V_{CCO} and the regulated backup supply is connected. A burst CAS\ before RAS\ refresh cycle is generated at a cycle time of 350 ns maximum. This burst refresh continues for 520 or 1032 consecutive cycles, depending on the dash number of the device (see Table 1). After the burst refresh is complete, subsequent burst refreshing continues at 8, 16, 32, or 64 ms intervals until V_{CCI} returns to normal levels and the system signals the DS1237 that it is ready to assume refresh duties. The WE\ output is held at the high (inactive) level from the time power fail is detected until the system assumes refresh duties.

OPERATION - RETURN TO NORMAL POWER CONDITIONS

When the system +5 volt supply returns and exceeds the 4.5 volt BKUP supply voltage on pin 14, the V_{CCI} input is immediately reconnected to the V_{CCO} output pin while the regulated backup supply is internally disconnected from V_{CCO}. Burst refreshing continues without interruption until the system signals that it is ready to assume the responsibility of refreshing the DRAMs. Refresh duties are shifted from the DS1237 to the system when a software controlled switch is set by sending a specific pattern on address lines A0, A1, and A2 for 24 consecutive cycles. This address pattern which sets the software switch is shown in Figure 1. The address pattern is clocked into the DS1237 on the falling edge of CAS\ provided that setup and hold times are met. When the 24th cycle is correctly entered, the DS1237 will issue a final refresh burst and then turn over control to the host system. At this point, the host system will be responsible for handling all refresh requirements. RAM read and write cycles can resume without restrictions after the software switch is correctly set.

ACTIVATION OF BACKUP SUPPLY

A software-controlled switch allows conservation of the backup supply when data retention is not required. The switch is controlled by the same method described for refresh except that the bit pattern is different. On the initial application of the battery, the battery backup switch will be off. The bit patterns shown in Figure 2 turn on or off this switch which connects or disconnects the backup supply.

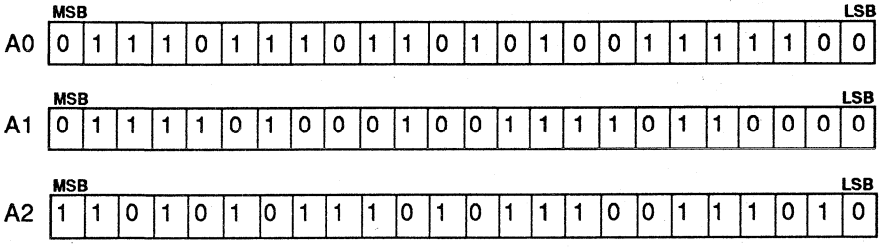
NOTE: On the initial connection of the battery, the battery backup switch will be off.

REFRESH INTERVALS Table 1

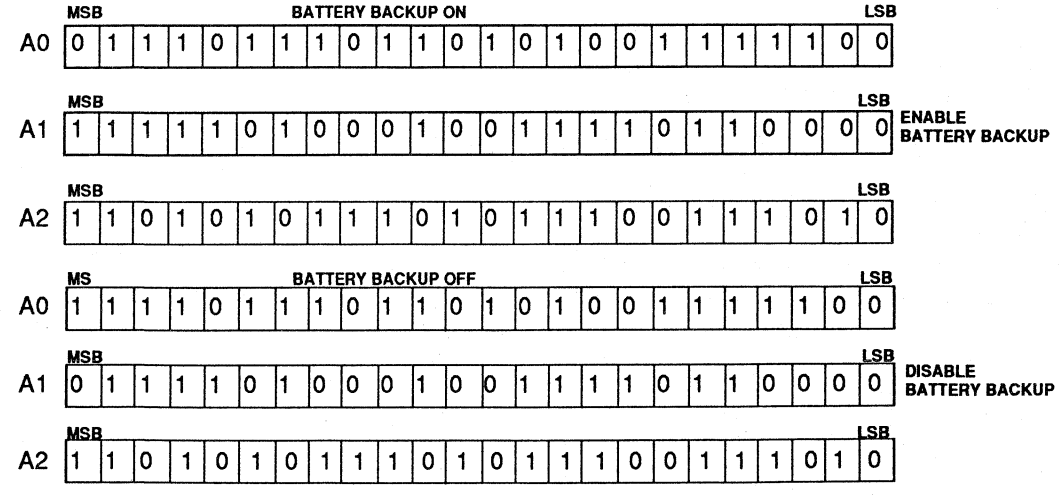
	REFRESH INTERVAL*			
NUMBER OF CYCLES	8	16	32	64
256K DRAM: 520	-1	-2	-3	-4
1 Meg DRAM: 1032	-5	-6	-7	-8

*Refresh intervals have a tolerance of +0/-12.5%.

SOFTWARE SWITCH FOR PROCESSOR CONTROL ON POWER-UP Figure 1



SOFTWARE CONTROLLED SWITCH FOR ACTIVATION OF BACKUP SUPPLY Figure 2



BATTERY CONDITION

The DS1237 has two features which provide information about the condition of the backup supply. First, the DS1237 monitors the backup supply input condition. If this input is below V_{CCI}, the backup condition output pin (BC\) is driven to the active state (low) and will remain in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CC} is applied within nominal limits. Whenever the backup supply is supplying power, the BC\ pin remains at a logic zero state. The second feature for monitoring the condition of the backup supply is a counter which is decremented on one second intervals whenever the backup supply is supplying power. This counter is set with a number while V_{CC} is within nominal limits. The value of the counter is entered by sending a 24-bit sequence on address lines A0, A1, and A2 in the same manner as described for refresh control. This sequence is shown in Figure 3. After the 24-bit sequence is correctly entered, the next 24 bits will define the time count in seconds which will start decrementing down when the backup supply is supplying power. This count is 24 bits long and is entered LSB first on address line A0 when the CAS line goes low. The counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the BC\ pin will be low even though the V_{CC} supply is within nominal limits. The BC\ pin will remain low until a new value is entered into the counter. This time can be calculated by dividing the capacity in ampere hours of the backup supply by the average load current of the DRAMs and converting this value into seconds (see Figure 5). The value in the counter can be read at any time while V_{CC} is within nominal limits by sending the 24-bit sequence which is shown in Figure 4. This sequence is entered in the same manner as described for refresh control. After this sequence is correctly entered, the next 24 CAS\ cycles will cause the contents of the counter to be shifted out one bit at a time starting with the LSB on the BC\ pin. A logic zero on BC\ while CAS\ is low is a logic zero for that bit.

BACKUP CONDITION APPLICATIONS

The backup condition features of the DS1237 can supply the system valuable information about the backup supply. A simple application may only use the V_{CC} comparator to tell the system that a battery is weak and should be replaced. A more sophisticated system may use the backup condition counter to measure the time that a primary battery is used to supply power to DRAMs. By knowing the capacity of the battery and the requirements of the DRAM, the time for battery replacement can be predicted. In fact, if worst case primary supply outages can be estimated, the backup battery can be selected so that replacement can always occur prior to backup supply failure. If a rechargeable backup supply is used, such as a capacitor or a nicad battery, the backup condition counter can be used to measure both the charge and discharge time. Charge time can be measured by using a system time base and periodically adjusting the battery condition counter under software control to reflect the amount of time (amount of charge) that the system primary power is within nominal limits.

NOTE:

The DS1237 requires capacitive bypassing techniques between V_{CCO} and GND for proper operation. A bypass capacitor between V_{CCI} and BKUP is also essential for proper operation. While applications vary, a 10 uf capacitor value is typically required.

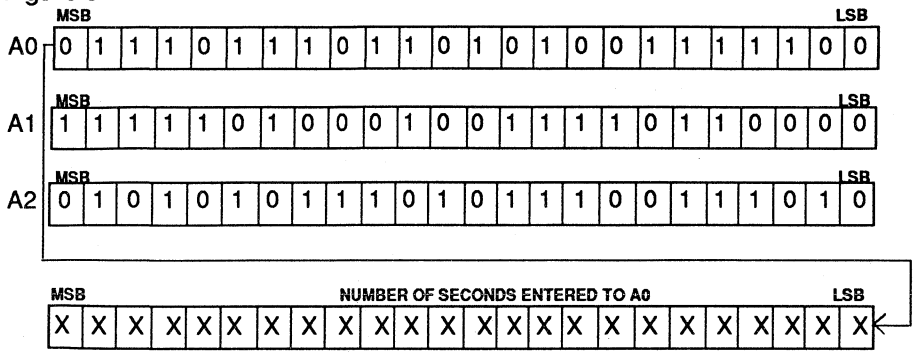
DATA RETENTION TIMES

The equations in Figure 5 are used to find the data retention time of DRAMs using the DS1237 DRAM Nonvolatizer Chip.

Calculating the actual current consumption of the DRAMs requires special attention since they are placed into the standby mode and then activated only when refreshing is required. This implies that the current draw of the DRAMs will be an average of the standby current and the active currents in direct proportion to the refresh cycle time and duration.

SOFTWARE SEQUENCE FOR SETTING THE BACKUP CONDITION COUNTER

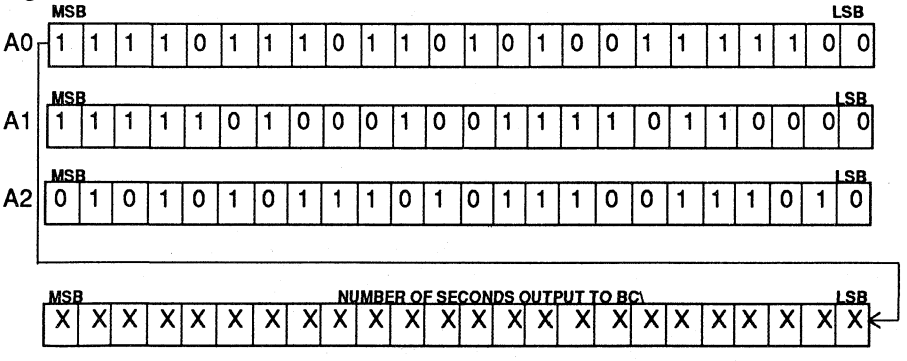
Figure 3



NOTE:
The binary count which is entered into the backup condition counter is a calculated value based on application and has a range of 2^{24} seconds with an accuracy of +/- 20%.

SOFTWARE SEQUENCE FOR READING THE BACKUP CONDITION COUNTER

Figure 4



DS1237 NONVOLATIZER DRAM DATA RETENTION TIMES Figure 5

$I_{datareten}$ = (# of DRAMs) x [(I_{act} + I_{std}) / $8e^{-3}$] + 4 mA

where,

I_{act} = 520 x $350e^{-9}$ x I_{active}
- 520 => number of refresh cycles (burst)
- $350e^{-9}$ => access cycle time of DRAM, and
- I_{active} => active current draw of DRAM

I_{std} = ($8e^{-3}$ - (520 x $350e^{-9}$)) x $I_{standby}$
- $8e^{-3}$ => refresh period
- 520 => number of refresh cycles (burst)
- $350e^{-9}$ => access cycle time of DRAM, and
- $I_{standby}$ => standby current draw of DRAM

The forgoing equations can then be used to directly calculate the data retention time:

$t_{datareten} = Q_{bat} / I_{datareten}$

ABSOLUTE MAXIMUM RATINGS *

Voltage on Battery Input Pins Relative To Ground	-0.3V to +12V
Voltage on any Other Pin Relative to Ground	-0.3V to +7V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	Volts	1
Voltage Input Logic 1	V_{IH}	2.0		V_{CC}+0.3V	Volts	1
Voltage Input Logic 0	V_{IL}	-0.3		+0.8	Volts	1
Backup Supply	BKUP	6.0V	8.0V	10.0	Volts	2,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.50V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-2.0			mA	1,5
Output Current @ 0.4 V	I_{OL}	+8.0			mA	1,5
Input Supply Current	I_{CCI}		3	7	mA	6
Output Supply Current $V_{CCO}=V_{CCI}$ -0.2 V	I_{CCO}			200	mA	4
PF\ Detect TOL = V_{CCO}	V_{TP}	4.5	4.62	4.75	V	7
PF\ Detect TOL = GND	V_{TP}	4.25	4.37	4.5	V	7
Output Supply Current $V_{CCI} < V_{TP}$	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUP}			1	uA	9

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	COND.	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	7		pF	

AC ELECTRICAL CHARACTERISTICS - RAPID REFRESH

(0° to 70°C, $V_{CCI} < V_{TP}$)

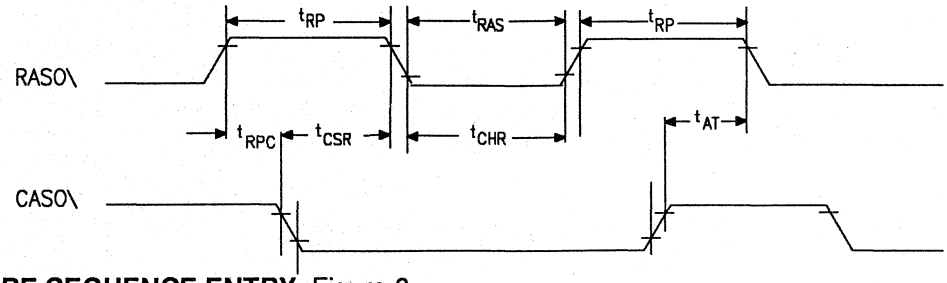
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RASO\ Precharge Time	t_{RP}	90			ns	
RASO\ Precharge to CASO\ Hold Time	t_{RPC}	60			ns	
CASO Setup Time	t_{CSR}	30			ns	
CASO\ Hold Time	t_{CHR}	60			ns	
RASO\ Pulse Width	t_{RAS}	0.120		10	us	
Elapsed Time Between Rapid Refresh Burst	t_{AT}	SEE TABLE 1			ns	

AC ELECTRICAL CHARACTERISTICS

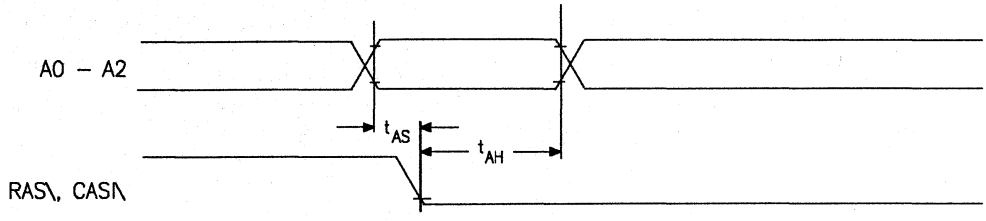
(0°C to 70°C, $V_{CCI} > V_{TP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	t_{AS}	0			ns	
Address Hold Time	t_{AH}	20			ns	
Propagation Delay	t_{PD}		7	15	ns	

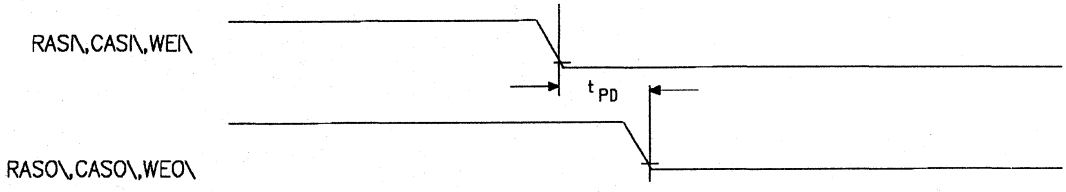
REFRESH CYCLE DURING BURST REFRESH RETENTION (WEO=V_{IH}) Figure 5



SOFTWARE SEQUENCE ENTRY Figure 6



PROPAGATION DELAY - NORMAL OPERATION Figure 7



NOTES

1. All voltages are referenced to ground.
2. The BC\ pin will be driven active whenever V_{CC} is within nominal limits and the backup supply is below V_{CC}.
3. Backup input voltage is internally regulated within the DS1237 such that V_{CCO} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1237 can supply to RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 300 pF.
6. Measured with all outputs open.
7. V_{TP} is the trip point where the internal switching circuits disconnect V_{CCI} and connect the internally regulated backup supply to V_{CCO}. Rapid refresh is also initiated at this time, and the PF\ output is driven active.
8. I_{CCOB} is the maximum current the DS1237 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage is the internal current consumed by the DS1237 in the data retention mode, with battery backup disabled.

APPLICATION NOTE: DIODE CONTROL OF BKUP INPUT

The fabrication of the DS1237 produces an N well for the BKUP input (pin 14) that must be considered by the user. Because of this it is imperative that the BKUP input does not go more negative from V_{CCI} input (pin 16) than the amount of one silicon diode.

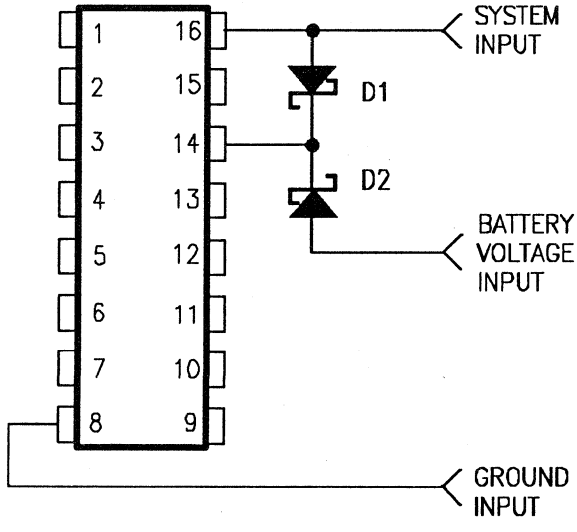
This requirement can be achieved by using a Schottky diode (D1) between the V_{CCI} input and BKUP input (see example below). This diode will limit the negative voltage level of BKUP input relative to the V_{CCI}.

A Shottky diode is required for D1.

Eventually the battery voltage that is applied to the BKUP input can decrease below the negative clamp voltage of D1. At this time, the battery should be disconnected from the circuit during the time that V_{CCI} input is present.

This can be achieved by using a diode (D2) between the battery positive supply lead and the BKUP input. Diode D2 will then disconnect the battery positive suply lead from the BKUP input when the battery output voltage has decreased.

A Shottky diode is suggested for D2.



NOTE: For circuits where the BKUP source is a primary battery, Underwriter Laboratories requires D2.

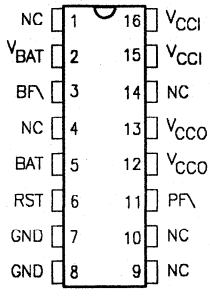
DALLAS SEMICONDUCTOR

DS1259/S
Battery Manager Chip

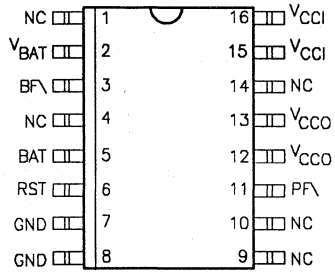
FEATURES

- Facilitates uninterruptible power
- Uses battery only when primary V_{CC} is not available
- Low forward voltage drop
- Power fail signal interrupts processor or write protects memory
- Consumes less than 100 nA of battery current
- Low battery warning signal
- Battery can be electrically disconnected upon command
- Battery will automatically reconnect when V_{CC} is applied
- Mates directly with DS1212 Nonvolatile Controller x 16 Chip to back up 16 RAMs
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



16-Pin DIP Package
(300 mil)



16-Pin SOIC Package
(300 mil)

PIN NAMES (\ Denotes Condition Low)

NC	- No Connection
V_{BAT}	- Battery Input Connection
BF\	- Battery Fail Output Signal
BAT	- Battery Output
RST	- Reset Ground Signal
GND	- Ground
PF\	- Power Fail Output Signal
V_{CCO}	- RAM Supply
V_{CCI}	- +5V Supply

DESCRIPTION

The DS1259 Battery Manager Chip is a low-cost battery management system for portable and nonvolatile electronic equipment. A battery connected to the battery input pin supplies power to CMOS electronic circuits when primary power is lost through an efficient switch via the V_{CCO} pins. When power is supplied from the battery, the power fail signal is active to warn electronic reset circuits of the power status. Energy loss during shipping and handling is avoided by pulsing reset, thereby causing the battery to be isolated from other elements in the circuits.

OPERATION

During normal operation, V_{CCI} (Pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (Pins 12 and 13) through an internal switch at a voltage level of V_{CCI}-0.2 volts at 250 mA. During this time the power fail signal (PF\) is held high, indicating valid V_{CCI} voltage (see Figure 1). However, if the V_{CCI} falls below the trip point (V_{TP}), a level of 1.26 times the battery level (V_{BAT}), the power fail signal is driven low. As V_{CCI} falls below the battery level, power is switched from V_{CCI} to V_{BAT} and the battery supplies power to the uninterruptible output (V_{CCO}) at V_{BAT}-0.2 volts at 15 mA.

On power-up, as the V_{CCI} supply rises above the battery, the primary energy source, V_{CCI}, becomes the supply. As V_{CCI} rises above the trip point (V_{TP}), the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level regardless of the level of V_{CCI}.

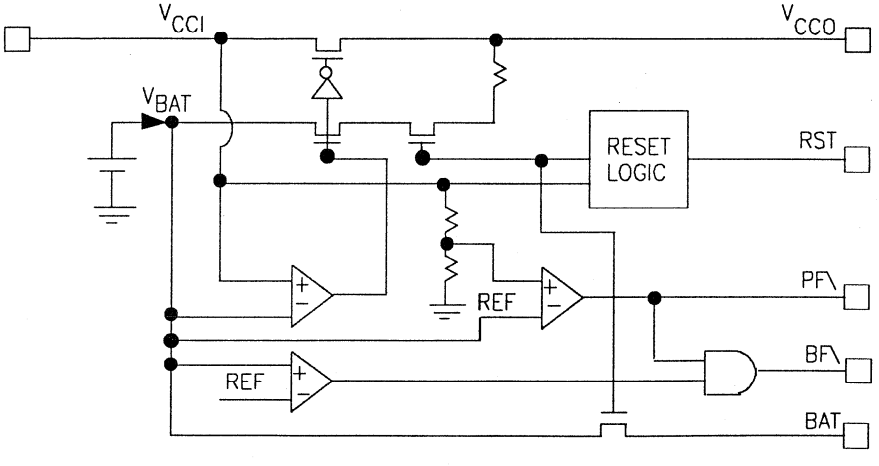
BATTERY FAIL

When power is being supplied from the primary energy source, BF\ (Pin 3) is held at a high level provided that the attached battery (V_{BAT}) is greater than 2 volts. If the battery level should decrease to below 2 volts, the BF\ signal is driven low, indicating a low battery. The BF\ signal is always low when the PF\ signal is low.

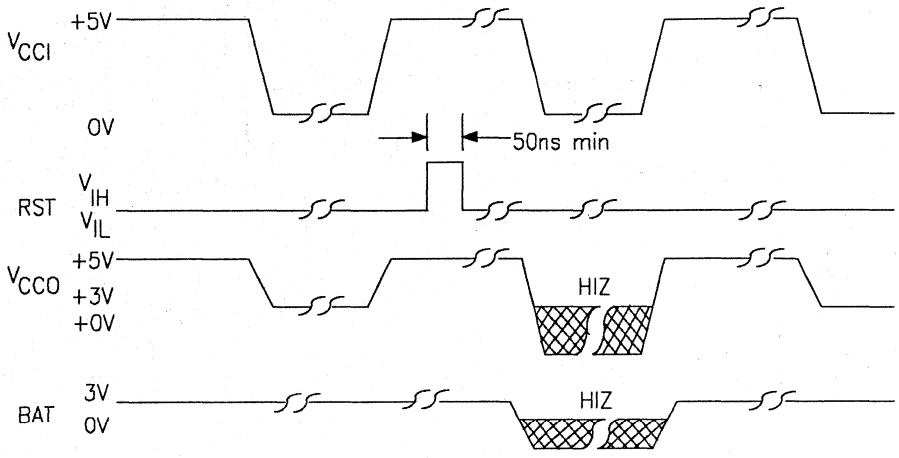
RESET

The reset input can be used to prevent the battery from supplying power to V_{CCO} and BAT even if V_{CCI} falls below the level of the battery. This feature is activated by applying a pulsed input on RST to high level for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the battery or V_{CCI}. The BAT output will also return to the level of the battery. Figure 3 shows the DS1259 in a typical application.

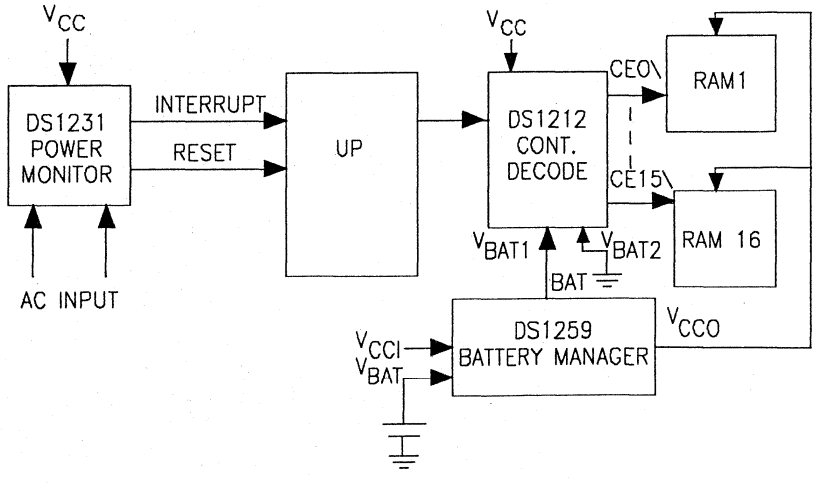
BLOCK DIAGRAM Figure 1



RESET TIMING Figure 2



TYPICAL APPLICATION Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}		5	5.5	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Battery Voltage Pin 2	V_{BAT}	2.5	3	3.7	V	6
Battery Output Pin 5	BAT	V_{BAT}- 0.1			V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5 to 5.5V)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			10	mA	3
Pins 12, 13 V_{CCO}=V_{CCI}-0.2	I_{CCO}			250	mA	
Pin 11 PF\ Detect	V_{TP}		1.26xV_{BAT}		V	4,6
Pin 3 BF\ Detect	V_{BATF}		2.0		V	7

(0°C to 70°C, V_{CCI} < V_{BAT})

PARAMETER	SYMBOL	TYP	MIN	MAX	UNITS	NOTES
Pins 12, 13 V_{CCO}=V_{BAT}-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8
Pin 5 Battery Output Current	I_{BAT}OUT			100	uA	

CAPACITANCE

(t_A = 25°C)

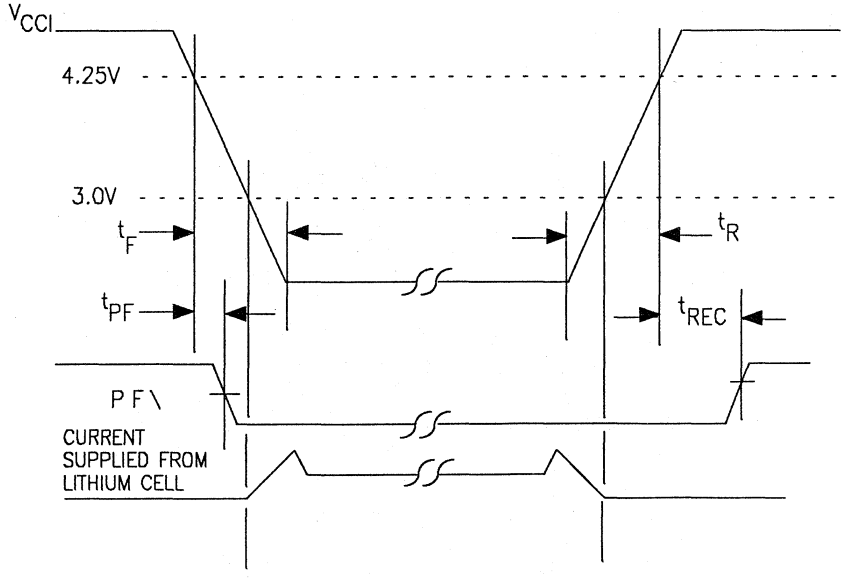
PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Output Capacitance	C_{OUT}	5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{CCI} Slew Rate	t_F	300			us
V_{CCI} Slew Rate	t_R	1			us
Power-Down to PF\ Low	t_{PF}	0			us
PF\ High after Power-Up	t_{REC}			100	us

POWER-DOWN/POWER-UP CONDITION



NOTES:

1. All voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13, and 3 open.
4. V_{TP} is the point that PF\ is driven low.
5. I_{CCO2} may be limited by the capability of the battery.
6. Trip Point Voltage for Power Fail Detect:
   V_{TP} = 1.26 x V_{BAT}
   For 5% operation: V_{BAT} = 3.7V Max.
7. V_{BATF} is the point that BF\ is driven low.
8. Battery leakage is the internal energy consumed by the DS1259.

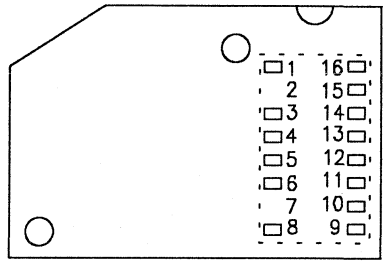
DALLAS SEMICONDUCTOR

DS1260
SmartBattery

FEATURES

- Encapsulated lithium energy cell with shelf life beyond 10 years
- Available with energy capacities of 250, 500, and 1,000 mAH @ 3 volts
- Plugs into a standard 16-pin DIP socket
- Lithium cell electrically disconnects from exposed pins upon command
- Battery isolation ensures full capacity after shipping and handling
- Lithium cell automatically reconnects when V_{CC} is applied
- Recessed pins prevent bending
- V_{CC} fail signal interrupts processor or write protects memory
- Exhausted energy cell warning signal
- Low profile permits mounting on 0.5-inch printed circuit board centers
- Mates directly with DS1212 Nonvolatile Controller to back up 16 SRAMs
- Uninterruptible supply for CMOS and portable devices

PIN DESCRIPTION



PIN NAMES
(\ Denotes Condition Low)

Pins 1, 4, 9, 10, and 14 are No-Connects
Pins 2 and 7 are missing
Pin 3 is Battery Fail (BF\)
Pin 5 is Battery Out (BAT)
Pin 6 is RESET (RST)
Pin 8 is Ground
Pin 11 is Power Fail (PF\)
Pins 12 and 13 are RAM Supply (V_{CCO})
Pins 15 and 16 are +5V Supply (V_{CCI})

DESCRIPTION

The DS1260 SmartBattery is a low-cost, backup energy supply for portable and nonvolatile electronic equipment. A lithium energy source of up to 1 amp hour can supply power to CMOS electronic circuits when primary power is lost through an intelligent and efficient switch. When power is supplied from the lithium power source, the power fail signal is held low to warn electronic RESET circuits of the power status. Energy loss during shipping and handling is avoided by pulsing RESET, thereby causing the backup energy source to be isolated from the exposed pins. The DS1260 can be plugged into a standard 16-pin, low-cost DIP socket, allowing for proven interconnect and simple replacement if the energy has been exhausted.

OPERATION

During normal operation V_{CCI} (pins 15 and 16) is the primary energy source and power is supplied to V_{CCO} (pins 12 and 13) through an internal switch at a voltage level of V_{CCI} -0.2 volts @ 250 mA. During this time the power fail signal (PF\) is held high, indicating valid primary voltage (see Figure 1). However, if the V_{CCI} falls below the level of 4.25 volts, the power fail signal is driven low. As V_{CCI} falls below the level of the lithium supply (V_{BAT} = 3 volts), power is switched and the lithium energy source supplies power to the uninterruptible output (V_{CCO}) at V_{BAT} -0.2 volts @ 5 mA.

On power-up, as the V_{CCI} supply rises above 3 volts, the primary energy source, V_{CCI}, becomes the supply. As the V_{CCI} input rises above 4.25 volts, the power fail signal is driven back to the high level. During normal operation, BAT (Pin 5) stays at the battery level of 3 volts, regardless of the level of V_{CCI}.

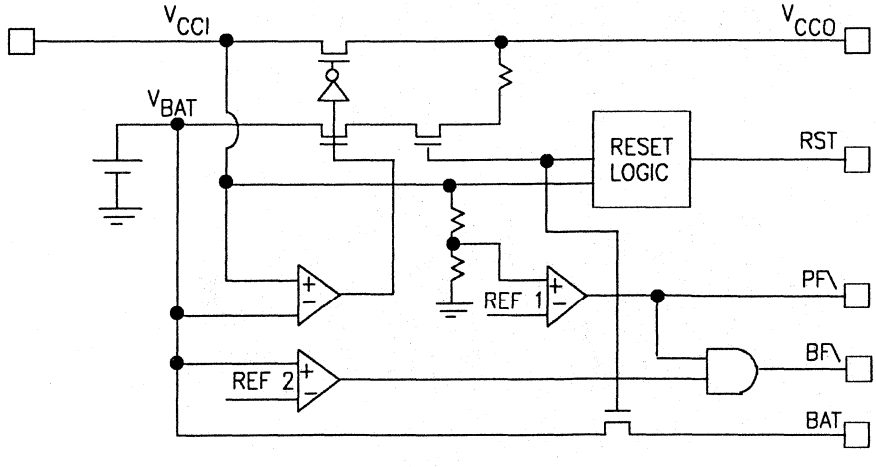
BATTERY FAIL

When power is being supplied from the primary energy source, BF\ (Pin 3) is held at a high level (V_{OH}) provided that the lithium energy source is greater than 2 volts. If the lithium energy source should decrease to below 2 volts, the BF\ signal is driven low (V_{OL}), indicating an exhausted lithium battery. The BF\ signal is always low when power is being supplied by the lithium energy source.

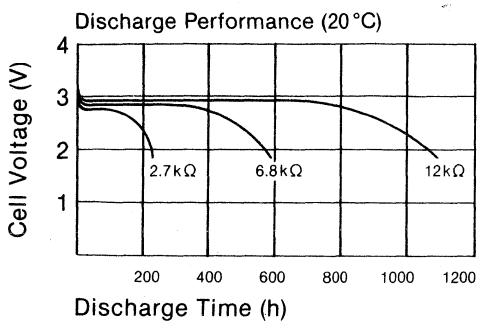
RESET

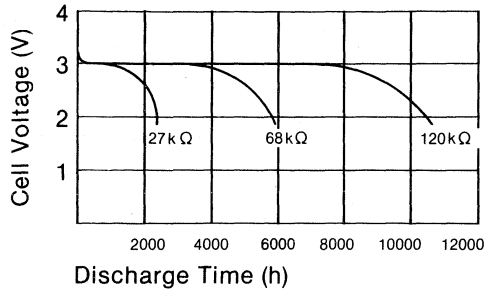
The reset input can be used to prevent the lithium energy source from supplying power to V_{CCO} and BAT even if V_{CCI} falls below 3 volts. This feature is activated by applying a pulsed input on RST to a high level (V_{IH}) for 50ns minimum while primary power is valid (see Figure 2). When primary power is removed after pulsing RST, the V_{CCO} output and BAT will go to high impedance. The next time primary power is applied such that V_{CCI} is greater than V_{BAT}, normal operation resumes and V_{CCO} will be supplied by the lithium energy source when V_{CCI} again falls below 3 volts. BAT will also return to the level V_{BAT}. Figure 3 shows how the SmartBattery is used in a system application.

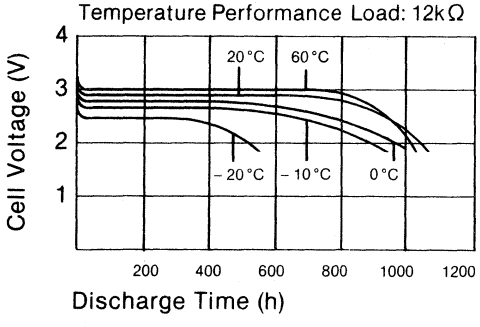
BLOCK DIAGRAM Figure 1

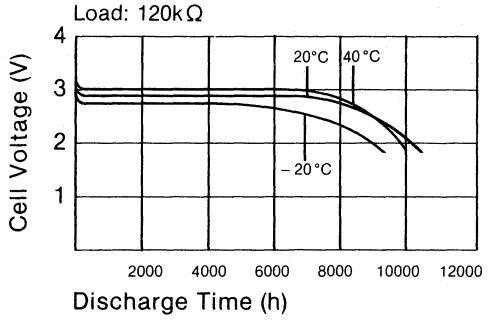


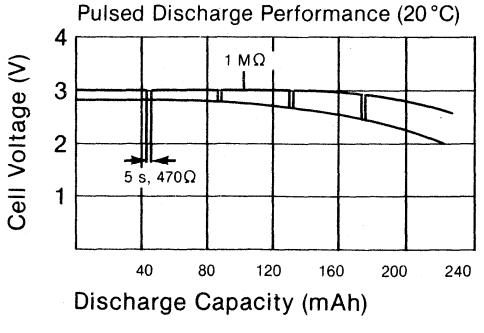
BATTERY PERFORMANCE DS1260-25



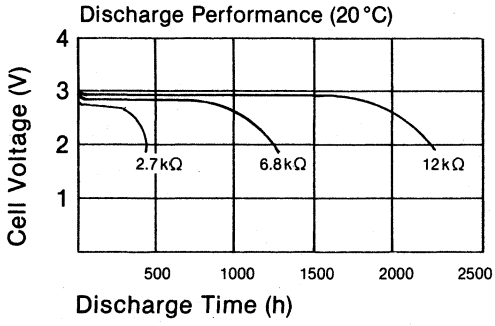


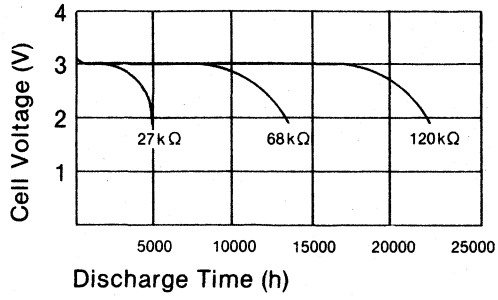


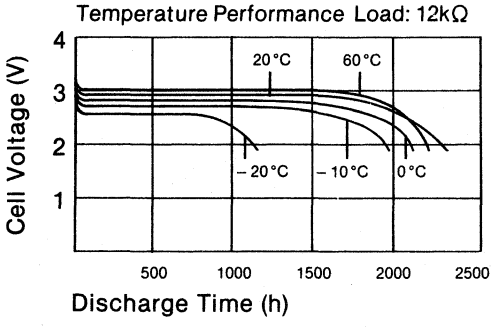


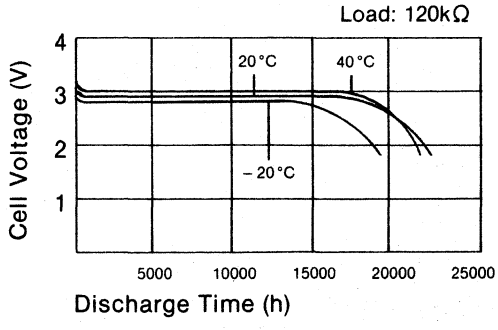


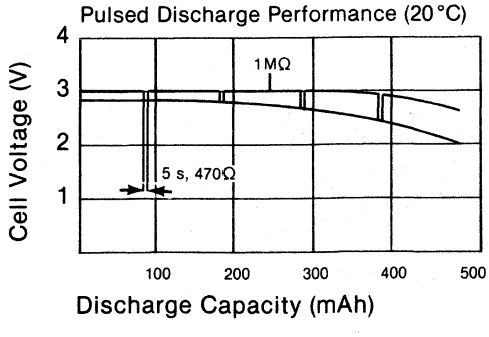
BATTERY PERFORMANCE DS1260-50





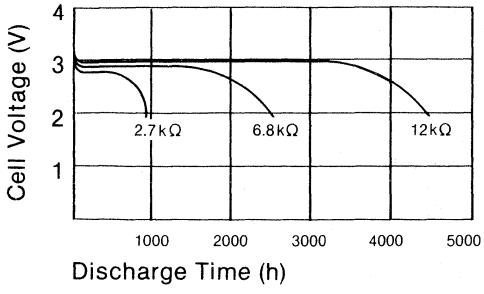


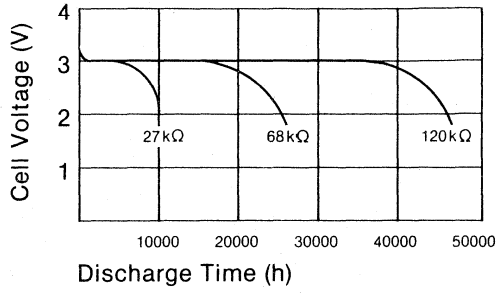




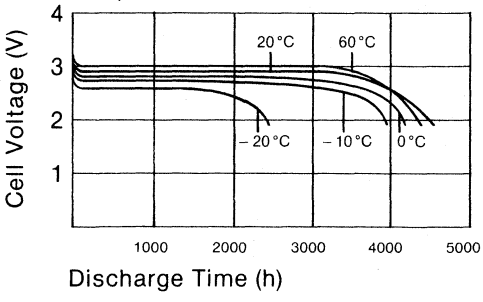
BATTERY PERFORMANCE DS1260-100

Discharge Performance (20 °C)

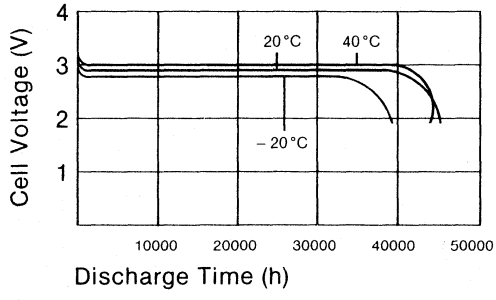




Temperature Performance Load: 12kΩ



Load: 120kΩ



Pulsed Discharge Performance (20 °C)

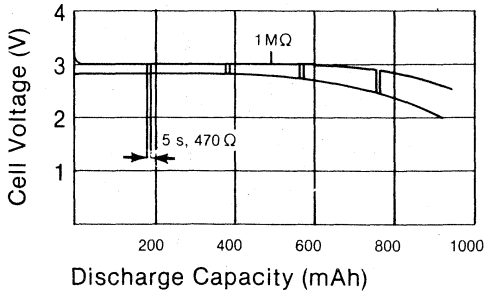
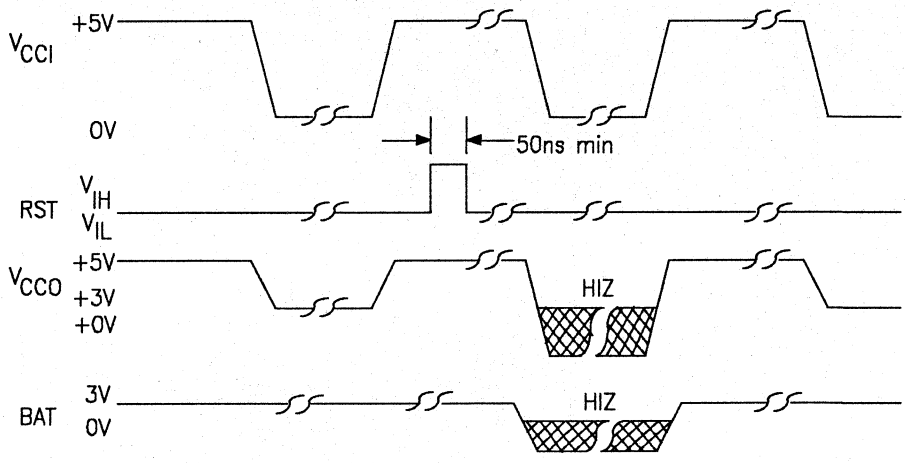


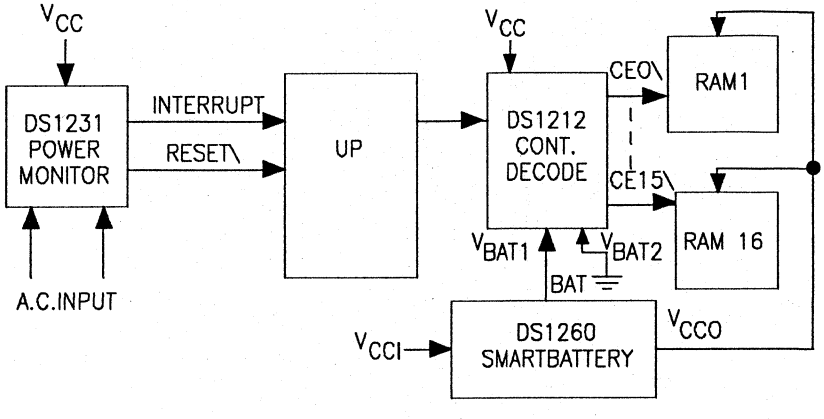
TABLE 1

PART NO.	CAPACITY	NOMINAL VOLTAGE
DS1260-25	250 mAH	3 volts
DS1260-50	480 mAH	3 volts
DS1260-100	960 mAH	3 volts

RESET TIMING Figure 2



INTEGRATED BATTERY BACKUP—APPLICATIONS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -40°C to +70°C
Soldering Temperature 260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.0		VCCI+0.3	V	1
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CCI}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1, 2
Output Current @ 0.4V	I_{OL}			+4.0	mA	1, 2
Input Supply Current	I_{CCI}			5	mA	3
Pins 12, 13 V_{CCO}=V_{CCI}-0.2	I_{CCO}			250	mA	
Pin 11 PF\ Detect	V_{TP}		4.25	4.5	V	4
Pin 3 BF\ Detect	V_{BATF}		2.0		V	7

(0°C to 70°C; $V_{CCI} < V_{BAT}$)

Pin 5 Battery Voltage	V_{BAT}		3		V	6
Pins 12, 13 V_{CCO}=V_{BAT}-0.2V	I_{CCO2}			15	mA	5
Battery Leakage	I_{BAT}			100	nA	8, 9
Pin 5 Battery Output Current	I_{BAT}OUT			100	uA	

CAPACITANCE

(t_A = 25°C)

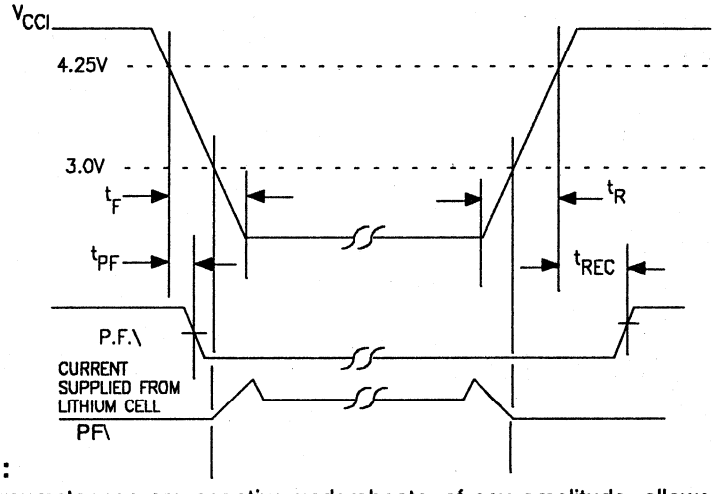
PARAMETER	SYMBOL	TYP	MAX	UNITS
Output Capacitance	C_O	5	10	pF
Input Capacitance	C_I	5	10	pF

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}=4.0 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{CCI} Slew Rate	t_F	300			us
V_{CCI} Slew Rate	t_R	1			us
Power-Down to PF\ Low	t_{PF}	0			us
PF\ High after Power-Up	t_{REC}			100	us

POWER-DOWN/POWER-UP CONDITION



WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

NOTES:

1. Voltages are referenced to ground.
2. Load capacity is 50 pF.
3. Measured with Pins 11, 12, 13, and 3 open.
4. V_{TP} is the point that PF\ is driven low.
5. Sustained I_{CCO2} currents above 1 mA cause a significant drop in battery voltage.
6. V_{BAT} is the internal lithium energy source voltage.
7. V_{BATF} is the point that BF\ is driven low.
8. Battery leakage is the internal energy consumed by the DS1260.
9. Storage loss is less than 1% per year at 25°C.
10. V_{CCI} = +5 volts; t_A = 25°C.

DALLAS SEMICONDUCTOR

DS1262
Serial DRAM Nonvolatizer Chip

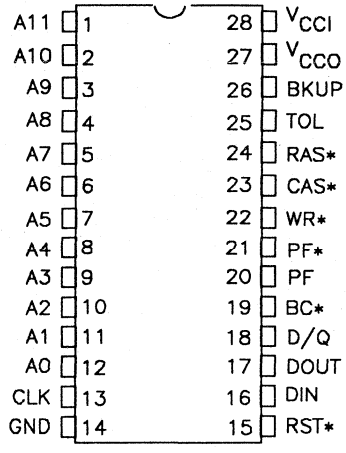
FEATURES

- Provides 3-wire serial access to DRAM
- Converts DRAM into nonvolatile memory using external backup supply
- Addresses up to 16Mx1 of memory
- Data can be read from or written to DRAM via single- or multi-bit transfers
- Onboard delay line generates precise DRAM timing signals
- Automatic CAS-before-RAS refresh in active and data retention modes
- Gas gauge for backup supply warns of impending data retention failure
- Selectable refresh periods: 4, 8,16, or 32 ms
- Power fail detection signals provide hardware interrupt to host
- Backup supply range of 6 to 10 volts
- Power fail detect at 5% and 10% of V_{cc}
- 28-pin DIP and SOIC (DS1262S) packages available

DESCRIPTION

The DS1262 Serial DRAM Nonvolatizer Chip enables read/write access of DRAM from a simple 3-wire serial port. Refresh and RAS/CAS timing for the DRAM is performed automatically, transparent to the operation of the serial port. In addition, the DS1262 performs all of the power switching and refresh duties necessary to retain DRAM data when the primary power supply fails. The backup supply input accepts a wide voltage range, suitable for use with rechargeable batteries. The DS1262 also provides an electronic "gas gauge" which can predict the condition of the backup supply. It can be used with DRAM densities of 256Kx1 to 16Mx1.

PIN DESCRIPTION



28-PIN DIP
(600 Mil.)

PIN NAMES (* Denotes Condition Low)

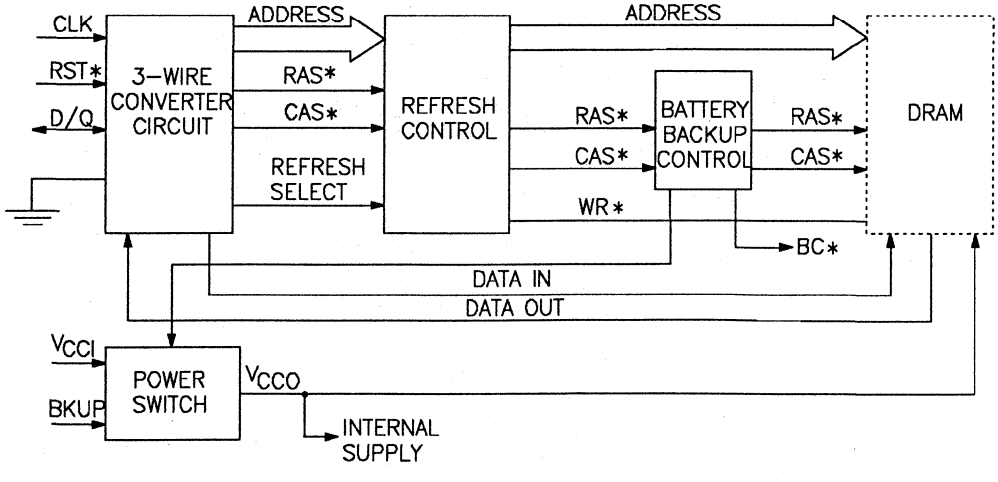
A0 - A11	Address Outputs to DRAM
DIN	Data In from DRAM
DOUT	Data Out to DRAM
WR*	Write Signal to DRAM
RAS*	Row Address Strobe for DRAM
CAS*	Column Address Strobe for DRAM
V_{cci}	+5V Primary Supply
V_{cco}	V_{cc} Output for DRAM
CLK	Serial Clock Input
RST*	Serial Reset Input
D/Q	Serial Port Data I/O
BKUP	Backup Supply Input
TOL	5% or 10% V_{cc} Supply Select
BC*	Backup Supply Condition Pin
PF, PF*	Power Fail Signals
GND	Ground

OPERATION - SERIAL PORT INTERFACE

The main elements of the DS1262 are shown in Figure 1. Three signals control sending or retrieval of data using the 3-wire converter circuit. The signals CLK, RST*, and D/Q comprise a 3-wire serial port. To transfer data into the DS1262, RST* is first driven high while CLK is low. After sufficient setup time from RST*, one bit of data is placed onto the D/Q line. With valid data on D/Q the CLK line is then transitioned low to high. The CLK transition causes the first bit of data to be transferred into the 3- wire converter. Since the serial port can only accept data one bit at a time, address information must always be sent first to inform the 3-wire converter of the destination of the data that will follow. Address information is always entered starting with the least significant bit of the logical address field and ending with the most significant bit of the address field. Twenty-four address bits are always written to the 3-wire converter regardless of the RAM being used (Figure 2).

After the 24-bit address field is sent, an 8-bit function code is written to instruct the 3-wire converter of the action to be taken on data that will follow. The function codes are listed in Table 1. After a function code has been correctly entered, one or more data bits can be written to or read from the DRAM or the control registers within the battery backup control unit. Function codes that control the backup supply or refresh period cause further data transfer to terminate until RST* is driven low and then high again to begin a new cycle. Data is always written in the same manner as the address and function code information. Data is read by driving the clock low while RST* is high. Data becomes valid on the D/Q line after sufficient time is allowed for access. The read cycle is terminated when RST* is returned low.

DS1262 BLOCK DIAGRAM Figure 1



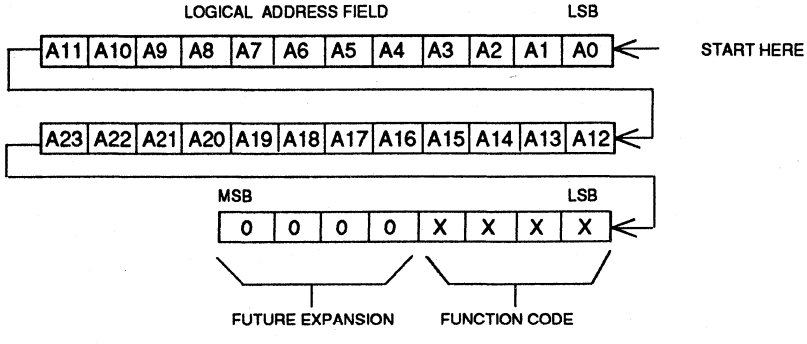
DRAM REFRESH CONTROL

Refresh cycles are always sent to the attached DRAM , regardless of activity on the serial port. When a proper DRAM read/write access code has been entered at the serial port, a normal DRAM read/write cycle will be interlaced with the refresh burst cycles. When V_{CCI} goes to an out-of-tolerance condition (see DC Electrical specifications for details), the DS1262 sends out 256 refresh cycles for each refresh period as selected by the user (4, 8, 16, or 32 msec). The 256 refresh cycles occur at a 500 ns rate for about 128 usec. All refresh cycles are the CAS-before-RAS type and are sufficiently long to meet the refresh requirements of most DRAM densities. After the refresh burst, the DS1262 remains quiet for the remainder of the refresh period to conserve power, except for DRAM read/write cycles initiated by the serial port.

BURST MODE

When it is necessary to retrieve or write multiple consecutive bits of data from the DRAM, burst read or burst write function codes can be used to minimize protocol overhead. In this mode, the starting memory address is entered in the address field. This field is then incremented for each new clock cycle. While low density DRAMs do not require the entire 24-bit address field, 24 bits must be always entered; unused upper address bits should always be the same value (0's are recommended). The DS1262 will always produce the appropriate RAS and CAS address. Burst mode is terminated when RST* is driven low. Each clock cycle for read or write operations is exactly the same as single bit transfers.

SERIAL PORT PROTOCOL Figure 2



FUNCTION CODES Table 1

FUNCTION NAME	FUNCTION CODE (HEX)
BURST READ DRAM DATA	00
READ DRAM DATA	01
READ BKUP COUNTER	02
WRITE BKUP COUNTER	03
REFRESH PERIOD=4 MSEC	04
REFRESH PERIOD=8 MSEC	05
REFRESH PERIOD=16 MSEC	06
REFRESH PERIOD=32 MSEC	07
BACKUP SUPPLY ENABLED	0C
BACKUP SUPPLY DISABLED	0D
WRITE DRAM DATA	0E
BURST WRITE DRAM DATA	0F,FF

DRAM TIMING - READ CYCLE

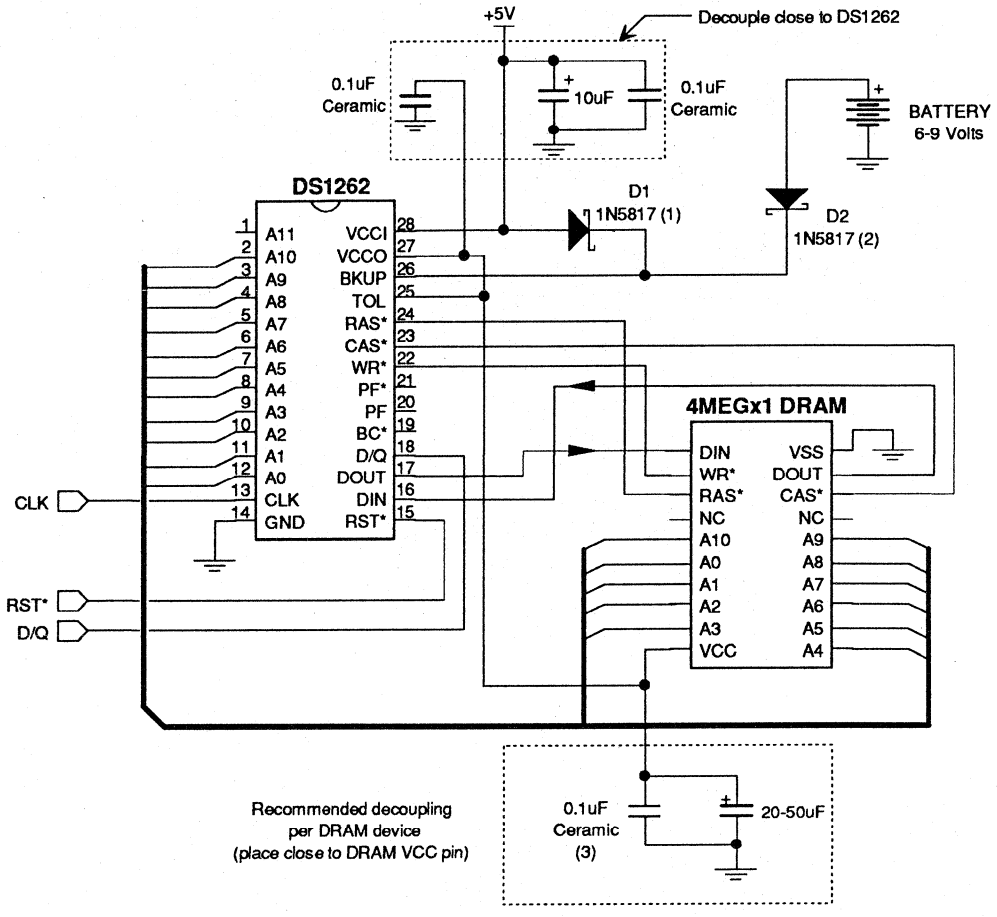
A read cycle is started when the row addresses are asserted valid on the address output pins of the DS1262 (A0 - A11). After sufficient setup time, the RAS* signal is asserted low and the row addresses are latched into the DRAM. Next the column addresses are asserted valid and after setup time the column address strobe (CAS*) goes active, latching the column address. The CAS* strobe will stay low for a sufficient time for valid data to be output and received from the DRAM at the DIN pin. The cycle is terminated when both RAS and CAS are returned high. The WR* signal is always high during the read cycle (see timing diagrams at the back of this data sheet). Unused upper address output pins should always beleft unconnected.

DRAM TIMING - WRITE CYCLE

A write cycle is started when the row addresses are asserted valid on the address output pins of the DS1262 (A0 - A11). After sufficient setup time, the RAS* signal is asserted low and the row addresses are latched into the DRAM. At the same time, valid data is placed on the data output pin (DOUT). Next the WRITE* signal is asserted low. At the same time, the column address is asserted valid on the address bus. After setup time the column address is asserted low.

All signals (RAS*, CAS*, A0-A11, WR*, and DOUT) remain active and valid until the write cycle is complete. The cycle is terminated when RA*, CAS*, and WR* are returned back high and the data out pin (DOUT) returns to a high impedance state.

DS1262 APPLICATION CIRCUIT WITH 4Mx1 DRAM Figure 3



NOTES:

1. BKUP input must not be allowed to go 0.7 volts more negative than V_{CCI}; otherwise an internal silicon diode in the DS1262 will short V_{CCI} to ground. D1 clamps BKUP so that it can only go 0.3 volts below V_{CCI}.

2. D2 prevents reverse-charging of battery and may be required for UL approval if battery source is the primary source for the user's system.

3. The decoupling capacitors attached to the DRAM V_{CC} input(s) are required because of the switching noise of the regulated V_{CCO} supply from the DS1262. Also, this capacitance satisfies fast rise-time current demands of the DRAM.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5-volt V_{CCI} power begins to drop, an internal precision band-gap reference and comparator senses this change. Depending on the level of the tolerance pin, a power fail signal will be generated if V_{CCI} falls below 4.75 volts or 4.5 volts. (See DC Electrical specifications for detail.) The power fail outputs (PF,PF*) are driven active at this time and will remain active until V_{CCI} is restored to a normal condition. When the data retention mode begins, the DS1262 isolates the 3-wire serial port, drives the address outputs low, and starts driving RAS*, CAS*, and the WR* outputs. If an active DRAM read/write cycle is in progress when power loss occurs, the DS1262 will complete this cycle properly before isolating the 3-wire serial port (RST*, CLK, D/Q). The V_{CCI} input is then disconnected from the V_{CCO} output and the backup supply connected to the BKUP pin is switched in. The BKUP input is normally connected to either a rechargeable battery or supercapacitor. However, any backup supply with a voltage output between the limits of 6 and 10 volts is suitable. If nonvolatile operation is not desired, the BKUP input should be left unconnected or tied to the VCCI pin; do not tie this pin low when not using the battery-backup function.

After power loss, a burst CAS-before-RAS refresh cycle is generated at a cycle time of 500 ns. This burst refresh continues for 256 cycles. After the burst refresh is complete, subsequent refreshing continues at intervals determined by the refresh period function code written.

BATTERY GAS GAUGE

The DS1262 contains two features that provide information about the condition of the backup supply. First, the DS1262 monitors the backup supply input condition. If this input is below V_{CCI} the backup condition output pin (BC*) is driven active low and remains in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CCI} is applied within nominal limits. Whenever the backup supply is providing power, the BC* pin remains in a high impedance state.

The second feature for monitoring the condition of the backup supply is a gas gauge circuit, consisting of a counter that is decremented at 1 second intervals whenever the backup supply is providing power. This counter is initialized with a number by the user while V_{CCI} is within normal limits. The value of the counter is set by entering the desired binary value in the logic address field, followed by a write battery condition function code. The value is entered starting with the LSB of the address field and ending with the MSB of the address field after the function code is correctly entered. Information in the address field is automatically entered into the battery condition counter when RST* is brought low to end the cycle. The battery condition counter value can only be entered when V_{CCI} is within normal limits. No other action will take place when using the write battery condition function code.

The battery condition counter can be read by loading the address field with any value followed by a read battery condition function code. After this function code is entered, the next 24 clock cycles will output the value of the battery condition counter on the D/Q line. The value of the battery condition counter can only be read when V_{CCI} is within normal limits. No other action will take place when a read backup condition function code is used. The backup condition counter is a binary number representing the time allowed until the backup supply has been discharged. When the counter reaches zero, the BC* pin will be driven low as soon as V_{CCI} is within normal limits. The BC* pin will remain low until a new value is written into the battery condition counter. The correct value to enter into the counter can be calculated by dividing the capacity in ampere-hours of the backup supply by the average load current of the DRAM and converting this value into seconds.

CONSERVATION OF THE BACKUP SUPPLY

Two other function codes are used to control a switch that allows conservation of the backup supply when data retention is not required. The switch is set on or off by entering any value in the address field followed by the function code for turning off or on the backup supply. The bit patterns are shown in Table 1. The backup supply switch can only be set when V_{CCI} is within normal limits. No other action will take place when using these function codes.

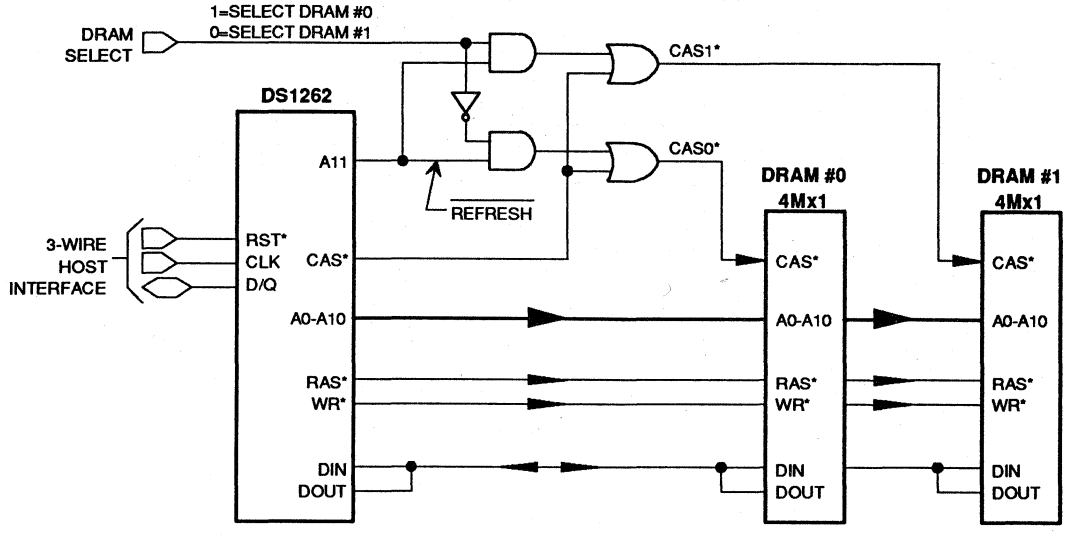
REFRESH PERIOD FUNCTION CODES

Four function codes are used to set the refresh period for the attached DRAM; all refresh periods contain 256 cycles. As such, most DRAMS will use 256 cycles per 4 msec refresh regardless of the density of the RAM attached. For example, a 1Mx1 DRAM requires 512 cycles in 8 ms while a 4Mx1 DRAM requires 1024 cycles in a 16 ms period. Both devices are satisfied using a 4 msec refresh period since a 4Mx1 DRAM is satisfied in 4 refresh periods (4 x 256 = 1024). However, extended refresh periods can be used in cases where DRAMS have been screened and tested for longer data retention between refresh bursts.

Whenever a function code is written to select the refresh period, the logic address field is ignored by the serial port and can be set to any value; however, all 24 address bits must entered. Function codes other than proper DRAM read / write codes do not cause any data to be written to the attached DRAM; the RST* pin must be reset low and then brought high to access the DRAM data after entering these codes. Data sent through the serial port after one of these functions codes is sent will be ignored until RST* is driven low and then high again to begin a new cycle.

Function codes for backup supply control or refresh control need only be written once after the BKUP supply is attached. The BKUP supply will preserve these codes as long it remains within specified limits.

BANK SELECT SCHEME FOR TWO 4Mx1 DRAMs Figure 4

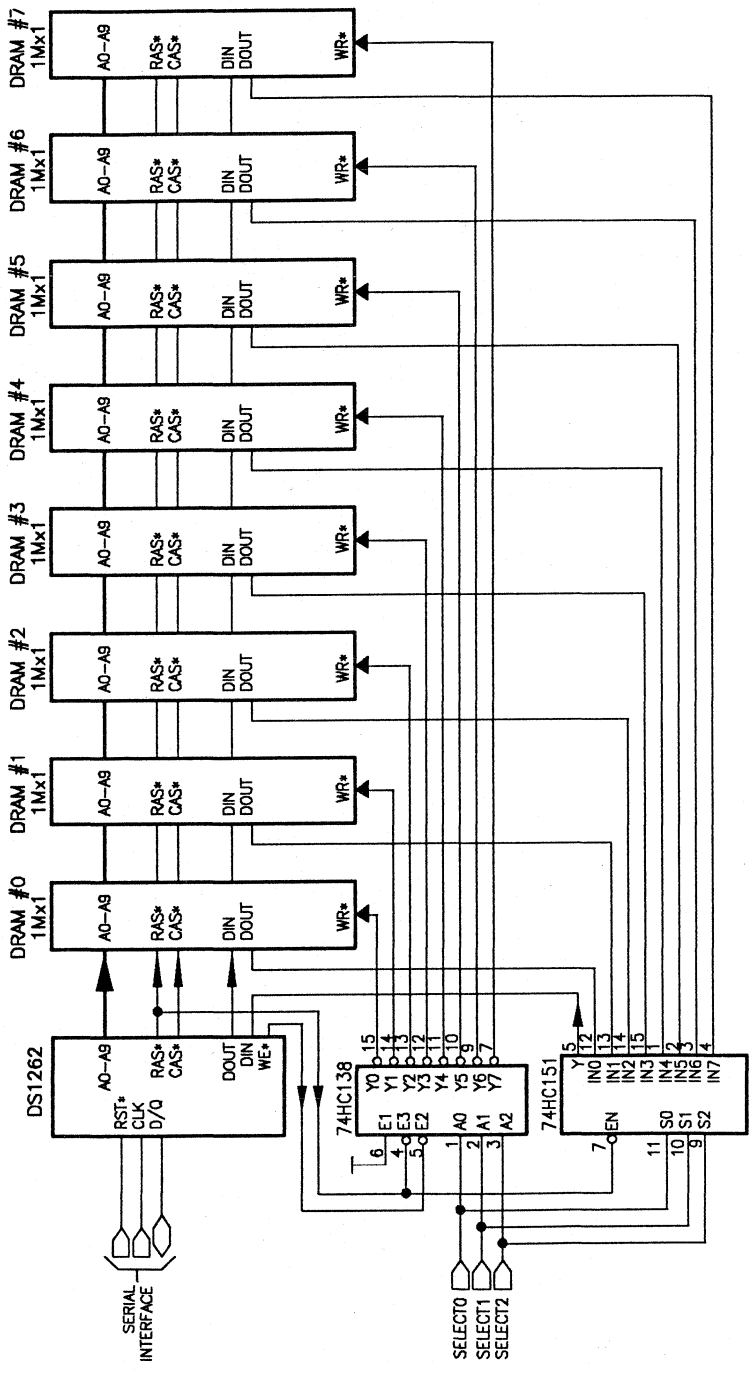


NOTES:

1. In this application, the A11 address output serves as a refresh indicator, going low whenever the DS1262 is in a refresh cycle. During refresh cycles, all address outputs are forced to the last row address state. Therefore, the user must program A23 = 0 and A22 = 1; that is, A23 maps to the row address output of A11 while A22 maps to the column address output of A11.

2. Caution must be taken to never program A23, A22 to any state other than 01 nor to allow the DS1262 to inadvertently reach this address in the burst read/write mode.

BANK SELECT SCHEME FOR EIGHT 1Mx1 DRAMs Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7V
Voltage on BKUP Pin Relative to Ground -0.3V to +12V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	Volts	1
Input Logic High	V_{IH}	2.0		V_{CC}+0.3	Volts	1
Input Logic Low	V_{IL}	-0.3		+0.8	Volts	1
Backup Supply	BKUP	5.5	8.0	10.0	Volts	1,2,3

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	uA	
DQ Leakage	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	1,5
Output Current @ 0.4V	I_{OL}	2.0			mA	1,5
Input Supply Current	I_{CCI}		3.0	7.0	mA	6
Output Supply Current $V_{CCO} = V_{CCI}$ - 0.2V	I_{CCO}			100	mA	4
TOL pin = V_{CCO}	V_{TP}	4.50	4.62	4.75	Volts	7
TOL pin = GND	V_{TP}	4.25	4.37	4.50	Volts	7
Output Supply Current $V_{CCI} < V_{TP}$	I_{CCOB}			30	mA	8
Backup Supply Leakage	I_{BKUPL}			2	uA	9
Backup Supply Quiescent	I_{BKUPQ}		2.0		mA	10

CAPACITANCE

PARAMETER	SYMBOL	COND.	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A = 25°C	5	7	pF	
Output Capacitance	C_{OUT}	t_A = 25°C	7	10	pF	
I/O Capacitance	$C_{I/O}$	t_A = 25°C	7	10	pF	

AC ELECTRICAL CHARACTERISTICS

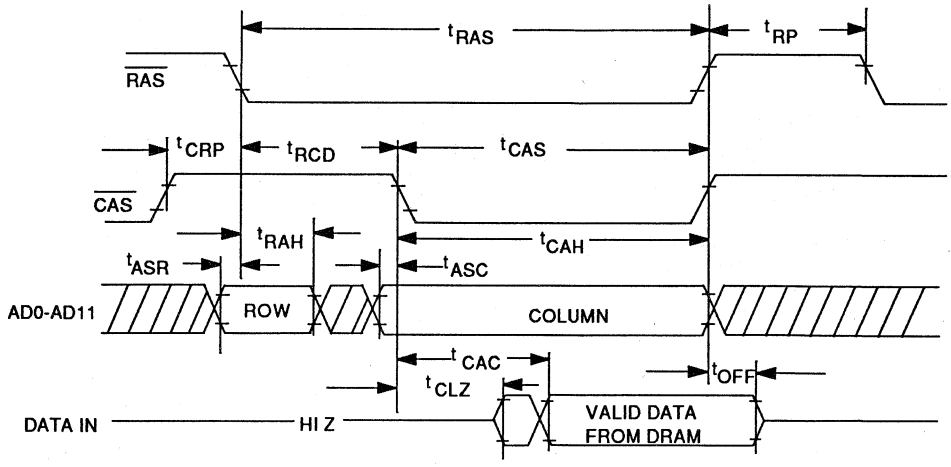
(t_A = 25°C, V_{CC} = 5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RAS* Pulse Width	t_{RAS}	250		350	ns	
RAS* Precharge	t_{RP}	150		200	ns	
CAS* to RAS* Precharge	t_{CRP}	150		200	ns	
RAS* to CAS* Delay	t_{RCD}	75		125	ns	
CAS* Pulse Width	t_{CAS}	125		275	ns	
Row Address Setup	t_{ASR}	30		150	ns	
Row Address Hold	t_{RAH}	25		50	ns	
Column Address Setup	t_{ASC}	5		25	ns	
Column Address Hold	t_{CAH}	125		175	ns	
Access Time From CAS*	t_{CAC}			100	ns	
CAS to Output In Low Z	t_{CLZ}				ns	1
Output Turn Off Delay	t_{OFF}				ns	1
RAS* to CAS* Precharge	t_{RPC}	10			ns	
CAS* Setup Time	t_{CSR}	10		50	ns	
CAS* Hold Time	t_{CHR}	250		350	ns	
Write Pulse Width	t_{WP}	150		300	ns	
Data Setup	t_{DS}	50			ns	
Data Hold	t_{DH}	125			ns	
D/Q to CLK Setup	t_{DC}	100			ns	
CLK to D/Q Delay	t_{CDD}			200	ns	
CLK Low Time	t_{CL}	500			ns	
CLK High time	t_{CH}	500			ns	
CLK Frequency	f_{CLK}	DC		1	MHz	
CLK Rise & Fall	t_R,t_f	3	10	20	ns	
RST* to CLK Setup	t_{CC}	1			us	
CLK to RST* Hold	t_{CCH}	200			ns	
RST* Inactive Time	t_{CWH}	1			us	
RST* to D/Q In High Z	t_{CDZ}			100	ns	

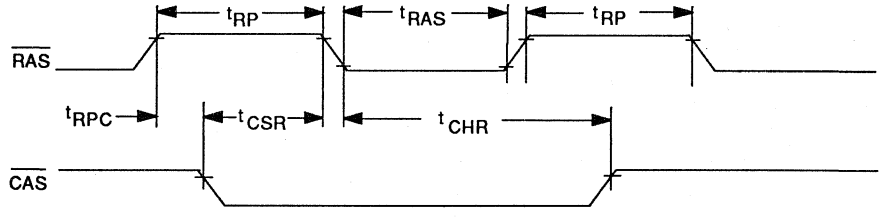
NOTE:

1. See RAM data sheet.

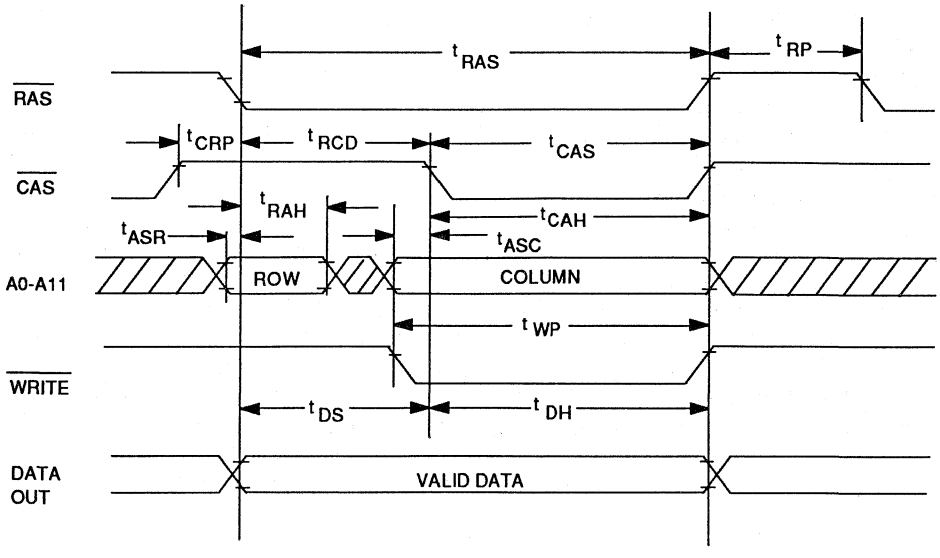
READ CYCLE FROM RAM (WR* = V_{OH}) Figure 6



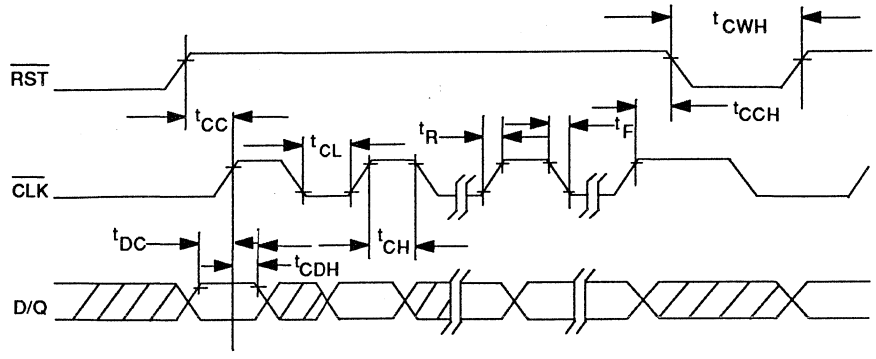
REFRESH CYCLE (WR* = V_{OH}) Figure 7



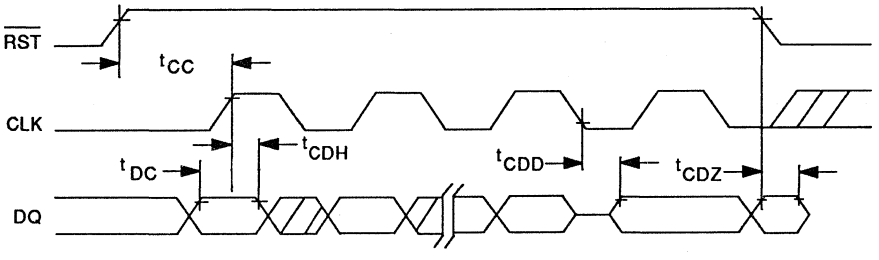
WRITE CYCLE OUTPUT TO RAM Figure 8



WRITE DATA TRANSFER FROM SERIAL PORT Figure 9



READ DATA TRANSFER FROM SERIAL PORT Figure 10



NOTES:

1. All voltages are referenced to ground.
2. The BC* pin will be driven active whenever V_{CCI} is within nominal limits and the backup supply is below V_{CCI}.
3. Backup input voltage is internally regulated within the DS1262 such that V_{CCI} is never below 4.5 volts for a backup input voltage of 6.0 volts minimum.
4. I_{CCO} is the maximum current which the DS1262 can supply RAM through the V_{CCO} pin with a voltage drop of less than 0.2 volts.
5. Load capacity is 100 pF.
6. Measured with all outputs open.
7. V_{TP} is the trip point where the internal switching circuits disconnects V_{CCI} and connects the internally regulated backup supply to V_{CCO}.
8. I_{CCOB} is the maximum current which the DS1262 can supply to RAM through the V_{CCO} pin from the internally regulated supply while in the data retention mode.
9. Backup leakage current is the current into the BKUP pin when the backup supply has been disabled (via the 0D function code) and the DS1262 is in the data retention mode (V_{CCI}=0V).
10. Backup quiescent current is the current consumed by the DS1262 when in the data retention mode and the backup supply is enabled. Total current into the BKUP pin in the data retention mode is this current plus the DRAM refresh current (see DRAM data sheet).

System Extension

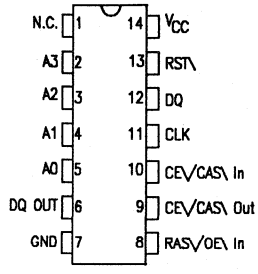
DALLAS SEMICONDUCTOR

DS1206
Phantom Serial Interface Chip

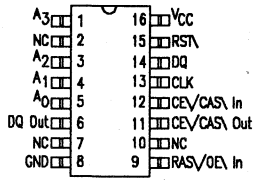
FEATURES

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory waveforms into a 3-wire serial port
- Operation is transparent to memory
- Software-generated memory cycles activate serial port and transfer data
- High bandwidth -- 1-bit data transfer per two memory cycles
- Intercepts memory signals so that pass-through connections to memory can be maintained
- Controls communications for as many as 10 DS1201 Electronic Tags, DS1204U Electronic Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low-power CMOS circuitry
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



14-PIN DIP (300 MIL)



16-PIN SOIC (300 MIL)

PIN NAMES (\ Denotes Condition Low)

NC	- No connection
A0-A3	- Memory address bus
DQ Out	- Data out to memory bus
GND	- Ground
RAS\ /OE\ In	- RAS\ input from memory bus
CE\ /CAS\ Out	- Chip enable or CAS\ from memory bus
CLK	- Clock for serial port
DQ	- Data I/O for serial port
RST\	- Reset for serial port
V_{CC}	- +5 Volts

DESCRIPTION

The DS1206 Phantom Serial Interface Chip is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a 3-wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. A sequence of software- generated memory cycles encodes commands and transfers data with low pin count. The serial port signaling is derived from the memory address bus lines A0 through A3, the CE\ /CAS\ signal and RAS\ /OE\ signal without affecting address space, thereby maintaining transparency to the memory bus. Communications are established under software control by an address pattern recognition sequence (serial port protocol) which disables a bytewide or DRAM memory via CE\ /CAS\ output. An additional address sequence is required to generate the 3-wire port signals: RESET\ (RST\), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201, DS1204U, DS1207, DS1223, and DS1290.

OPERATION

The main parts of the DS1206 are shown in the block diagram of Figure 1. Information presented on address inputs is latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of CE\ / CAS\ In and RAS\ /OE\ In. When redirecting information from a DRAM memory bus, both RAS\ and CAS\ inputs are required and the column addresses are used for signaling.

For a bytewide memory bus, only a CE\ input is required and the RAS\ /OE\ input can be tied low or connected to the memory OE\ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 4-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2.

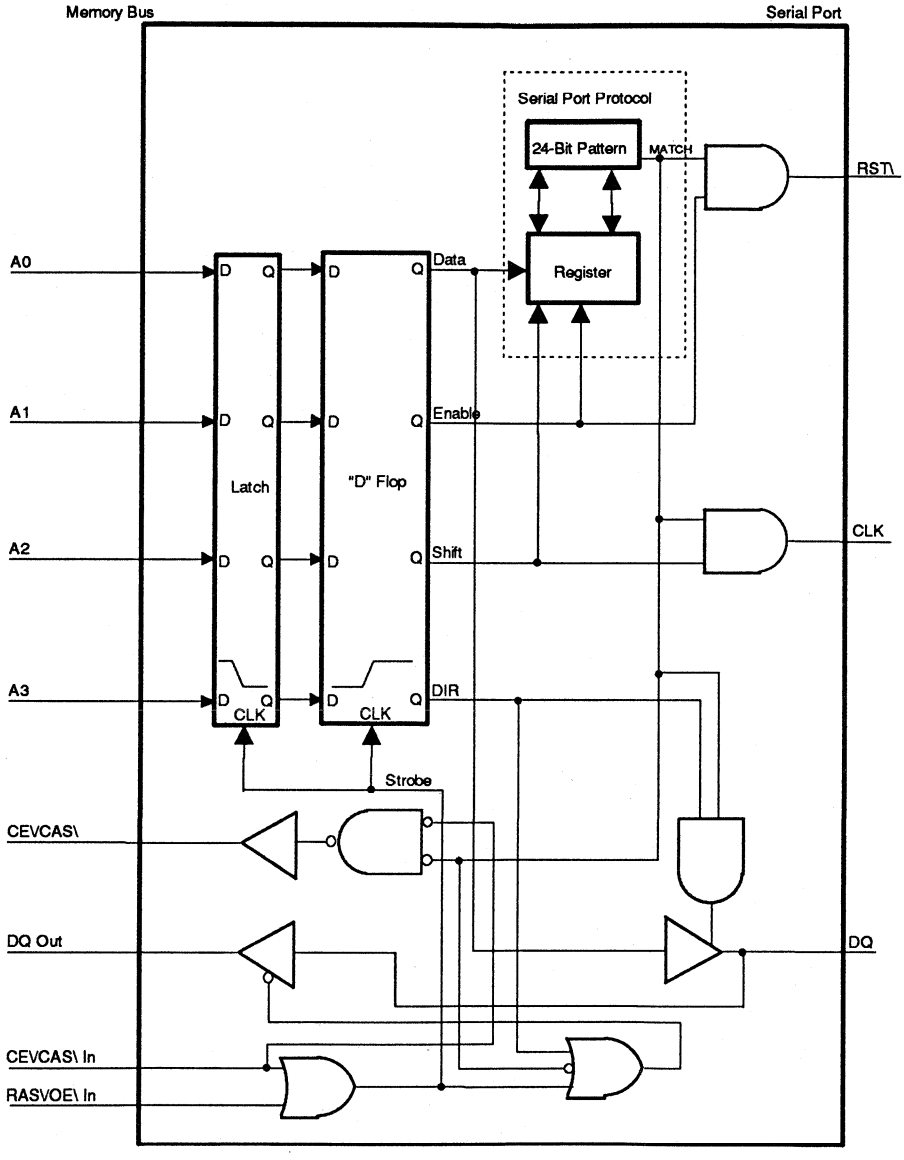
A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24-bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles.

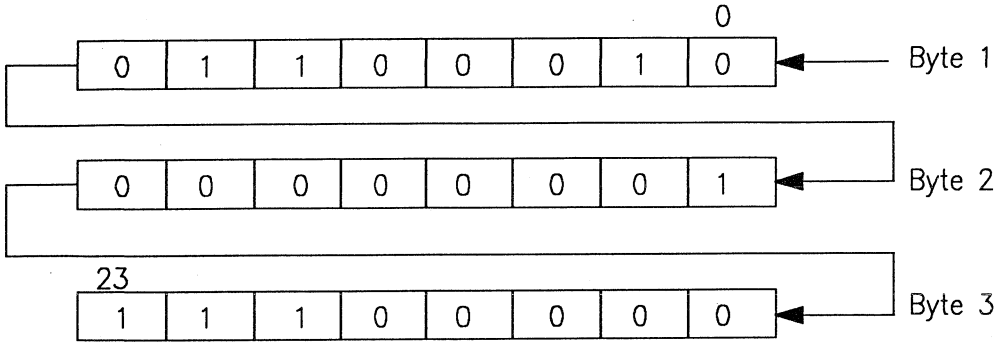
The first memory cycle sets A2 low and establishes the shift clock low. The second memory cycle sets A2 high and causes the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24-bit pattern has been correctly entered , a match signal is generated. The match signal is logically combined with the enable signal to generate the RST\ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and to enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus.

When RST\ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

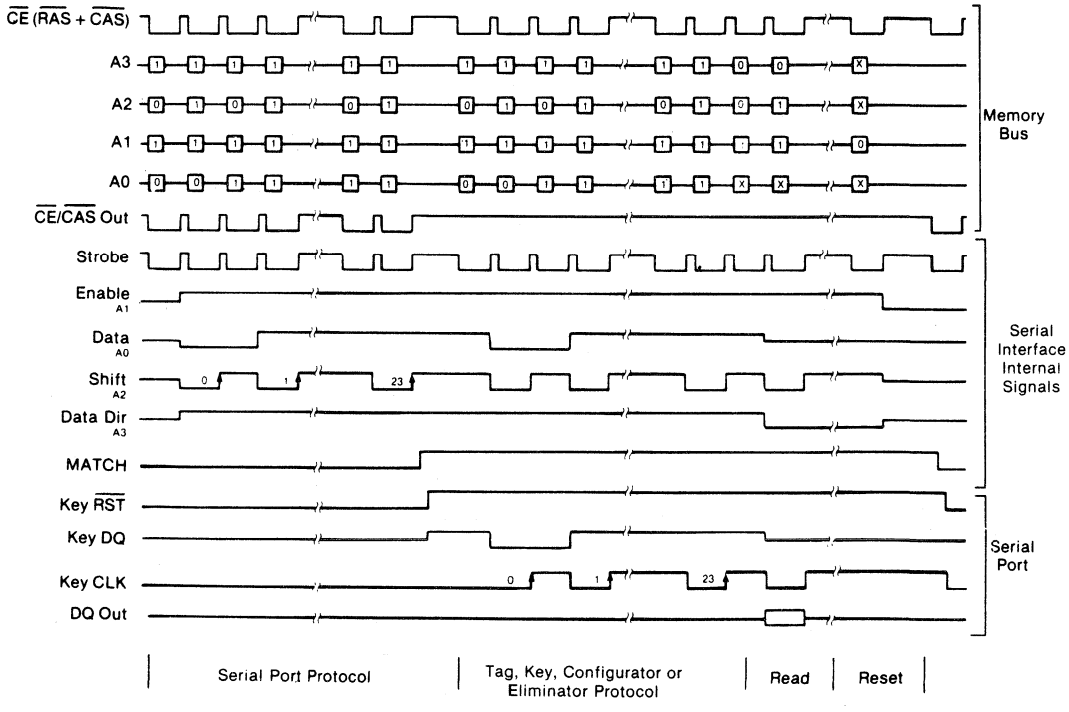
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D C OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

D C ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	uA	
Output Leakage	I_{LO}			1	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
RST\ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

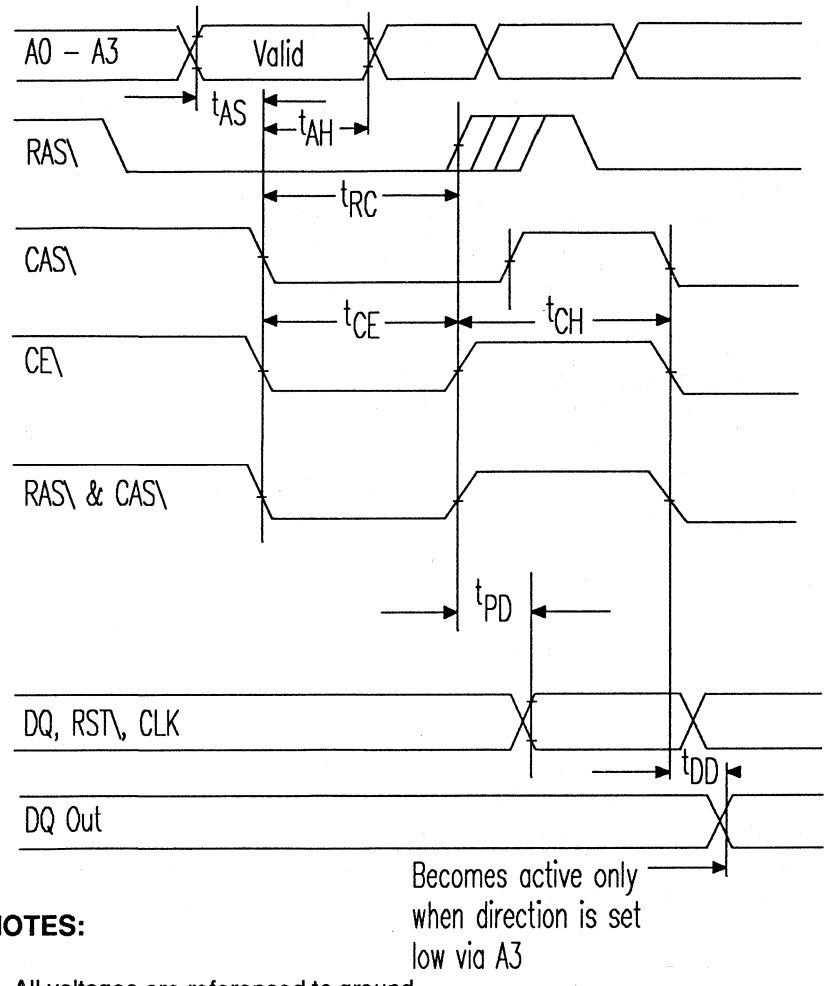
CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

A C ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{cc} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
RAS\ to CAS\ Overlap	t_{RC}	60			ns	
CE\ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
CE\ Inactive	t_{CH}	30			ns	

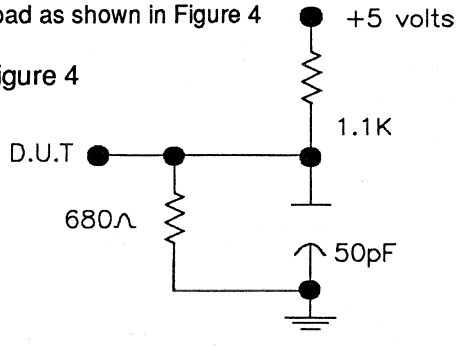
MEMORY BUS INPUTS



NOTES:

1. All voltages are referenced to ground
2. Measured with outputs open
3. Measured with a load as shown in Figure 4

OUTPUT LOAD Figure 4



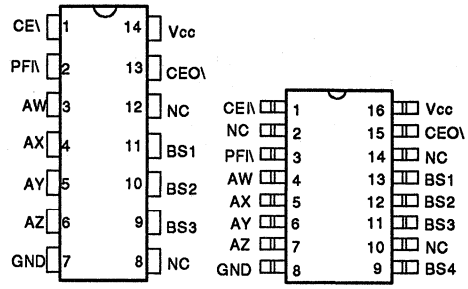
DALLAS SEMICONDUCTOR

DS1222
BankSwitch Chip

FEATURES

- Provides bank switching for 16 banks of memory
- Bank switching is software-controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power-up
- Bank switching logic allows only one bank on at a time
- Custom recognition patterns are available to prevent unauthorized access
- Full ± 10% operating range
- Low-power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1222 14-Pin DIP (300 Mil.)

DS1222S16-Pin SOIC (300 Mil.)

PIN NAMES (\ Denotes Condition Low)

A_W-A_Z	Address Inputs
CEI\	Chip Enable Input
CEO\	Chip Enable Output
NC	No Connection
BS1,BS2,	Bank Select Outputs
BS3,BS4	Bank Select Outputs
PFI\	Power Fail Input
V_{CC}	+5 Volts
GND	Ground

DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

OPERATION-BANK SWITCHING

Initially, on power-up all four bank select outputs are low and the chip enable output (CEO\) is held high. (Note: the power fail input [PFI\] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs A_W through A_Z should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when CEI\ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses A_X, A_Y, and A_Z. However, address line A_W defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of CEI\ when the last set of bits is input and a match has been established. After bank selection CEO\ always follows CEI\ with a maximum propagation delay of 15ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

	BIT SEQUENCE															
ADDRESS INPUTS	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_W	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	A_W Bit Sequence 11	12	13	14	15	Outputs BS1	BS2	BS3	BS4
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*CEO\ = V_{IH} independent of CEI\

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	2
Output Current @ 0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

CAPACITANCE (t_A=25°C)

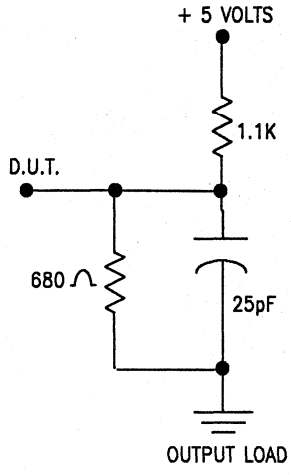
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V+/- 10%)

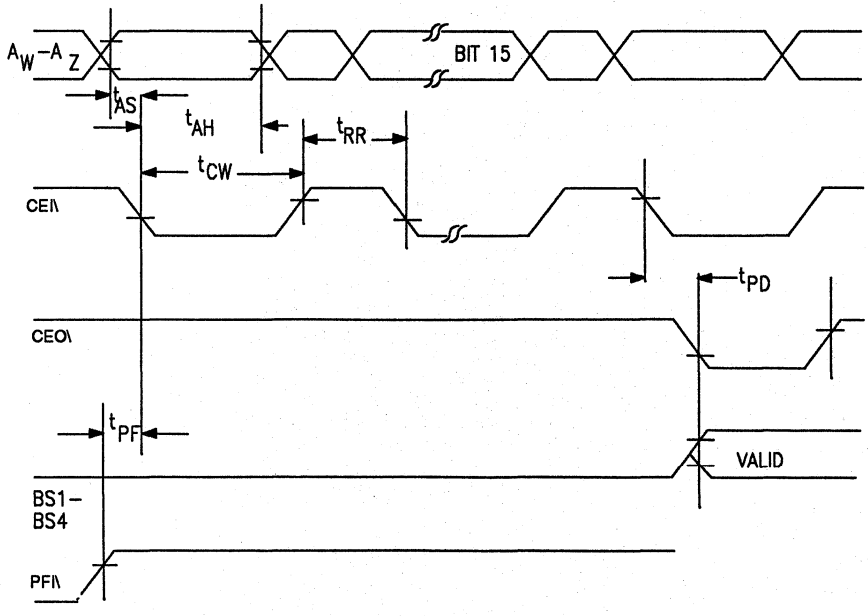
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First CE\	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

NOTES: 1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD FIGURE 1



TIMING DIAGRAM-ACCESS TO BANK SWITCH



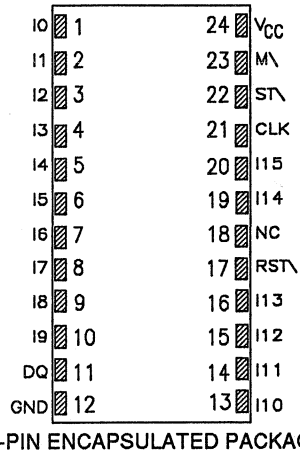
DALLAS SEMICONDUCTOR

DS1223
Electronic Configurator

FEATURES

- 16 remote programmable switches
- 9 bytes of nonvolatile read/write memory
- 16-bit programmable comparator
- 3-pin serial port sets switches and accesses memory
- Greater than 10 years of data retention
- Data and switch settings are automatically protected during power loss
- Full ± 10% operating range
- Applications include DIP switch replacement, remote PC board configuration, mapping, and decoding
- Connects directly to DS1206 Phantom Serial Interface Chip

PIN DESCRIPTION



24-PIN ENCAPSULATED PACKAGE
(720 MIL)

PIN NAMES (\ Denotes Condition Low)

I0-I15	- Switch, Comparator Input/Output
DQ	- Data Input/Data Output
GND	- Ground
RST\	- RESET
CLK	- CLOCK
ST\	- STROBE
V_{CC}	- +5 Volts
NC	- No Connection
M\	- Comparator Match

DESCRIPTION

The DS1223 Electronic Configurator is a CMOS nonvolatile switch, comparator, and read/write memory circuit designed for personalizing and configuring electronic equipment remotely. The Configurator has 16 switches that can be remotely programmed to either logic 1, logic 0, or high impedance. Switch pairs can also be connected to simulate 8 SPST switches. In addition, the logic state of 16 inputs can be compared to data contained in nonvolatile memory. There are 16 bytes of nonvolatile read/write memory. Bytes 0, 1, 2, 3, and 4 define switch settings; bytes 5 and 6 relate to the comparator; bytes 7 through 15 are free for any desired use.

A lithium energy source retains information stored in all 16 bytes of memory when power is lost. The Electronic Configurator monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is

switched on, and write protection is enabled to prevent loss of data. While in the data retention mode, the switch/comparator outputs are all in a high impedance mode and all inputs are ignored.

Information is sent to the Configurator via a serial input one byte at a time or in a burst where all 16 bytes are either written or read. Interface to a microprocessor is minimized by on-chip circuitry that permits data transfers with only three signals: CLOCK, RESET\, and Data Input/ Output.

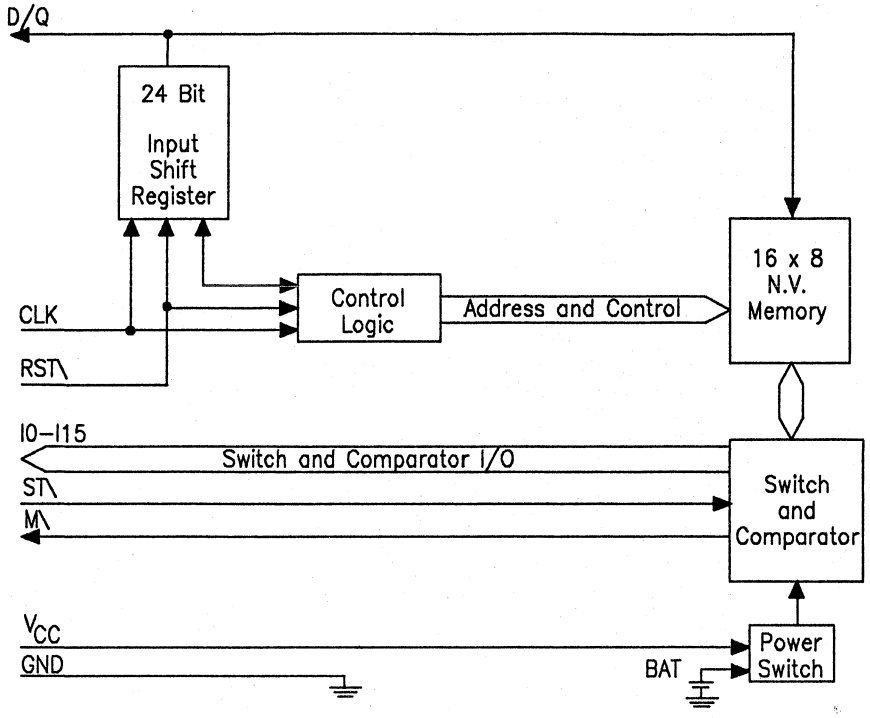
OPERATION

The block diagram (Figure 1) of the Electronic Configurator illustrates the main elements of the device: input shift register, control logic, nonvolatile memory, switch and comparator circuits, and power switch. To initiate communications with the Configurator, RESET\ is taken high and 24 bits are loaded into the input shift register providing both address and command information. Each bit is input serially on the rising edge of the clock. Four address bits specify one of 16 nonvolatile memory locations. The remaining command bits specify read/write and byte/burst mode. After the first 24 clocks which load the input shift register, additional clocks will output data for a read or input data for a write. The number of clock pulses equals 24 plus 8 for byte mode or 24 plus 128 for burst mode.

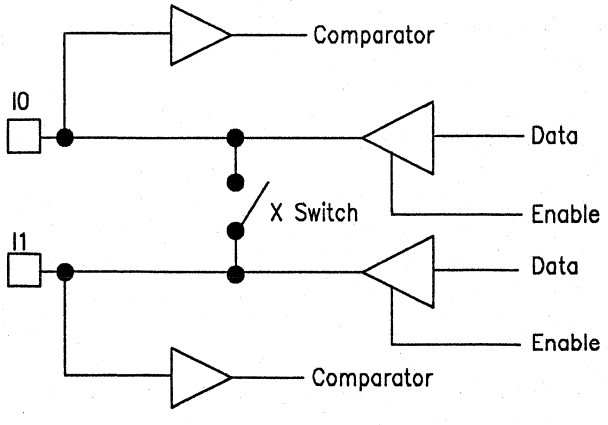
The information stored in the first five bytes of the nonvolatile memory defines the status of input/output pins I0-I15. The switch configuration is illustrated in Figure 2. Data stored in nonvolatile memory bytes 6 and 7 contain 16 bits that are compared to the input/output pins I0-I15. When all inputs match the value stored in bytes 6 and 7, the MATCH\ pin will be latched and driven low when the STROBE\ input transitions from low to high.

The nine remaining bytes serve as user read/ write nonvolatile memory. Figure 3 illustrates the Configurator register address and the definition of each bit.

ELECTRONIC CONFIGURATOR BLOCK DIAGRAM-Figure 1



CONFIGURATOR SWITCHES Figure 2



X Switch Resistance ≤ 500Ω

Switch Pairs		
	I0–I1	I8–I9
	I2–I3	I10–I11
	I4–I5	I12–I13
	I6–I7	I14–I15

CONFIGURATOR MEMORY ADDRESSES-Figure 3

	MSB 7	6	5	4	3	2	1	0 LSB	
Byte 0	I15,I14	I13,I12	I11,I10	I9,I8	I7,I6	I5,I4	I3,I2	I1,I0	X Switch 1= Closed 0= Open
Byte 1	I7	I6	I5	I4	I3	I2	I1	I0	Data Out 1= Logic High 0= Logic Low
Byte 2	I15	I14	I13	I12	I11	I10	I9	I8	Data Out 1= Logic High 0= Logic Low
Byte 3	I7	I6	I5	I4	I3	I2	I1	I0	Enable Out 0= HiZ
Byte 4	I15	I14	I13	I12	I11	I10	I9	I8	Enable Out 0= HiZ
Byte 5	I7	I6	I5	I4	I3	I2	I1	I0	Comparison
Byte 6	I15	I14	I13	I12	I11	I10	I9	I8	Comparison
Byte 7									User Byte
Byte 8									User Byte
Byte 9									User Byte
Byte 10									User Byte
Byte 11									User Byte
Byte 12									User Byte
Byte 13									User Byte
Byte 14									User Byte
Byte 15									User Byte

ADDRESS/COMMAND

Each data transfer consists of a three-byte address/command input called the address/command. The address/command is shown in Figure 4. As defined, the first byte of the address/command specifies whether the memory will be written into or read. If any one of the bits of the first byte of the address command fails to meet the exact pattern of read or write, the cycle is aborted and all future inputs to the Configurator are ignored until RESET\ is brought low and then high again to begin a new cycle. The 8-bit pattern for read is 01100010. The pattern for write is 10011101. The second byte of the address/command describes address A0 in bit 0, A1 in bit 1, A2 in bit 2, and A3 in bit 3. Bits 4 through 7 of the second byte of the address/command must be set at logic 0. If bits 4 through 7 do not equal logic 0, the cycle is aborted and all future inputs to the Configurator are ignored until RESET\ is brought low and then high again to begin a new cycle. The third byte of the address/command must have a logic 0 in bit 0 through bit 5 and a logic 1 written in bit 6. Bit 7 of byte three of the address/command is used along with bits A0 through A3 in byte 2 to define the burst mode. When A0 through A3 of byte two equals logic 0 and bit 7 of byte three equals logic 1, the Configurator will enter the burst mode after the 24-bit address/command sequence is complete.

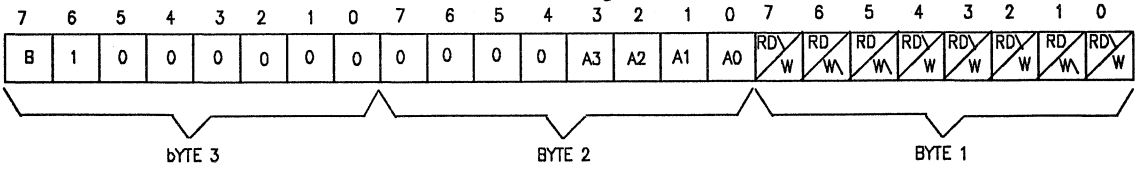
BURST MODE

Burst mode is specified for the Electronic Configurator when all address bits (A0-A3) of the address/command are set to logic 0 and bit 7 of byte three is set to logic 1. The burst mode causes 16 consecutive bytes to be read or written. Burst mode terminates when the RESET\ input is driven low.

RESET AND CLOCK CONTROL

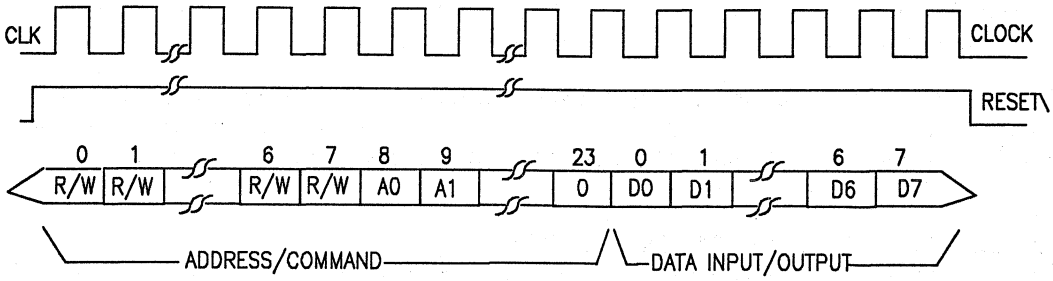
All data transfers are initiated by driving the RESET\ input high. The input also provides a method of terminating either single-byte or multiple-byte transfers. A clock cycle is a sequence of a falling edge followed by a rising edge. For data input, the data must be valid during the rising edge of clock cycles. Address/command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminate and the D/Q pin goes to a high impedance state if the RESET\ input is low. The RST\ input is used only to control communications with the Configurator and has no effect on the nonvolatile memory data. Data transfer is illustrated in Figure 5.

CONFIGURATOR-ADDRESS/COMMAND WORD Figure 4

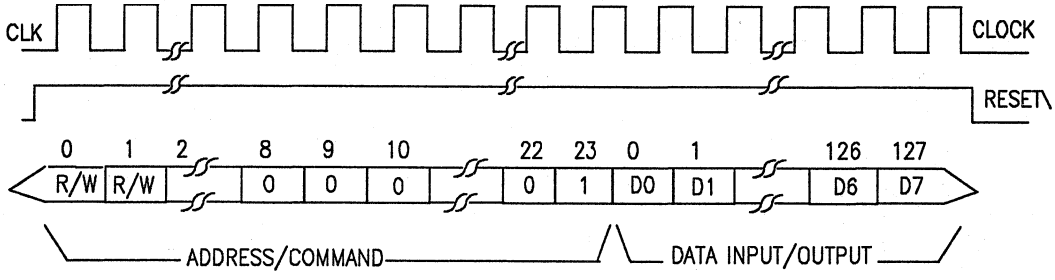


B-Burst
RD-Read
W-Write
A0-A3-Address

DATA TRANSFER Figure 5
SINGLE BYTE TRANSFER



BURST MODE TRANSFER



NOTES:
1. Data input sampled on rising edge of clock.
2. Data output changes on falling edge of clock.

DATA INPUT
Following the 24 CLOCK cycles that input an address/command, a data byte is input on the rising edge of the next 8 CLOCK cycles, assuming that the read/write and write/read bits are properly set. (For data input byte 1, bit 0 = 1; bit 1 = 0; bit 2 = 1; bit 3 = 1; bit 4 = 1; bit 5 = 0; bit 6 = 0; bit 7 = 1.)

DATA OUTPUT
Following the 24 CLOCK cycles that input the read mode, a data byte is output on the falling edge of the next 8 CLOCK cycles. (For data output byte 1, bit 0 = 0; bit 1 = 1; bit 2 = 0; bit 3 = 0; bit 4 = 0; bit 5 = 1; bit 6 = 1; bit 7 = 0.)

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			1	uA	5
Output Leakage	I_{LO}			1	uA	5
Output Current @2.4V	I_{OH}	-1			mA	11
Output Current @ .4V	I_{OL}			+4	mA	11
Output Current @2.4V	I_{OH}	-400			uA	12
Output Current @ .4V	I_{OL}			1.6	mA	12
X Switch Impedance	X			500	ohms	7
Active Current	I_{CC1}			10	mA	8
Standby Current	I_{CC2}			2	mA	8, 2

CAPACITANCE (t_A = 25°C)

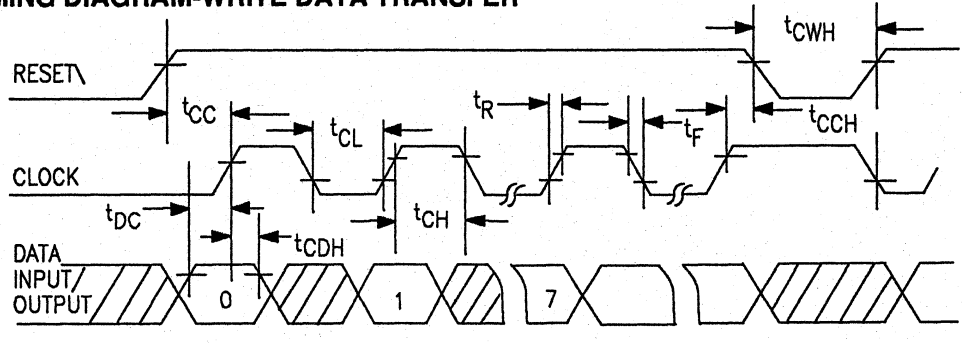
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5			pF	
Output Capacitance	C_{OUT}	7			pF	

AC ELECTRICAL CHARACTERISTICS

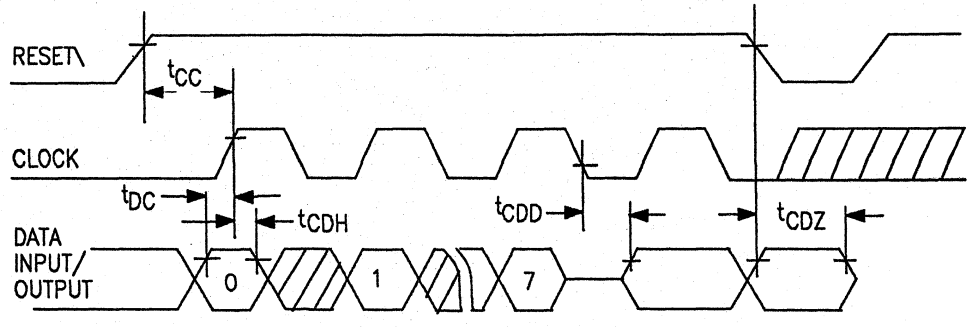
(0°C to 70°C, V_{CC} = 5v ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	3
Data to CLK Hold	t_{CDH}	50			ns	3
CLK to Data Delay	t_{CDD}			200	ns	3,4,6
CLK Low Time	t_{CL}	250			ns	3
CLK High Time	t_{CH} ,	250			ns	3
CLK Frequency	f_{CLK}	DC		2.0	MHz	3
CLK Rise & Fall	t_R,t_F			10	ns	3
RST\ to CLK Setup	t_{CC}	1			us	3,9
CLK to RST\ Hold	t_{CCH}	50			ns	3
RST\ Inactive Time	t_{CWH}	1			us	3
RST\ to //O High Z	t_{CDZ}			75	ns	3
Strobe to MATCH\ Valid	t_{SM}			35	ns	3
Input Setup	t_{SU}	40			ns	3,4
Input Hold	t_{HD}	10			ns	3,4

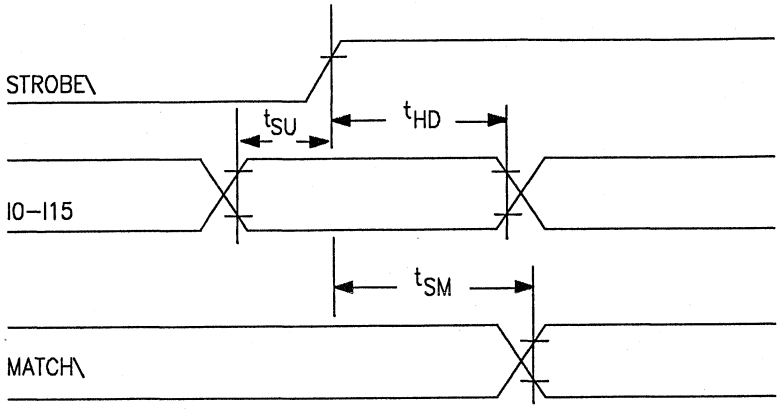
TIMING DIAGRAM-WRITE DATA TRANSFER[10]



TIMING DIAGRAM-WRITE DATA TRANSFER[10]



TIMING DIAGRAM-COMPARATOR[10]



NOTES:

1. All voltages are referenced to GND.
2. RESET\ = V_{IH}.
3. Measured at V_{IH} = 2.0 or V_{IL} = .8V and 10 ns maximum rise and fall time.
4. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.
5. V_{CC} = +5 volts with outputs open.
6. Load capacitance = 100 pF.
7. X Switch Impedance is the terminal resistance of switch pairs when the X switch is closed; see Figure 2.
8. Measured with outputs open.
9. Measured at V_{IN} of RST\ = 3.8V.
10. A period of 100 ns must elapse after data transfer before switches and comparator outputs are valid.
11. Applies to DQ and MATCH\.
12. Applies to switches.

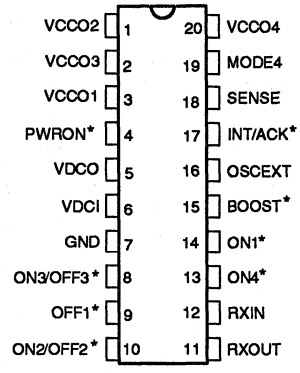
DALLAS SEMICONDUCTOR

DS1227
KickStarter Chip

FEATURES

- Provides step-up regulation and microenergy management for battery-operated systems
- Converts +3V to +6V DC input power source to +5 V DC out for system power
- Kickstarts system power upon detection of external stimuli:
  - -Clock/calendar alarm
  - -Sensor trip; such as from a photo diode
  - -Incoming activity to a serial port
  - -Any low-level signal transition
- Shuts down microcontroller power under software control when operation complete
- Provides 3 auxiliary power outputs for independent powering of system functions
- Allows design of power-on-demand systems
- Ensures maximum life of main power source
- Ideally suited for DS5000-based systems
- Available in 20-pin DIP or SOIC packages

PIN DESCRIPTION



20-Pin DIP
(300 Mil)

(* Denotes Condition Low)

ORDERING INFORMATION

DS1227:	20-Pin DIP
DS1227S:	20-Pin SOIC

DESCRIPTION

The DS1227 KickStarter Chip is a unique CMOS circuit which combines power conversion and microenergy management functions for battery operated systems. Using its integral DC-DC converter, the DS1227 supplies +5V on demand from either a 3 or 6 volt battery input. The primary +5V output, typically tied to the microcontroller's V_{CC} pin, is kickstarted on in response to any one of several possible momentary, external signal transitions. Two auxiliary +5V power supply outputs can then be independently enabled or disabled under software control. When the primary power supply output is disabled, also under software control, the auxiliary power supply outputs remain in the state selected. In this manner, individual portions of the system can be powered only when they are required, minimizing the energy consumption of the system.

The KickStarter activates, or kickstarts, the primary V_{CC} output in response to external momentary low-going signals. Examples of such signals include a clock/calendar alarm from a DS1283 Watchdog Timekeeper, or an incoming asynchronous serial data word from a host PC via the DS1275 Line-Powered RS-232 Transceiver, or a simple pushbutton switch.

In addition, the DS1227 kickstarts primary system power in response to activity detected by an external sensor circuit. In this case, the KickStarter can be signalled at regular intervals, typically from a DS1283 Watchdog Timekeeper, to momentarily apply power to the sensor and monitor an input for an active response.

An application using the KickStarter has the capability to "wake-up" from a ultra-low power state, perform a task using minimum energy, and then go back to sleep until the DS1227 is signalled to kickstart system operation once again.

PIN	I/O	DESCRIPTION
BOOST*	Input	Regulation mode control
VDCO	Output	Main DC supply voltage output
VDCI	Input	Main DC supply voltage input
GND	-	System ground
VCCO1	Output	Primary switched supply voltage output
ON1*	Input	On control for VCCO1. ON1* is negative edge triggered and internally pulled high via a weak resistor.
INT/ACK*	Input/ Output	Interrupt output/input; internally pulled low via a weak resistor during output; level activated via strong high voltage for input
OFF1*	Input	Off control for VCCO1; edge-triggered active low
PWRON1*	Output	VCCO1 Power On signal output; indicates when VCCO1 is powered on; sometimes required for controlling external tri-state buffers in systems where microenergy management techniques are employed.
VCCO2	Output	Auxiliary switched supply voltage outputs
ON2/OFF2*	Input	On/Off controls for VCCO2/VCCO3; Level activated
ON3/OFF3*	Input	
VCCO4	Output	Momentarily switched VCC output
ON4*	Input	VCCO4 trigger; edge activated; active low
SENSE	Input	Sense input sampled just prior to VCCO4 off; turns on VCCO1 if active; active high
MODE4	Input/ Output	Selects VCCO4 on time; level sensitive input/current source output
RXIN	Input	Serial I/O input; On control for VCCO1 when serial activity detected; edge activated
RXOUT	Output	Serial I/O output; Echos incoming serial data from RXIN when VCCO1 is turned on
OSCEXT	Output	Oscillator Signal Output; Gated by internal comparator when BOOST* is enabled. Continuous when BOOST* is disabled.

INPUT SUPPLY VOLTAGE

The KickStarter is capable of operating either in a regulated step-up DC to DC conversion (boost) mode or in a non-regulated supply voltage pass-through mode.

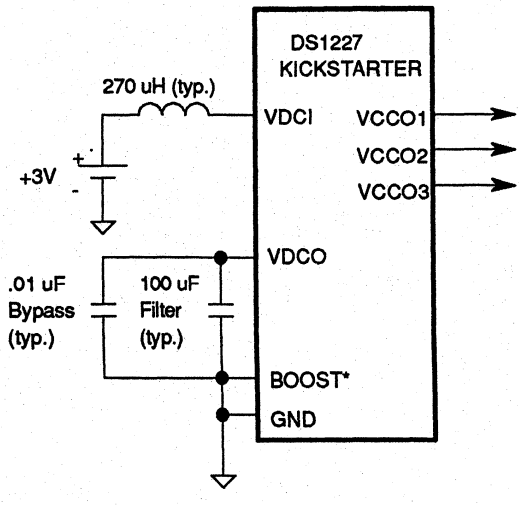
In boost mode, the KickStarter is designed to provide a regulated +5V output on the VCCO1, VCCO2, or VCCO3 voltage supply output pins from a +3V lithium source. Figure 1 illustrates the standard configuration for use of this mode. The BOOST* pin should be tied low in order to enable step-up DC to DC conversion. VDCI is used for the DC power supply input and is tied through an inductor (270 uH typical) to a +3V lithium cell. VDCO is the main DC output which is switched to the VCCO1, VCCO2, and VCCO3 outputs. This pin requires a large capacitor (typically 100 uF) to ground for the boost regulation low pass output network. Further details of the boost voltage regulator operation are given in the "Boost Mode Operation" section of this data sheet.

Figures 2 and 3 illustrate the required configurations to select the supply voltage pass-through mode of operation. In both of these configurations the BOOST* pin should be strapped directly to the VDCO pin. This connection causes the BOOST* pin to remain at a high level at all times that a battery is connected. As a result, the internal boost regulator will be disabled when kickstarting occurs. When a +5V supply is used as the input DC power source, it should be directly connected to the VDCO in parallel with a filter capacitor as shown in Figure 2. The VDCI input itself should be grounded in this configuration.

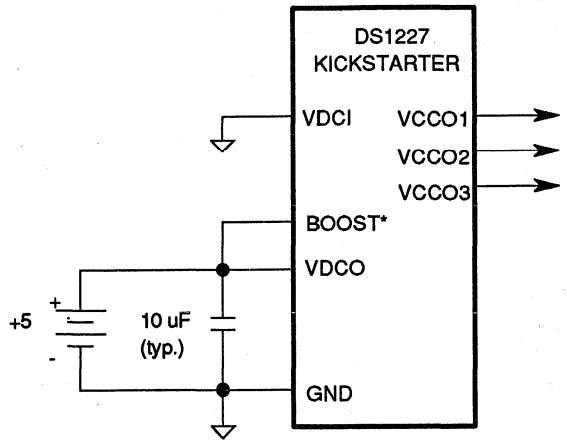
If a +6V supply is used, then it should be connected to the VDCI pin. A filter capacitor should still be connected to VDCO. The voltage on VDCO and subsequently on VCCO1, VCCO2, and VCCO3 (when they are enabled following kickstarting) will be a diode drop below the VDCI voltage.

In both the boost and pass-through modes, the DS1227 uses the voltage on VDCO as its own internal supply.

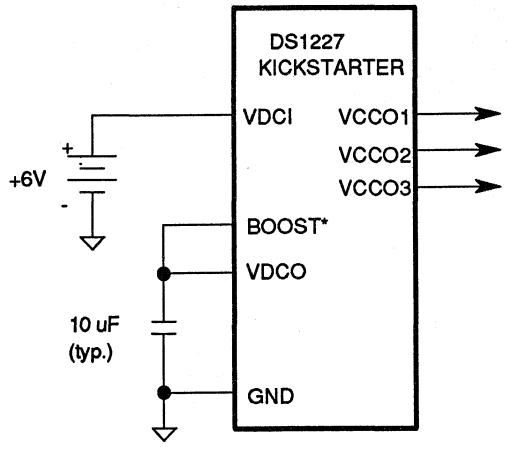
DS1227 BOOST MODE CONFIGURATION Figure 1



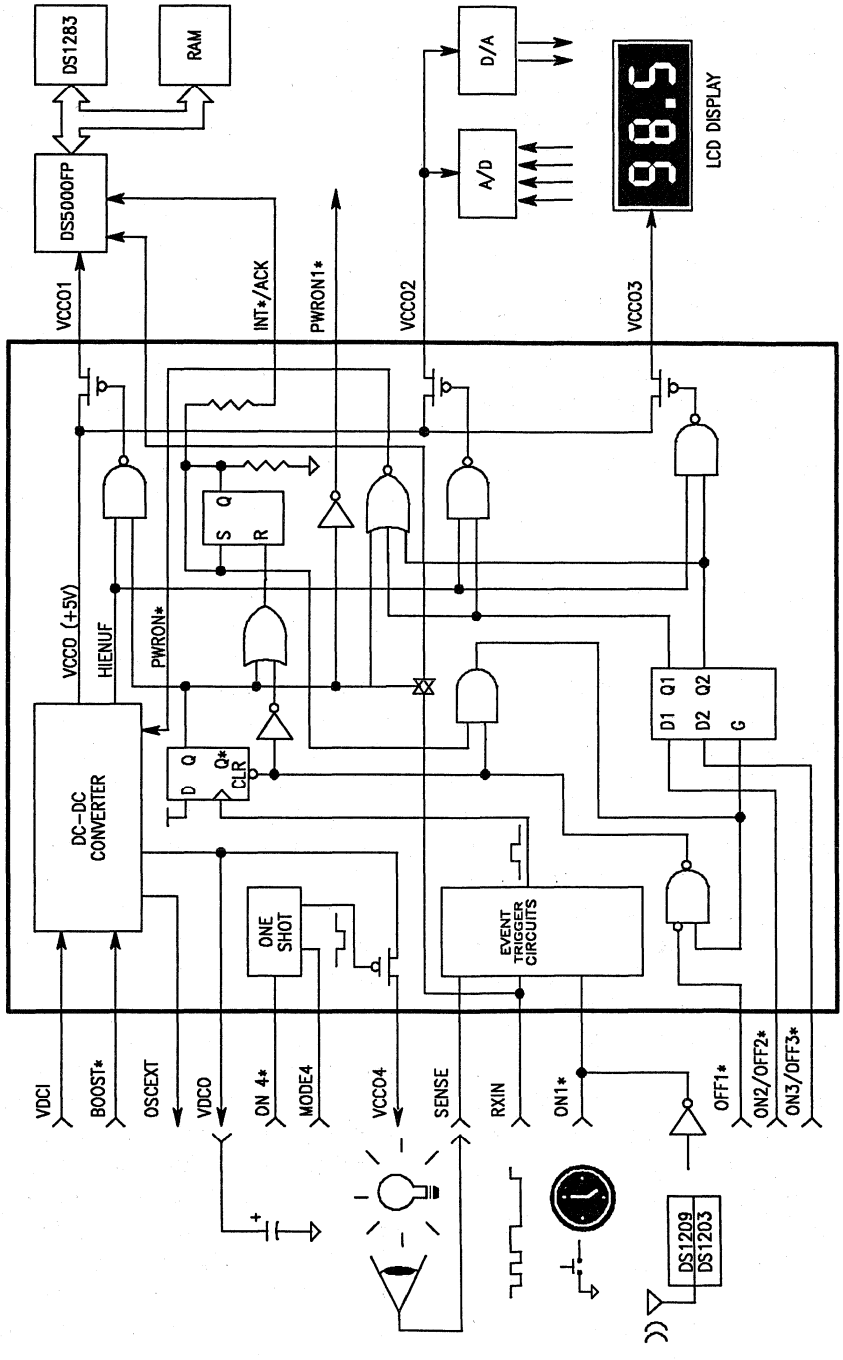
DS1227 +5V PASS-THROUGH MODE CONFIGURATION Figure 2



DS1227 +6V PASS-THROUGH MODE CONFIGURATION Figure 3



DS1227 KICKSTARTER BLOCK DIAGRAM Figure 4



KICKSTARTER OPERATION

A conceptual block diagram of the internal circuitry of the DS1227 is illustrated in Figure 4 for reference. While in an initial power-down state, the DS1227 will sense activity from an external stimulus applied to one of three input pins and kickstart system power by applying voltage from the input power source to the primary VCCO output (VCCO1). Activity detected on any of the ON1*, RXIN, and SENSE pins initiates the kickstarting action.

When kickstarting occurs and the DS1227 is configured for boost operation, the on-chip step-up DC-to-DC converter is started and the voltage on VDCO will be boosted from its initial V_{BAT} level to V_{DCON} before VCCO1 is turned on. If the DS1227 is configured for voltage pass-through operation, then the DC-to-DC converter will remain disabled and voltage on the VDCO line will be switched to the VCCO1 pin immediately following the detection of an active transition on a stimulus input.

Initially, when VCCO1 is off, the INT*/ACK pin is collapsed to ground. At the time that voltage is switched to the VCCO1 output pin during kickstarting, the INT*/ACK pin will be latched such that it will remain in a low state. This signals the microcontroller that a power-on reset has occured. The OFF1, ON2/OFF2*, and ON3/OFF3* inputs are all ignored until the microcontroller acknowledges this power-on reset condition. This acknowledgement is performed via the same INT*/ACK pin, which also performs the function of an interrupt acknowledge input. This is made possible due to the fact that the pin has a weak NMOS pulldown which forms a latch. When INT*/ACK is externally driven with a sufficiently strong high signal (as described in the "Electrical Characteristics" section), the state of the latch will be switched and as a result the interrupt condition will be reset.

After the power-on reset interrupt has been acknowledged and the DS1227 is in a powered on condition, the INT*/ACK pin will be again taken low to signal the detection of active signalling on the ON1* or SENSE inputs. Further activity on the RXIN input will not cause a subsequent interrupt condition. The INT*/ACK can be returned to its high (reset) state, again by externally driving it with a sufficiently strong high signal.

The OFF1* input is used to turn off the VCCO1 output under software control. It is typically interfaced to the system microcontroller via a port pin configured as an output. As noted above, it is active only when VCCO1 is on and INT*/ACK has been set high.

STIMULUS INPUTS

ON1* is a simple TTL-level compatible input which is designed to detect a negative-going edge. VCCO1 is kickstarted whenever an active edge is detected on this pin.

The RXIN input can be used to initiate the kickstarting action in response to the detection of incoming serial data. In this configuration, the RXIN pin is interfaced to an incoming serial data line, typically from an RS232 tranceiver. RXOUT is the corresponding output and is used to route the serial data to the microcontroller. RXIN remains internally disconnected from RXOUT until VCCO1 is powered on. At that time, the two lines are connected and serial data is passed straight through the device to the microcontroller.

The SENSE pin is intended to be connected to an external sensor circuit which is powered from VCCO4. This circuit is then momentaritly powered from the KickStarter's VCCO4 output in response to a negative going edge applied to the ON4* input. VCCO4 will stay powered for an amount of time determined by the circuitry on the MODE4 pin. During the time that VCCO4 is on, the SENSE pin has an internal pulldown device which is activated. SENSE is sampled just prior to the VCCO4 output being discon-

nected. If SENSE is externally driven high (V_{IH}) at this time, it kickstarts VCCO1 power. Any time that VCCO4 power is off, the SENSE pin appears as a high impedance to external circuitry.

The amount of time that VCCO4 is on is determined by the configuration of the MODE4 pin. MODE4 is intended to either be tied high (typically to VDCO) or tied to an external capacitor. The VCCO4 on time is thereby determined either by the amount of time between falling edges on ON4* or by the value of the capacitor.

If the MODE4 pin is tied high at the time that ON4* is activated, then VCCO4 will remain on until the next falling edge is detected on ON4*. Figure 5 illustrates the timing associated with this mode of operation. If the KickStarter is also configured for boost regulation and VCCO1, VCCO2, and VCCO3 are turned off, the DC-DC converter will be briefly enabled so that +5V will be supplied on VCCO4 for the duration of the time that it is on.

The alternative MODE4 configuration is illustrated in Figure 6B. As shown in the figure, it is recommended for most applications that a large resistor also be connected between MODE4 and ground in addition to the capacitor. For the configuration shown, the MODE4 pin will be sensed low by the KickStarter just following the negative-going edge at ON4* as shown in the timing diagram in Figure 6A. Following this condition, a constant current specified as I_{M4ON} is supplied out of the MODE4 pin. This will cause the voltage on MODE4 to rise linearly. VCCO4 will remain on until the voltage on MODE4 reaches a threshold specified as V_{M4OFF} (approximately 0.5 V_{DCO}). At this time, VCCO4 will be shut off. At the same time, the constant current source on the MODE4 pin will be disconnected and an internal resistive element (specified as R_{M4DIS}) will be connected between the MODE4 pin and ground. This internal resistive element along with any external resistance will cause the voltage on the capacitor to decay exponentially until it reaches a threshold specified as V_{M4DIS} (approximately 0.1 V_{DCO}). When this condition is reached, the internal resistive element will be disconnected, and the MODE4 pin will appear as a high impedance until the next active transition occurs on ON4*. The external resistor (if present) will then cause the voltage on MODE4 to further decay until it reaches ground or until the next ON4* negative transition, whichever comes first.

When MODE4 is initially grounded as described above, VCCO4 power is switched from the VDCO pin, regardless of whether or not VCCO1, VCCO2, or VCCO3, are powered on. This means that VCCO4 will be switched with the voltage present on VDCO, which could be from +3V to +5V depending on the configuration, input battery voltage used, and whether or not VCCO1, VCCO2, or VCCO3 are switched on.

The above described sampling operation of VCCO4 and SENSE in response to ON4* also takes place when a kickstart has already occured and VCCO1 is on. If SENSE is found to be active in this condition, an interrupt will be signalled on the INT/ACK* pin.

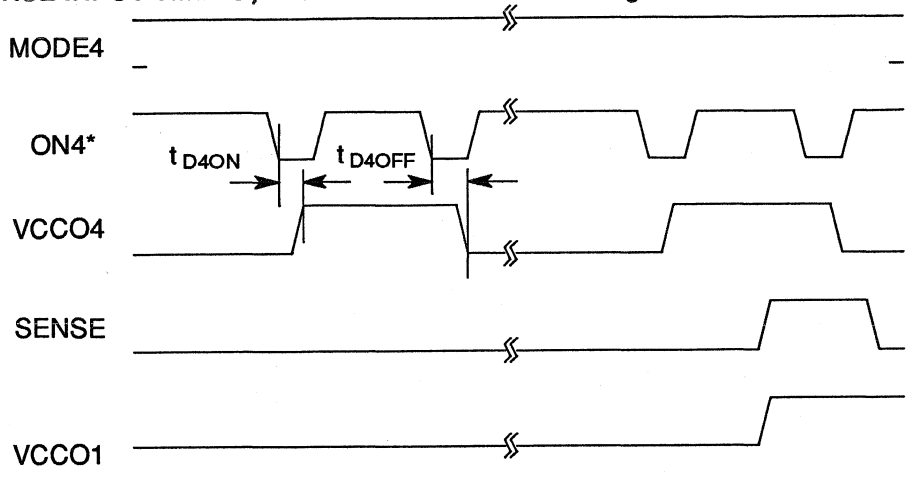
MICRO ENERGY MANAGEMENT

In addition to the kickstarting features described above, the DS1227 allows sections of system circuitry to be individually powered up or down under command of the microcontroller. This capability is referred to as the Micro Energy Management feature of the DS1227.

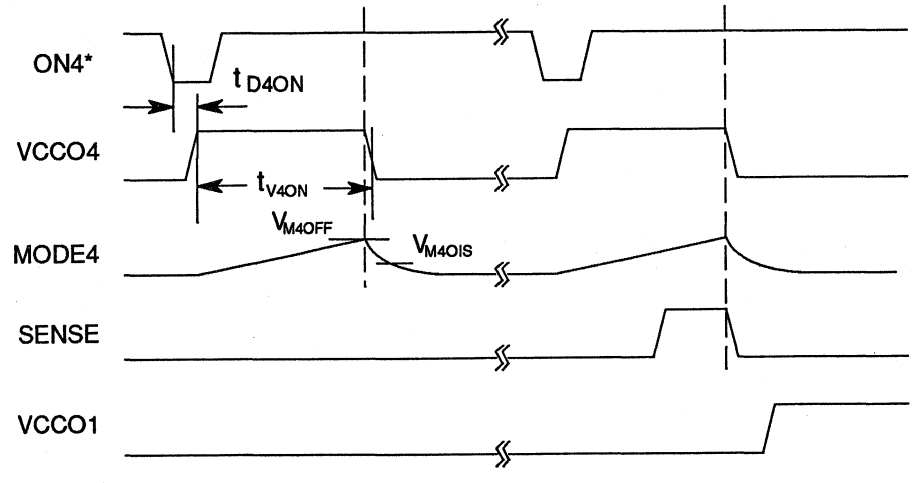
VCCO2 and VCCO3 are auxiliary power supply outputs which can be switched on or off via the ON2/OFF2* and ON3/OFF3* pins, respectively. The ON2/OFF2* and ON3/OFF3* control pins are intended for connection to two microcontroller's port pins configured as outputs. The corresponding VCCO output pins can then be turned on or off as desired under control of the system application software.

The ON2/OFF2* and ON3/OFF3* inputs are

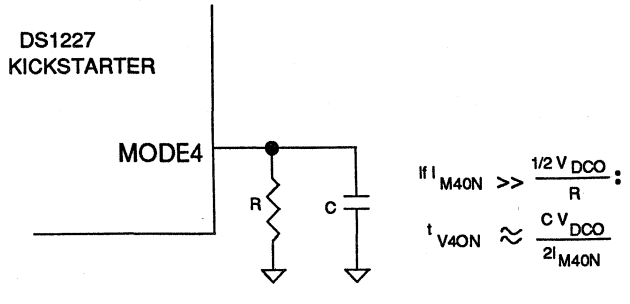
SENSE INPUT TIMING; MODE4 STRAPPED HIGH Figure 5



SENSE INPUT TIMING; MODE4 WITH RC NETWORK Figure 6A



MODE4 RC NETWORK CONNECTION Figure 6B



level-activated. The corresponding VCCO output therefore turns on when the on/off pin is high and off when it is low. These inputs are active only if the VCCO1 output is on and the INT*/ACK output has been set to a high state signalling a power-on reset condition.

When VCCO2 or VCCO3 are turned on, they will remain on until the corresponding control input is taken low by the software. This is true even if the OFF1* input is taken to its active low state at the time that either ON2/OFF2*, ON3/OFF3*, or both, are high.

Once OFF1* is activated, the current states of ON2/OFF2* and ON3/OFF3* are internally latched and further activity on these pins is ignored. If both of the corresponding outputs (VCCO2 and VCCO3) are turned off at this time and boost operation has been selected, then the internal oscillator is killed and the DC-to-DC converter will be shut down. If either VCCO2 and/or VCCO3 are left switched on when OFF1* is activated, they will remain switched on even after VCCO1 has been turned off. If the DS1227 has been configured for boost operation, the DC-to-DC converter will remain operational during the entire time that VCCO1 is turned off so that +5 volts will continue to be supplied on either or both of these output pins. These pins can be shut off only when kickstarting occurs once again and VCCO1 is switched on and INT*/ACK has been set high.

BOOST MODE OPERATION

The DS1227 KickStarter incorporates all of the necessary control and power switching functions required for its +3V to +5V step-up DC-to-DC converter. These functions include a bandgap reference, oscillator, voltage comparator, catch diode, and a N-channel MOSFET. The only external components required are an output filter capacitor and a low-cost inductor. The block diagram shown in Figure 7 illustrates the DC-to-DC converter.

When kickstarting occurs from an initial powered down state (i.e., VCCO1, VCCO2, and VCCO3 turned off), an internal start sequence is initiated within the DS1227. During this sequence, the VCCO1 output remains shut off and the BOOST* pin is sampled in order to determine if the DS1227 is configured for boost mode operation. If BOOST* is low, then boost mode operation is enabled and the DC-to-DC converter is started.

The internal DC-to-DC converter is started by enabling the on-chip 40 KHz oscillator. It then begins to build up the voltage on the VDCO filter capacitor. Internal counter logic ensures that the DC-to-DC converter stays in start mode for a minimum of 6 clock periods (nominally 150 us @ 40 KHz). After this initial delay time, the VDCO output is monitored by the internal Error Comparator as it slews up to V_{DCON}. As long as the VDCO voltage remains below the preset value, the Error Comparator will be switched high and the internal 40 KHz oscillator will be connected to the gate of the VDCI driver.

The VDCI driver is a large N-channel MOSFET with a typical ON resistance of less than 4 ohms and is capable of supplying a peak current of 450 mA. The output device is turned on during each ON half-cycle generated by the internal square-wave oscillator, and is turned off during each OFF half-cycle. During each ON half-cycle, the current through the inductor rises linearly, storing energy in the coil. When the output device is turned off, the external inductor's magnetic field collapses, and the voltage across the inductor reverses sign. The voltage at VDCI then rises until the internal diode is forward biased, delivering power to the VDCO output. The converter is thereby powered from its own VDCO output. This is often referred to as "bootstrapped" operation, since the circuit figuratively "lifts" itself up. In order to guarantee that the KickStarter can bootstrap itself up to operating voltage, the VDCI voltage must be at the minimum level of

V_{DCISU} as listed in the DC characteristics section of this data sheet.

When the voltage on VDCO rises to the V_{DCON} threshold, the internal signal called "HIENUF" will be active and the VCCO1 PMOS device is switched on. As noted above, internal circuitry ensures that this device will not be switched on for a minimum of 6 clock cycles from the time that the DC-to-DC converter is started. However, since the recommended values for the external LC components result in a time constant which is much longer than 6 cycles, the actual slew rate will, in practice, be much longer than this delay time.

If loading of the VCCO outputs causes VDCO to drop below V_{DCOFF}, the DS1227 will deactivate HIENUF and the VCCO1 PMOS device as well as the other VCCO PMOS devices will be switched off. The VDCO voltage will then be monitored for the V_{DCON} trip point before reconnecting the load. As a result, the power control regulation loop could oscillate between these two states until the VCCO1 node had sufficient charge to remain above the V_{DCOFF} threshhold. To prevent this from occuring, the value of the filter capacitor must be sufficiently large. For large capacitive loads on VCCO1 the output may dip below V_{DCOFF} as a result of charge sharing and a larger regulation capacitor at VDCO may be required. For large resistive loads the inductance and capacitance values may need to be adjusted using a smaller inductor value and large capacitance. In order not to violate the peak VDCI current it may be necessary to use the external oscillator OSCEXT to drive an additional switchmode boost regulator, as shown in Figure 8.

Following the above described start sequence, normal boost operation is performed by the converter. VDCO output voltage is constantly monitored by the Error Comparator. When VDCO voltage drops below the preset value, the Error Comparator switches high and connects the internal 40 KHz oscillator to the gate of the VDCI output driver. When the output voltage reaches the desired level, the Error Comparator inhibits the VDCI output driver until the load on VCCO1 discharges the output filter capacitor to less than the desired output level.

INDUCTOR SELECTION

The available output current from the KickStarter's on-chip DC-DC boost converter is a function of the input voltage, external inductor value, output voltage, and the operating frequency. For most applications, the inductor is the only design variable since the internal oscillator is preset to a fixed value of 40 KHz. The proper inductor must have the following characteristics:

1) The correct inductance value must be selected.
2) The inductor must be able to handle the required peak currents.
3) The inductor must have acceptable series resistance and must not saturate.

When the internal N-channel MOSFET turns on, the current through the inductor rises linearly since:

$di / dt = V / L$ where L is the inductance value

At the end of the on-time, t_{ON}, the peak current, I_{PK} is:

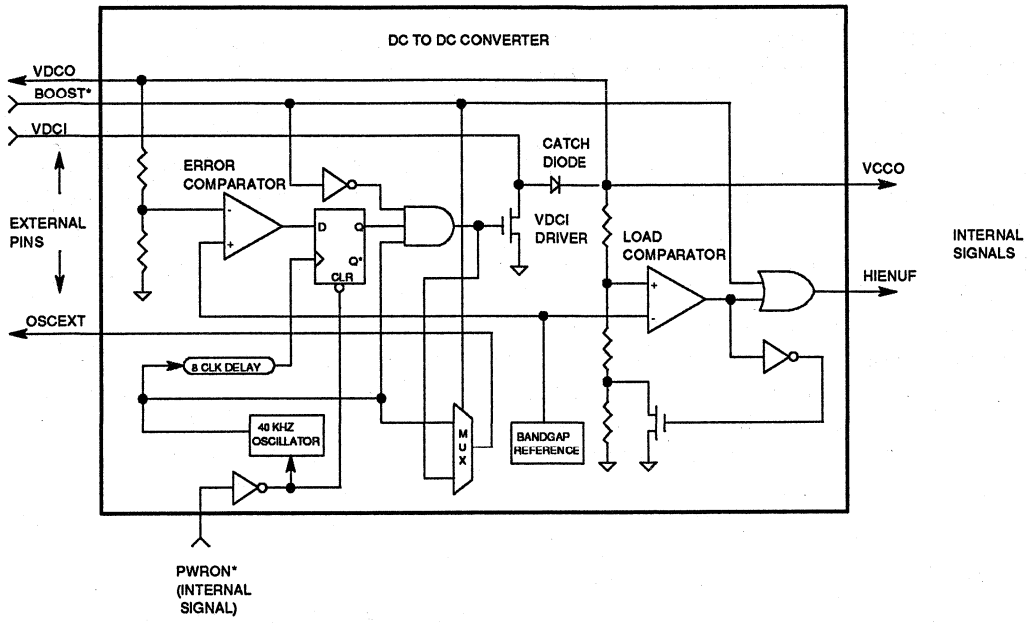
$I_{PK} = V t_{ON} / L$ where: $t_{ON} = 1 / 2 f_o$

The energy in the inductor is:

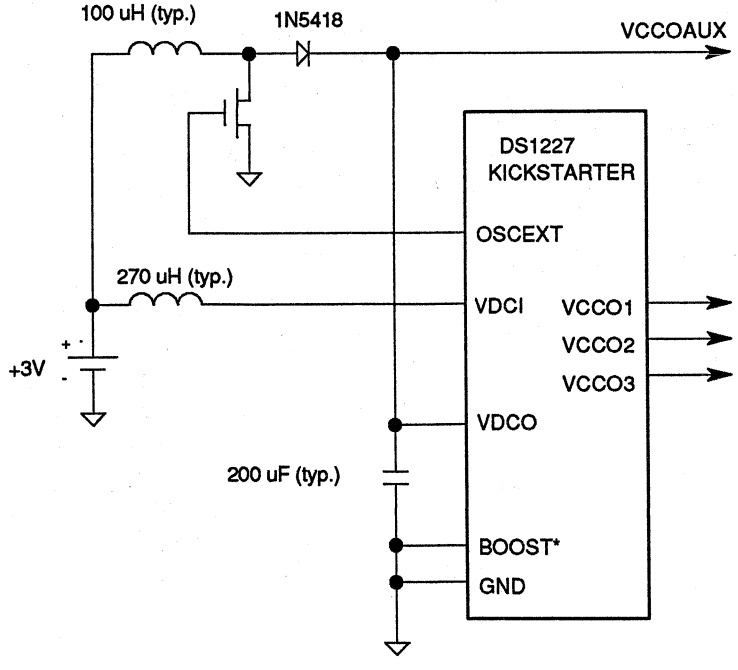
$E_L = L I_{PK}^2 / 2$

At maximum load this cycle is repeated f_0 (typically 40 KHz) times per second, and the power transferred through the coil is $P_L = f_0 \times E_L$. Since the coil only supplies the voltage above the input

DC-DC CONVERTER Figure 7



AUXILIARY BOOST SUPPLY CONFIGURATION Figure 8



voltage:

$$I_{OUT} = P_L / V_{OUT} - V_{IN}$$

The DC-DC converter's output current is provided both by the inductor and directly from the battery. If the load draws less than the maximum current, the VDCI N-channel MOSFET is turned on only often enough to keep the output voltage at the desired level.

If the selected inductor has too high a value, the DS1227 will not be able to deliver the desired output power, even with the MOSFET turned on for every oscillator cycle. The available output power can be increased by either raising the input voltage or lowering the inductance. This causes the current to rise at a faster rate and results in a higher peak current at the end of each cycle. The available output power increases since it is proportional to the square of the peak inductor current. The maximum inductance therefore is:

$$L_{MAX} = V_{IN}^2 / 8 f_o P_L$$

since: $P_L = L I_{PK}^2 f_o / 2$ and:

$$I_{PK} = V_{IN} / 2 f_o L$$

The required output power must include what is dissipated in the forward drop of the catch diode and each of the VCCO1, VCCO2, and VCCO3 pass transistors. This can be expressed as follows:

$$P_{OUT} = V_F I_{OUT} + (I_{OUT1}^2 R_{ON1} + I_{OUT2}^2 R_{ON2} + I_{OUT3}^2 R_{ON3} + I_{OUT4}^2 R_{ON4}) + V_{OUT} I_{OUT}$$

$$= P_L = V_F I_{OUT}$$

where:

$$I_{OUT} = I_{OUT1} + I_{OUT2} + I_{OUT3} + I_{OUT4}$$

If the inductance value is too low, the current at V_{DCI} may rise above the maximum rating. The minimum allowed inductor value is expressed by:

$$L_{MIN} = V_{IN} / 2 f_o I_{MAX} \quad (I_{MAX} = 450 \text{ mA})$$

TYPES OF INDUCTORS

The following is a brief discussion of various types of inductors which can be used with the DS1227 KickStarter to facilitate boost mode operation. Table 1 lists some manufacturers of these types of inductors. Table 2 summarizes performance of the circuit for various inductors.

Molded Inductors

These are cylindrically wound coils which look similar to 1 watt resistors. They have the advantages of low cost and ease of handling, but have higher resistance, higher losses, and lower power handling capability than other types of inductors.

Potted Toroidal Inductors

A typical 1 mH, 0.82 ohm potted toroidal inductor (Dale TE-3Q4TA) is 0.685" in diameter by 0.385" high and mounts directly onto a printed circuit board by its leads. Such devices offer high efficiency and mounting ease, but at a somewhat higher cost than molded inductors.

Ferrite Cores (Pot Cores)

Pot cores are very popular as switch-mode power supply applications since they offer high performance and ease of design. The coils are generally wound on a plastic bobbin, which is then placed between two pot core sections. A simple clip to hold the core sections together completes the inductor. Smaller pot cores mount directly onto printed circuit boards via the bobbin terminals. Cores come in a wide variety of sizes often with the center posts ground down to provide an air gap. The gap prevents saturation while accurately defining the inductance per turn squared.

Pot cores are suitable for all DC-DC converters, but are usually used in the higher power applications. They are also useful for experimentation since it is easy to wind coils onto the plastic bobbins.

Toroidal Cores

In volume production, the toroidal core offers high performance, low size and weight, and low cost. They are, however, slightly more difficult for prototyping, in that manually winding turns onto a toroid is more tedious than on the plastic bobbins used with pot cores. Toroids are more efficient for a given size since the flux is more evenly distributed than in a pot core, where the effective core area differs between the post, side, top, and bottom.

Since it is difficult to gap a toroid, manufacturers produce toroids using a mixture of ferromagnetic powder (typically iron or Mo-Permalloy powder) and a binder. The permeability is controlled by varying the amount of binder, which changes the effective gap between the ferromagnetic particles. Mo-Permally powder (MFP) cores have lower losses and are recommended for the highest efficiency, while iron powder cores are lower cost.

COIL AND CORE MANUFACTURERS Table 1

TYPE	TYPICAL MANUFACTURER	PART #	DESCRIPTION
Molded	Dale	1HA-104	500 uH, 0.5 ohms
"	Cadell-Burns	7070-29	220 uH, 0.55 ohms
"	Gowanda	1B253	250 uH, 0.44 ohms
"	Nytronics	WEE-470	470 uH, 10 ohms
"	TRW	LL-500	500 uH, 0.75 ohms
Potted Toroidal	Dale	TE-3Q4TA	1 mH, 0.82 ohms
"	Gowanda	050AT1003	100 uH, 0.05 ohms
"	TRW	MH-1	600 uH, 1.9 ohms
"	Torotel Prod.	PT 53-18	500 uH, 5 ohms
Toroidal Core	Allen	T0451S100A	500 nH/T²
"	Bradley		
	Siemans	B64290-K38-X38	4 uH/T²
"	Magnetics	555130	53 nH/T²
Ferrite Core	Stackpole	57-3215	14 mm x 8 mm
"	Magnetics	G-41408-25	14 x 8, 250 nH/T²

Note: This list does not constitute an endorsement by Dallas Semiconductor and is not intended to be a comprehensive list of all manufacturers of these components.

INDUCTOR SELECTION FOR COMMON DESIGNS Table 2

VIN (V)	VDCO (V)	I_{OUT} (mA)	EFF. (%)	INDUCTOR		
				PART #	uH	Ohms
2	5	5	78	CB 6860-21	470	0.4
2	5	10	74	G 1B253	250	0.44
2	5	15	61	G 1B103	100	0.25
3	5	25	82	CB 6860-21	470	0.4
3	5	40	75	CB 7070-29	220	0.55

Note: CB = Cadell-Burns, NY (516) - 746 -2310
G = Gowanda Electronics Corp., NY (716) - 532-2234
Other manufacturers listed in Table 1

OUTPUT FILTER CAPACITOR

In boost regulation mode, the DS1227's output voltage ripple on VDCO has two components, with approximately 90° phase difference between them. One component is created by the change in the capacitor's stored charge with each output pulse. The other ripple component is the product of the capacitor's charge/discharge current and its ESR (Effective Series Resistance). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is generally larger than that caused by the change in charge.

$V_{ESR} = I_{PK} \times ESR = (V_{IN} / 2Lf_o) \times ESR$ (Volts p-p)

Where V_{IN} is the coil input voltage, L is its inductance, f_o is the oscillator frequency, and ESR is the equivalent series resistance of the filter capacitor.

The output ripple resulting from the change in charge on the filter capacitor is:

$V_{dQ} = Q / C$, where $Q = t_{DIS} \times I_{peak} / 2$

and $I_{peak} = t_{CHG} \times V_{IN} / L$ V_{dQ}
$= (V_{IN} \times t_{CHG} \times t_{DIS}) / 2LC$

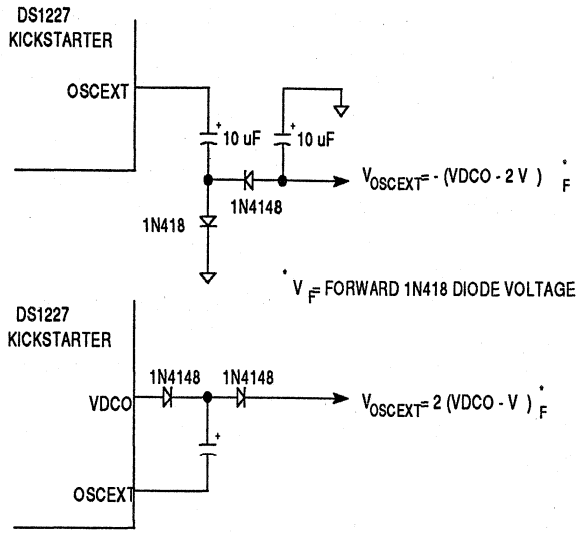
Where t_{CHG} and t_{DIS} are the charge and discharge times for the inductor ($1 / 2f_o$ can be used for nominal calculations).

High quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved in the 100 to 500 uF range, in parallel with a 0.1 uF ceramic capacitor.

OSCEXT FUNCTIONS

The OSCEXT pin is connected to the internal 40 KHz oscillator (nominal frequency). When Boost mode is enabled (BOOST* = 0) and the DC-to-DC converter is running, OSCEXT is active at the same time whenever the Error Comparator is switched high, i.e., whenever the internal oscillator is enabled to the gate of the VDCI driver. In this configuration it can be used to drive an auxiliary switch mode boost regulator as shown in Figure 8. In this circuit, OSCEXT drives an external NMOS switch with its drain pin connected to an additional inductor and filter capacitor as well as an external catch diode. The amount of supply current which can be realized at the +5V output is determined by the power ratings of the external components. Through proper selection of these components, more supply current can be realized than is

VOLTAGE INVERTER AND DOUBLE CONFIGURATIONS Figure 9



possible using the KickStarter's internal VDCI driver and catch diode.

When the Pass-Through mode is enabled (BOOST* = 1) and at least one of the VCCO outputs is switched on, the OSCEXT pin will be continuously driven with the 40 KHz frequency. In this configuration this pin could potentially be used to generate negative or doubled voltages as shown in Figure 9.

APPLICATION BRIEF

The schematic shown in Figure 10 illustrates a typical application of the DS1227 KickStarter in a microcontroller-based, battery-powered system. Together with the KickStarter, the system incorporates a DS5000FP Micro Chip, a DS1283 Watchdog Timekeeper, and a DS1275 Line-Powered RS-232 Transceiver. Although the system is not designed to serve a specific application, this chip set could serve the majority of requirements for many types of hand-held instruments.

The illustrated configuration provides the following major features:

- -Permanently powered operation from a +3V source for many applications
- -Data and event logging with time stamp and date
- -Reprogrammable through RS-232 serial interface
- -Buttonless (autonomous) operation for many tasks

COMPONENT DESCRIPTION

The DS5000FP is an 8-bit microcontroller which is instruction set compatible with the industry standard 8051. It provides an embedded interface to 32 Kbytes of nonvolatile static RAM which can be dynamically partitioned for program and data storage and can be loaded at any time via the on-chip serial port. With proper selection of RAM and the backup lithium source, nonvolatile storage can be maintained for over 10 years in the absence of V_{CC}. The DS5000FP

offers the standard low-power operating and standby modes (i.e., Idle, Stop). More importantly, sophisticated crashproof circuitry in conjunction with the lithium energy source allows it to retain its entire operating state for the duration of a power outage without drawing current from its V_{CC} line.

Timekeeping is provided by the DS1283 Watchdog Timekeeper. Incorporating a self-contained clock and calendar, the DS1283 tracks hundredths of seconds, seconds, minutes, hours, days, date of the month, month, and years. When its chip enable is inactive (no read or write), the DS1283 consumes extremely low current; typically 500 nA. Two alarm functions are provided: a Time of Day Alarm, and a Watchdog Alarm. The Time of Day Alarm can generate an interrupt pulse up to one week in advance of the current time. The Watchdog Alarm can produce an interrupt at regular intervals ranging from .01 seconds to 99.99 seconds. Both alarms function when the part is operating in low-power standby mode.

The DS1275 Line-Powered RS-232 Transceiver allows the instrument to communicate with the RS-232 port on a host computer (e.g., COM port on an IBM PC). It operates from a +5V supply and draws no power from the instrument's main energy source to create negative voltages. Instead, it steals power from the incoming RXD line to generate the negative voltages needed during transmission.

INSTRUMENT OPERATION

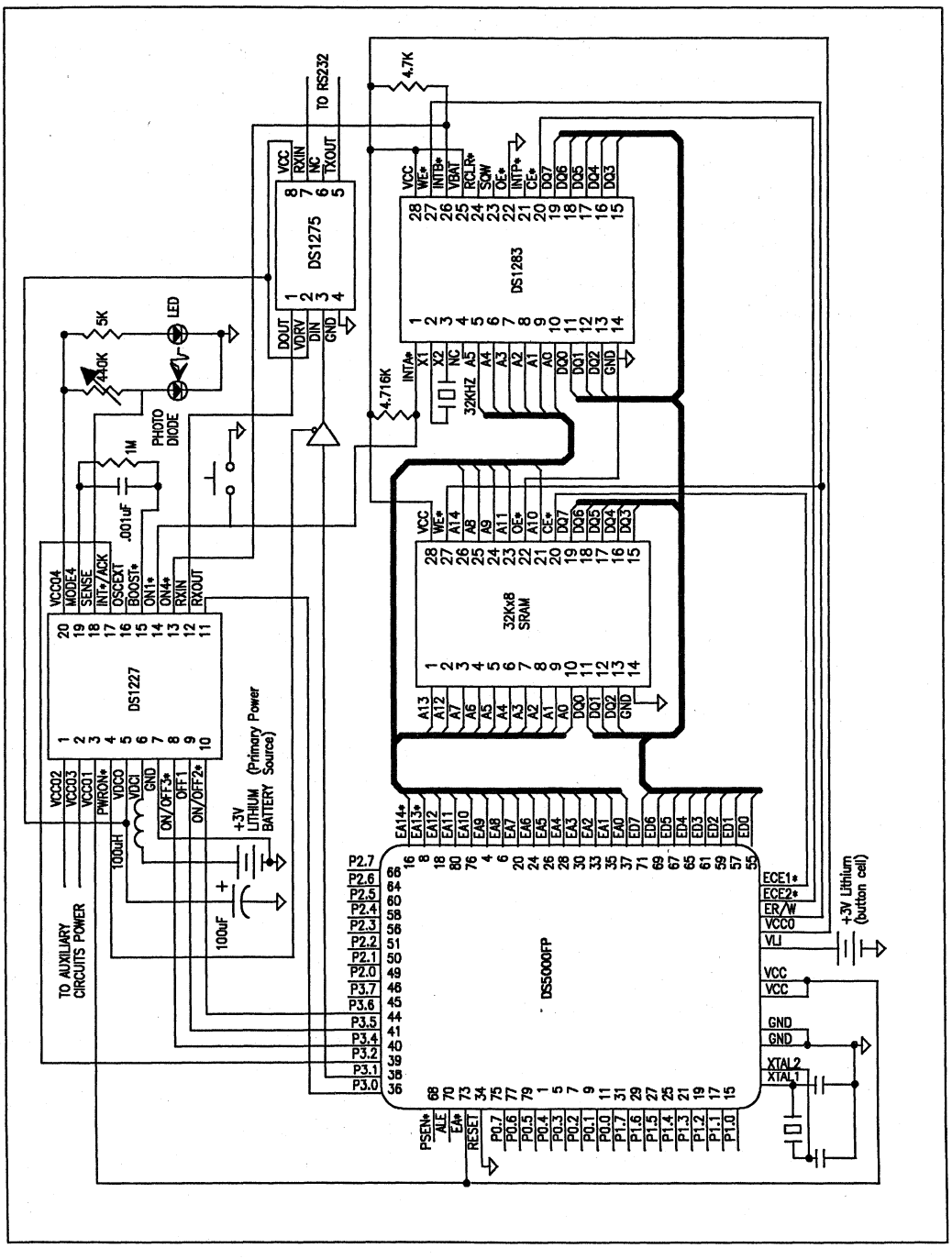
A common requirement of instruments is event logging with time stamp and date. The Dallas chip set provides this capability using the DS5000FP and DS1283. The DS1283 interfaces directly to the DS5000FP embedded bus, and can be accessed by CE2*. In this way, valuable port pins are conserved. Events can be recorded by the microcontroller and logged in RAM with the date and time. In the absence of V_{CC}, the data will be retained in RAM by the backup lithium cell. The same energy cell provides backup to the DS1283, so that timekeeping is maintained in the absence of a primary energy source. Therefore, events can be time stamped and dated with confidence that the correct time has been maintained. Backup lithium current is managed by the DS5000FP and is distributed from the V_{CCO} line in the absence of V_{CC}.

PERMANENTLY POWERED OPERATION

In order to achieve permanently powered operation, Dallas Semiconductor uses several techniques which conserve the life of a primary energy source. First, the illustrated chip set operates at extremely low power. These components are also capable of very low-power data retention. Second, the crashproof circuitry of the DS5000FP allows V_{CC} to be removed and restored without disruption. This allows the energy management circuits of the KickStarter to power down the microcontroller during periods when it is unused. Since the DS1227 can monitor external events and "wakeup" the DS5000FP as necessary, the microcontroller and other circuitry can remain in low-power data retention mode until needed. The DS5000FP, RAM and DS1283 will be backed up via the button cell as show in Figure 1. Finally, the KickStarter allows software-controlled powering of auxiliary circuits when tasks require them.

Low operating power is a basic requirement of battery-operated systems. The illustrated Dallas chip set can perform most instrument functions using minimal power. Using a 3.57 MHz crystal, the circuit in Figure 1 will draw approximately 8 mA during microcontroller operation. When the KickStarter turns off the DS5000FP, the circuit draws approximately 5 uA from the primary energy source. If a similar configuration were created with an ordinary CMOS microcontroller in stop mode, the current could be as high as 55

TYPICAL APPLICATION OF DS1227 KICKSTARTER Figure 10



uA. Idle mode operation would consume approximately 3 mA, which would excessively drain a primary power source over extended periods. The Dallas low-power chip set provides a ten to one improvement over previously available alternatives.

Achieving the lowest power instrument requires the DS1227 KickStarter. Using the KickStarter, low-power operation is achieved by powering down the microcontroller. When this occurs, the DS5000FP effectively consumes no power. RAM and key registers are backed by the lithium button cell with no power draw from V_{CC}. When a task must be performed, the KickStarter powers up the DS5000FP to execute a function and powers it down when the function is complete (under software direction). The period for which power remains on is minimized in this way. Since most tasks require minimal processing time with long periods of waiting, the instrument may remain in a low power data retention mode for the majority of time. Therefore, even if an operator interface is necessary, the microcontroller can remain on for milliseconds (or microseconds) to perform a task and remain off for the seconds between operations.

The ability to react to external stimuli allows the instrument to operate autonomously for many applications. Fundamental to this operation is the kickstart caused by external stimuli. The following section describes the operation of the KickStarter with respect to four different stimuli.

KICKSTARTING OPERATION

The DS1227 receives primary power from a +3V lithium battery. Prior to a kickstart, battery voltage is present on V_{DCO}, which is the main voltage output. When the system receives a kickstart stimulus, an on-chip boost regulator raises V_{DCO} to +5V. Upon completion of power-up, +5V is switched to the DS5000FP on V_{CCO1}. Prior to kickstart, no power was supplied to this line.

The schematic in Figure 10 demonstrates four kickstart stimuli. They are real time clock alarm, RS-232 incoming data, a sensor input, and a user switch. During the low power standby prior to kickstart, V_{CCO} from the DS5000FP provides battery power to the RAM and real time clock from the button cell. V_{DCO} supplies the RS-232 tranceiver. While operating on battery power, the RTC can still issue alarms. If a time of day alarm is programmed, INTA* will be taken low by the RTC when the alarm occurs. This is connected to ON1*, and issues a kickstart.

Incoming RS-232 activity will allow the transceiver to kickstart the DS1227. Following the initial interrupt, all additional RS-232 data is passed through the RXIN/RXOUT pins of the DS1227 to the DS5000FP without further action. In this way, the instrument can collect a table of data and dump it to a PC for analysis when necessary. Since the instrument will kickstart when it detects RS-232 communication, it is unnecessary for an operator to take further action. Enough time should be allowed for the DS5000FP to complete a power-on reset before sending meaningful data.

Two additional methods of kickstarting are illustrated. One method involves the use of a sampled sensor. A periodic pulse (the watchdog alarm) from the DS1283 causes V_{CCO4} to be applied to the LED. For example, this might occur every 250 ms. It remains on for the time it takes to charge the capacitor on MODE4 to 1/2 V_{DCO} (1.5V). In this example, the on period is approximately 75 usec. Just prior to removing V_{CCO4}, the sense line is sampled. If the LED light path to the photodiode is blocked, the sense line will be high and the system will be kickstarted. If the light path is clear, the sense line will be low, and nothing will happen. This facilitates checking for the presence of an ID card in a reader. In the other method a user switch, which is momentarily closed, will start the system. This is tied to ON1* in a wired-OR configuration. All of

the above kickstart stimuli cause the boost regulator to raise V_{DCO} and turn on V_{CC01}. In summary, the four kickstart stimuli are:

1) Time of Day Alarm - INTA* goes low and kickstarts V_{CC01}.
2) RS-232 Activity - Powers up V_{CC01}, and routes all RS-232 straight through to the DS5000FP.
3) INTB* goes low periodically, V_{CC04} turns on, and the sense line is sampled. If high, a kickstart occurs. If low, no action.
4) A user switch momentarily pulls ON1* low and kickstarts.

Although the user switch is easily implemented, it may be unnecessary. By allowing the instrument to power up and determine the cause of the kickstart, it is possible to achieve buttonless operation in many applications. Automatic response allows the instrument to function autonomously and save power by turning off unused circuits.

Once the DS5000FP receives power, it must read the INT*/ACK line (tied to INT0*). A power-on condition causes this signal to be low. The DS5000FP port pin should then acknowledge power-up by driving this line high. This recognizes the interrupt, and enables the KickStarter for further activity. The DS5000FP can now turn on auxiliary loads V_{CC02} and V_{CC03} using ON\OFF 2 and 3 (tied to any port pins). These auxiliary supplies can supply circuits which are not always necessary (e.g., an A/D converter). Peripheral circuits remain powered down until needed. After an operation is complete, the DS5000FP can turn off the auxiliary circuits. When processing of a task is complete, it can turn itself off using OFF1*. An application may require that an auxiliary circuit remain on when the microcontroller is off. This might occur with an LCD display or dual slope A/D converter. Since the dual slope A/D takes a relatively long period to convert (40-50 ms), the microcontroller can be powered down while waiting.

Since the INT/ACK* line is tied to INT0, additional kickstart stimuli which occur while V_{CC01} is on will cause the DS5000FP to receive an interrupt. This allows the DS5000FP to take action for specific conditions.

Precautions against excessive current drain are taken in this application. For example, the data input to the DS1275 RS-232 transceiver is tri-stated when V_{CC01} is off. This is necessary to prevent a high signal from driving the RS-232 bus and consuming power while the DS5000FP is off. Similar precautions should be taken by the user in designing systems with switched power supplies.

ABSOLUTE MAXIMUM RATINGS *

Input Voltage on any Pin Relative to Ground	-0.3 to +7.0V
V_{DCI} Peak Input Current	450 mA
Power Dissipation:	
Plastic DIP (derate 7.41 mW/°C above +50°C)	555 mW
Small Outline (derate 12.5 mW/°C above +50°C)	937 mW
Operating Temperature	0° to +70° C
Storage Temperature	-55° C to +125° C
Lead Soldering Temperature	260° C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ELECTRICAL CHARACTERISTICS

(t_A = 0° C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Startup Voltage	V_{DCISU}	1.8			V	1
VDCO Voltage Threshold for VCCO Turn-ON	V_{DCON}	4.38	4.50	4.62	V	
VDCO Voltage Threshold for VCCO Turn-OFF	V_{DCOFF}			3.00	V	
Operating Supply Current	I_{CC}					
(Boost\=0)			1.5	3.0	mA	4
(Boost\=1)			0.5	1.0	mA	2
Standby Supply Current	I_{SB}			200	nA	
VCCO1 DC Source Current (V_{CCO1} = V_{DCO} - 0.25V)	I_{CCO1}			100	mA	2, 7
VCCO2, VCCO4 DC Source Current (VCCO2, VCCO4 = V_{DCO} - 0.25V)	I_{CCO2} I_{CCO4}			50	mA	2, 7
V_{CCO3} Source Current (V_{CCO3} = V_{DCO} - 0.25V)	I_{CCO3}			10	mA	2, 7
VCCO1, VCCO2, VCCO3, VCCO4 Voltage	V_{OUTB}	4.75	5.00	5.25	V	1, 4

Continued on next page.

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
VCCO1, VCCO2, VCCO3, VCCO4 Voltage	V_{OUTP}	V_{DCO} - 0.25			V	2
VCCO4 Voltage	V_{OUT4}	V_{DCO} -0.25			V	
VCCO1 ON Resistance	R_{VCCO1}			2.5	Ohms	
VCCO2, VCCO4 ON Resistance	$R_{VCCO2,4}$			5.0	Ohms	
VCCO3 ON Resistance	R_{VCCO3}			25	Ohms	
Efficiency			80		%	1, 8
Line Regulation $+0.5V_{CCO} < +V_S < V_{CCO}$	V_{CCO}			0.4	%	1
Oscillator Frequency			40		KHz	
Oscillator Duty Cycle			50		%	
OSCEXT ON Resistance	R_{OSCEXT}		50	75	Ohms	
VDCI Driver ON Resistance (@ I_{VDCI} = 100 mA)	R_{VDCION}		6	12	Ohms	1
VDCI Driver OFF Leakage Current (t_A = 25° C)	I_{VDCIL}			30	uA	1
Catch Diode Forward Voltage	V_F			1.0	V	
Output Low Voltage, (OSCEXT, PWRON1\) I_{OL} = 1.6 mA	V_{OL}			0.45	V	
Output High Voltage (OSCEXT, PWRON1\) I_{OH} = -80 uA	V_{OH}	2.4			V	
Input Low Current (INT\, ON2/OFF2\, ON3/OFF3\, ON4\, BOOST\)	I_{IL1}	-1.0		1.0	uA	
Input Low Current (ON1\, RXIN)	I_{IL2}	-50			uA	6
Output High Current (PWRON1\)	I_{OH}	-400			uA	
Output Low Current (PWRON1\)	I_{OL}	2.0			mA	

Continued on next page.

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
RXIN Current (V_{RXIN} - V_{RXOUT} ≤ 500 mV)	I_{RXIN}	10			mA	
INT/ACK* Input Transition Current	I_{ACKT}			± 2.0	mA	5
INT/ACK* Input Leakage Current 0.0 ≤ V_{IN} ≤ 0.1, or V_{DCO} - 0.1 ≤ V_{IN} ≤ V_{DCO}	I_{ACKL}			± 200	uA	5
SENSE Resistance (VCCO4 ON)			250		Kohms	
MODE4 Source Current (MODE4 = 0 when ON4\ goes from 1 to 0)	I_{M4ON}	-10	-45	-80	uA	
MODE4 Source Current Shutoff Voltage	V_{M4OFF}		$0.5V_{DCO}$			
MODE4 Discharge Resistance (Following current source shutoff)	R_{M4DIS}			2	Kohms	
MODE4 Discharge Resistance Shutoff Voltage	V_{M4DIS}			$0.1V_{DCO}$		

NOTES:

1. Applicable only when Boost Mode operation is in effect.
2. Applicable only when Pass-Through Mode operation is in effect.
3. Valid when 2.5V ≤ V_{DCO} ≤ 5.0V.
4. Measured with Boost Mode operation in effect; I_{CCO1} = I_{CCO2} = I_{CCO3} = I_{CCO4} = 0. This value represents the amount of current drawn by the DS1227 itself during boost operation and does not include current supplied on the I_{CCO} outputs; nor does it include inefficiencies of DC-DC conversion.
5. Input transition current on the INT/ACK\ pin is specified to indicate the amount of current required to switch the pin from a high to a low or from a low to a high condition. Once the pin has switched states, then the leakage current specification is applicable.
6. ON1\ and RXIN have internal weak p-channel pull-up devices.
7. When BOOST operation is in effect, the total combined current supplied out of VCCO1, VCCO2, VCCO3, and VCCO4 is limited by the V_{DCI} peak current.
8. Actual efficiency is dependent on external discrete component characteristics.

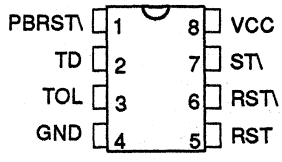
DALLAS SEMICONDUCTOR

DS1232/S
MicroMonitor Chip

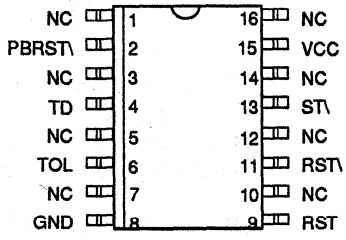
FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space-saving, 8-pin mini-DIP
- Optional 16-pin SOIC surface mount package
- Industrial temperature -40°C to +85°C available, designated N

PIN DESCRIPTION



DS1232 8-Pin DIP
(300 Mil)



DS1232S 16-Pin SOIC
(300 mil)

PIN NAMES (\ Denotes Condition Low)

PBRST\ - Pushbutton Reset Input
TD - Time Delay Set
TOL - Selects 5% or 10% V_{cc} Detect
GND - Ground
RST - Reset Output (Active High)
RST\ - Reset Output (Active Low, Open Drain)
ST\ - Strobe Input
V_{cc} - +5 Volt Power
NC - No Connections

DESCRIPTION

The DS1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{cc}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{cc} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION - POWER MONITOR

The DS1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and RST\ (Pin 6). When TOL is connected to ground, the RST and RST\ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and RST\ signals become active as V_{CC} falls below 4.5 volts. The RST and RST\ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and RST\ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

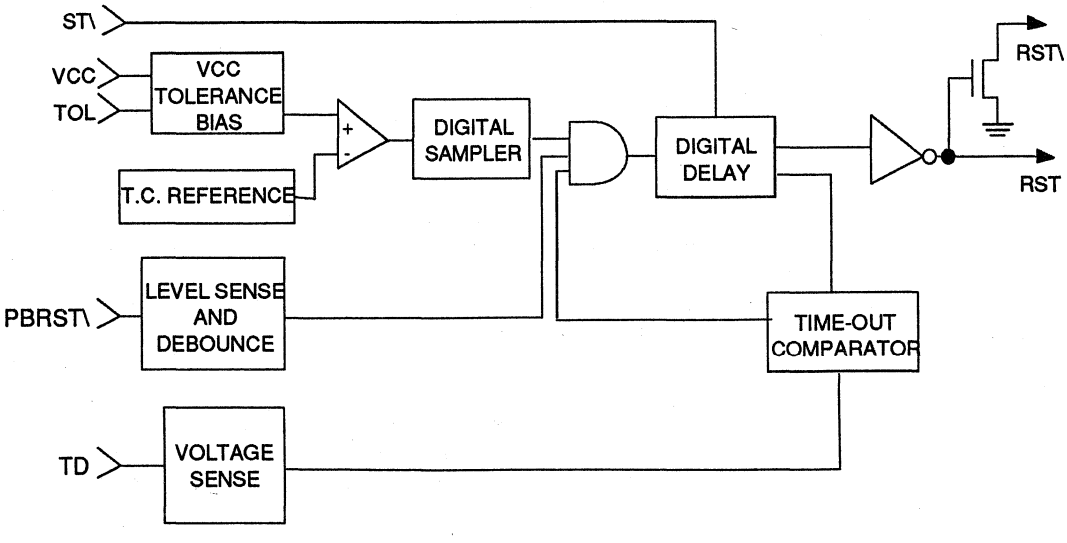
OPERATION - PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and RST\ signals of 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

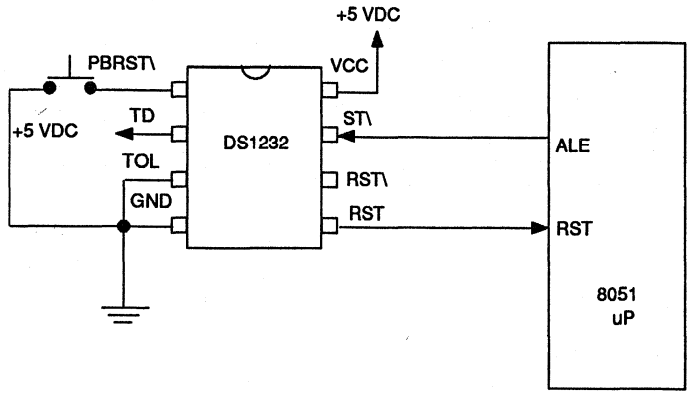
OPERATION - WATCHDOG TIMER

A watchdog timer function forces RST and RST\ signals to the active state when the ST\ input is not stimulated for a predetermined time period. The time period is set by the TD input to be 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and RST\ are inactive. If a high-to-low transition occurs on the ST\ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and RST\ signals are driven to the active state for 250 ms minimum. The ST\ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 3.

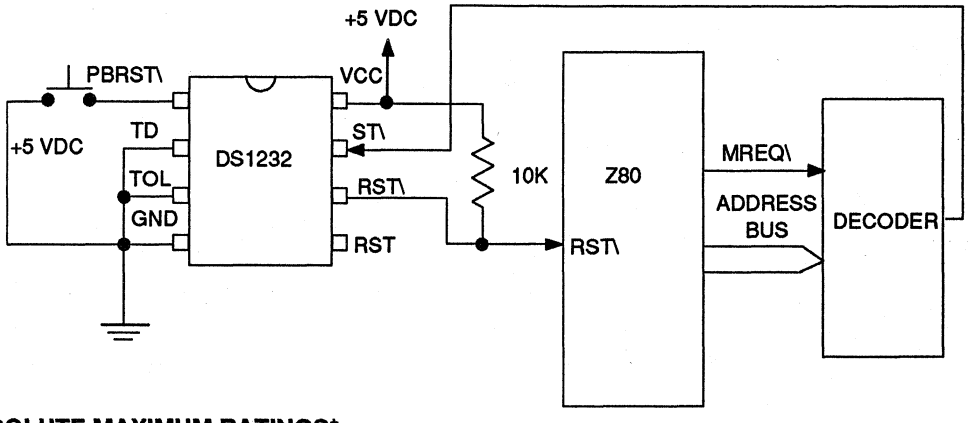
MICROMONITOR BLOCK DIAGRAM Figure 1



PUSHBUTTON RESET Figure 2



WATCHDOG TIMER Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
ST\ and PBRST\ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
ST\ and PBRST\ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0^{o}C$ to $70^{o}C$; V_{CC}=4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	8	10		mA	
Output Voltage @ -500 uA	V_{OH}	V_{CC} - 0.5V	V_{CC} - 0.1V		V	7
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4 .49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

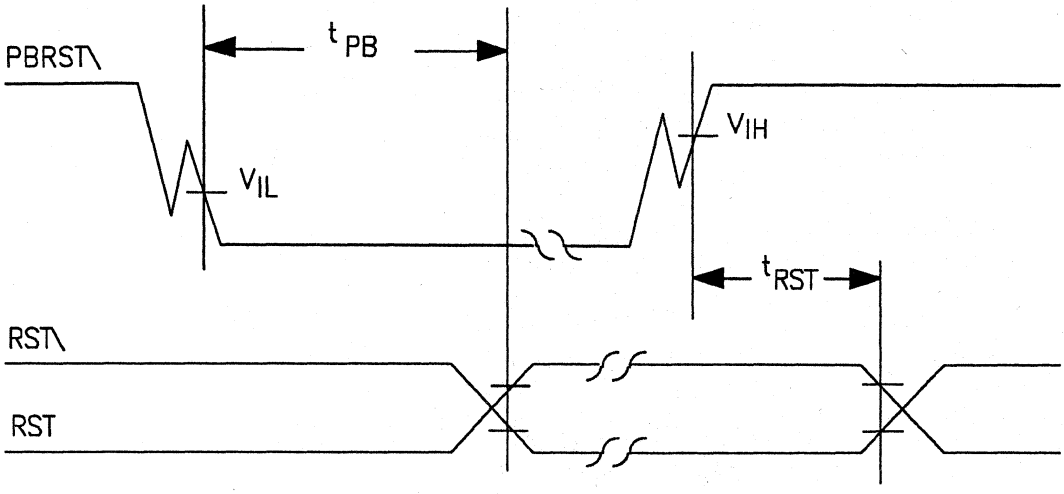
($0^{o}C$ to $70^{o}C$; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PBRST\ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
ST\ Pulse Width	t_{ST}	20			ns	6
V_{CC} Detect to RST and RST\	t_{RPD}			100	ns	
V_{CC} Slew Rate						
4.75V to 4.25V	t_F	300			us	
V_{CC} Detect to RST and RST\	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0			ns	

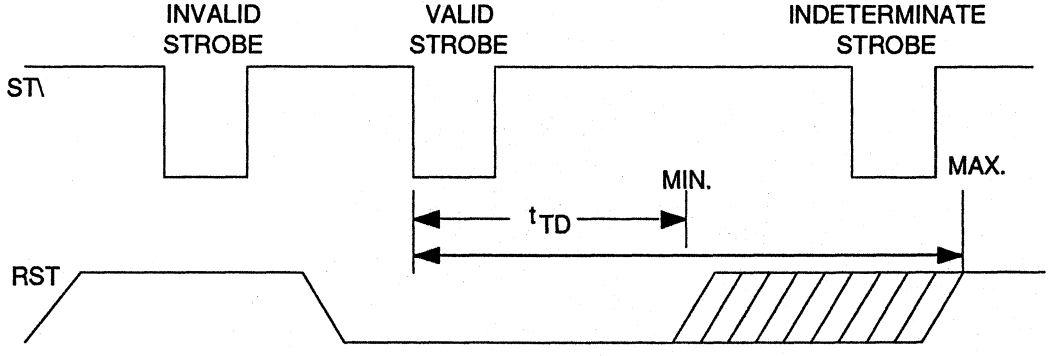
NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. PBRST\ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. t_R = 5 us.
5. RST\ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5 of V_{CC} on power-down until V_{CC} drops below 2.0V. RST\ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.

TIMING DIAGRAM - PUSHBUTTON RESET Figure 4



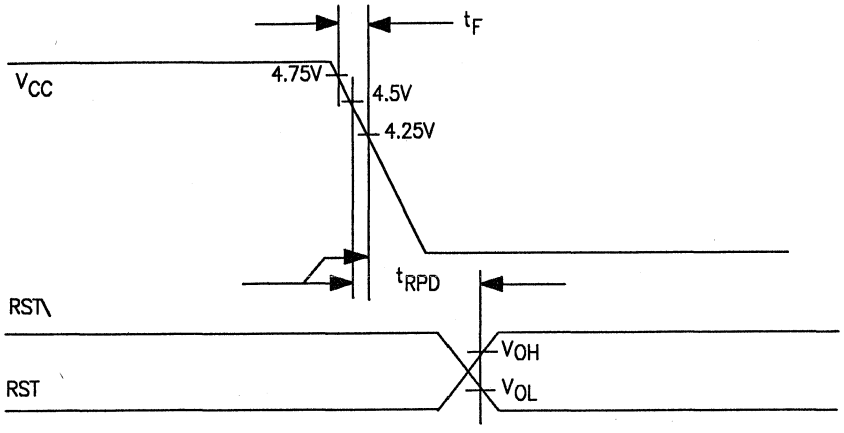
TIMING DIAGRAM - STROBE INPUT Figure 5



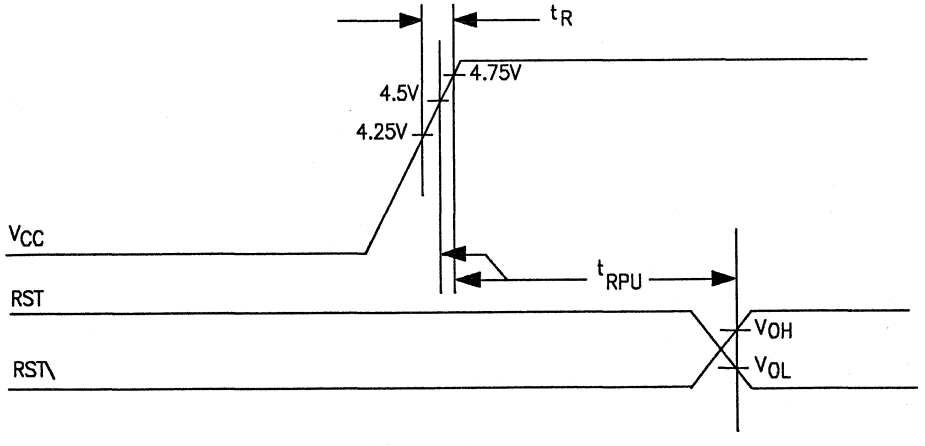
WATCHDOG TIMEOUTS Table 1

	TIMEOUT		
TD	**MIN**	**TYP**	**MAX**
GND	50ms	150ms	250ms
Float	250ms	600ms	1000ms
V_{CC}	400ms	1200ms	2000ms

TIMING DIAGRAM - POWER DOWN Figure 6



TIMING DIAGRAM - POWER UP Figure 7



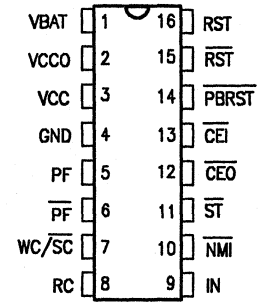
DALLAS SEMICONDUCTOR

DS1236
MicroManager Chip

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors push-button for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN DESCRIPTION



16-Pin DIP
(300 Mil.)

PIN NAMES(\ Denotes Condition Low)

V_{BAT}	+3 Volt Battery Input
V_{CCO}	Switched SRAM Supply Output
V_{CC}	+5 Volt Power Supply Input
GND	Ground
PF	Power Fail (Active High)
PF\	Power Fail (Active Low)
WC/SC	Wake-Up Control (Sleep)
RC	Reset Control
IN	Early Warning Input
NMI\	Non-Maskable Interrupt
ST\	Strobe Input
CEO\	Chip Enable Output
CEI \	Chip Enable Input
PBRST \	Push-Button Reset Input
RST\	Reset Output (Active Low)
RST	Reset Output (Active High)

DESCRIPTION

The DS1236 MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt.

External reset control is provided by a push-button reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and Wake-up/Sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236 is shown in Figure 1.

PIN DESCRIPTION

Pin Name	Description
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
PF\	Power fail indicator, active low.
WC/SC\	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output . Normally low for NMOS processors and high for battery backed CMOS processors.
IN	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
NMI\	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
ST\	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
CEO\	Chip enable output. Used with nonvolatile SRAM applications.
CEI\	Chip enable input.
PBRST\	Push-button reset input.
RST\	Active low reset output.
RST	Active high reset output.

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt (NMI\) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5 volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and RST\ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and RST\ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and RST\ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of intolerance V_{CC}. On power-up, the RST and RST\ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236 provides a watchdog timer function which forces the RST and RST\ signals to the active state when the strobe input (ST\) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum timeout of 600 ms. The watchdog time-out period begins as soon as RST and RST\ are inactive. If a high-to-low transition occurs at the ST\ input prior to time-out, the watchdog timer is reset and begins to time out again. The ST\ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on ST\ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and RST\ outputs are driven to the active state for 25 ms minimum. The ST\ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

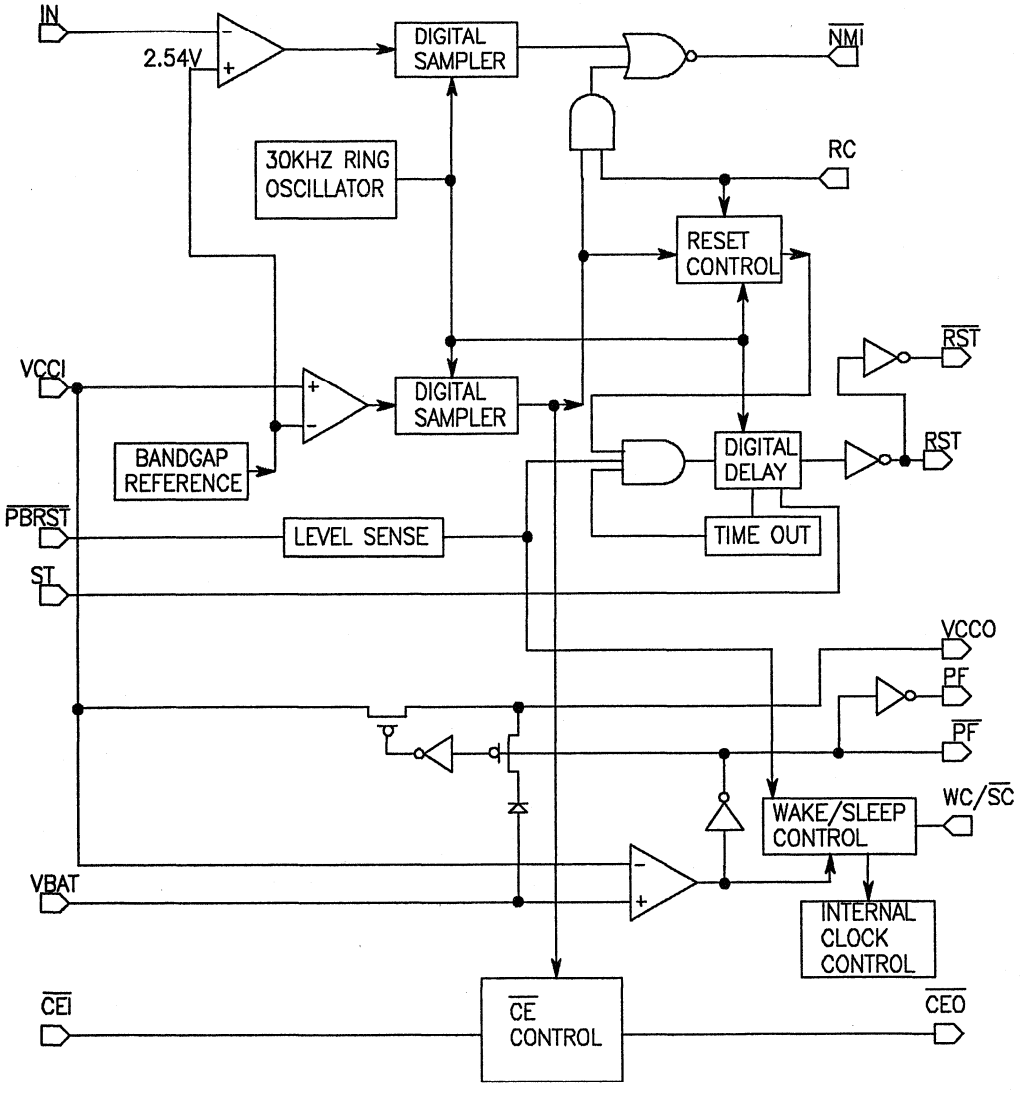
Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an NMI\ output will occur only at power-up, or when the ST\ pin is strobed. As shown in the Figure 3, a falling edge on ST\ will generate an NMI\ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an NMI\ will be returned immediately after the ST\ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC =0).

If the NMI\ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the ST\ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSH-BUTTON RESET

An input pin is provided on the DS1236 for direct connection to a push-button. The push-button reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V_{CC} is greater than V_{BAT}. The PBRST\ pin is also debounced, and timed such that the RST and RST\ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the push-button is released from a low level. A typical example of the power monitor, watchdog timer, and push-button reset connections are shown in Figure 4. The PBRST\ input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The PBRST\ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the PBRST\ generated RST is illustrated in Figure 5.

DS1236 FUNCTIONAL BLOCK DIAGRAM Figure 1



NON-MASKABLE INTERRUPT

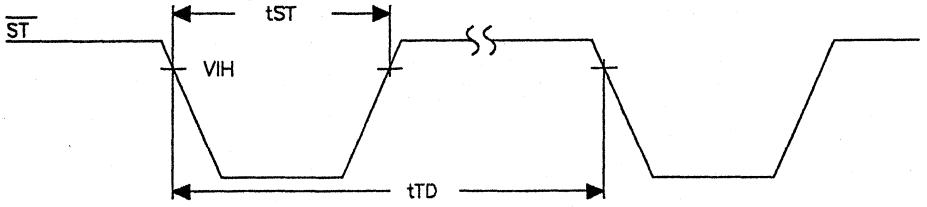
The DS1236 generates a non-maskable interrupt NMI\ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5 volt supply, or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R_1 and R_2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236 requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R_2 high enough to keep power consumption low, and solve for R_1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between NMI\ and RST or RST\.

When the supply being monitored decays to the voltage sense point, the DS1236 pulses the NMI\ output to the active state for a minimum of 200 us. The NMI\ power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 us/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active NMI\. Therefore, the supply must be below the voltage sense point for approximately 100 us or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up , any detected IN pin levels below V_{TP} by the comparator are disabled from reaching the NMI\ pin until V_{CC} rises to V_{CCTP}. As a result, any potential NMI\ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

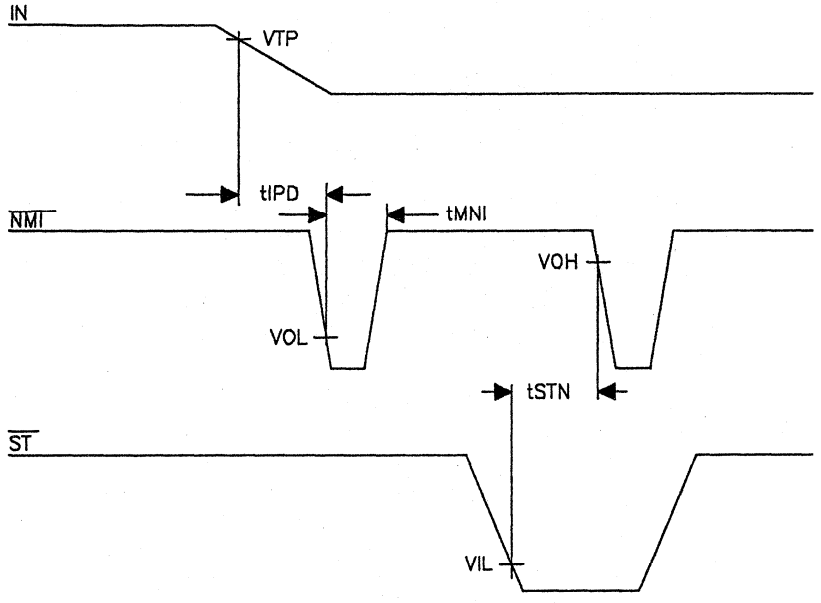
Removal of an active low level on the NMI\ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the NMI\ signal during power-up results in an NMI\ pulse of from 0 us minimum to 500 us maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 us minimum to 500 us maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, NMI\ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the NMI\ to be virtually non-existent on power-up. This is of no consequence, however, since a RST will be active.

If the IN pin is connected to V_{CCO}, the NMI\ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the NMI\ pin. Given that any NMI\ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the NMI\ pin will remain high. The NMI\ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the NMI\ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

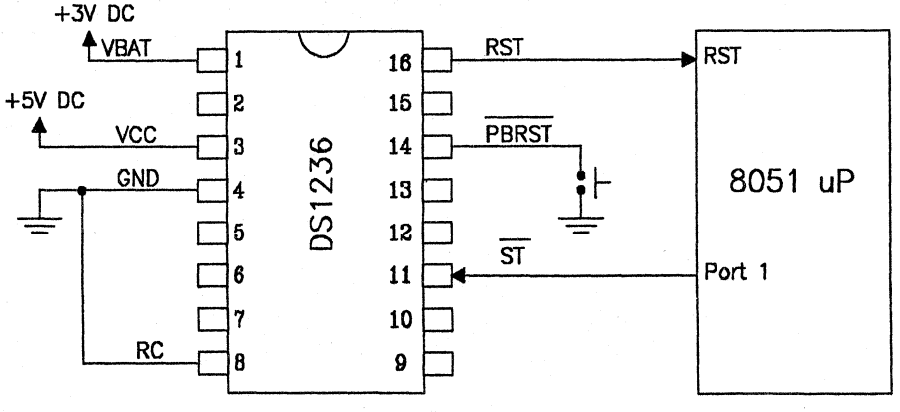
ST/INPUT TIMING Figure 2



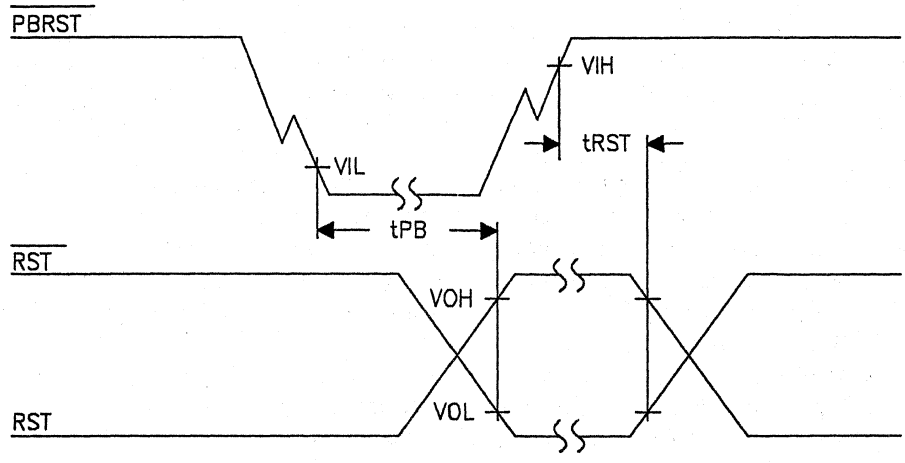
NMI/FROM ST/INPUT Figure 3



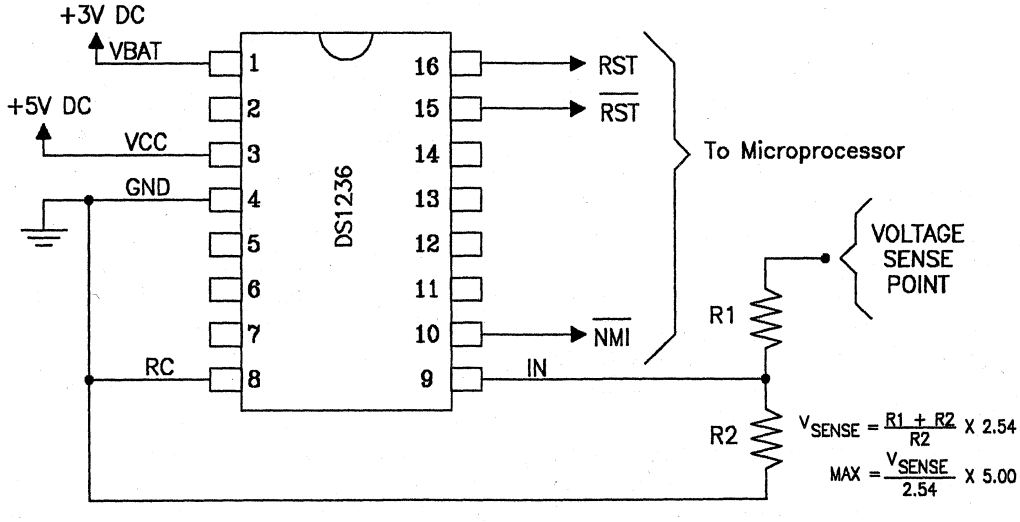
POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10k OHM, V_{SENSE} = 4.80 VOLTS

$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 8.9K \text{ OHM}$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 25.4K \text{ OHM}$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7 \text{ VOLTS}$$

MEMORY BACKUP

The DS1236 provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output (CEO\) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If CEI\ is low at the time power fail detection occurs, CEO\ is held in its present state until CEI\ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If CEO\ is in an inactive state at the time of V_{CC} fail detection, CEO\ will be unconditionally disabled within t_{CF}. During nominal supply conditions CEO\ will follow CEI\ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1236 provides a freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

POWER SWITCHING

When larger operating currents are required in a battery backed system, the 5 volt supply and battery supply switches internal to the DS1236 may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and PF\ outputs are provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power-up. The DS1336 is designed to use the PF\ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and PF\ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

RESET CONTROL

As mentioned above, the DS1236 supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, RST\, and NMI\ outputs for volatile processor operation versus nonvolatile battery back-up or battery operated processor applications.

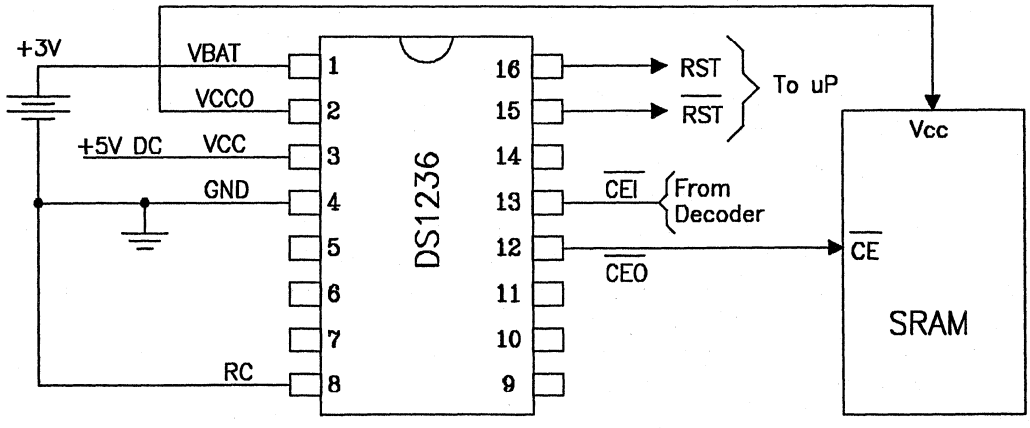
When the RC pin is tied to ground, the DS1236 is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile back-up of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236 are disconnected from the back-up battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the prin-

cipal emphasis is placed on giving early warnings with NMI\, then providing a continuously active RST and RST\ signal during power-down while isolating the back-up battery from the processor during a loss of V_{CC}.

During power-down, NMI\ will pulse low for a minimum of 200 us, and then return high. If RC is tied low (NMOS mode), the voltage on NMI\ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point NMI\ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and RST\ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, RST\ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the NMI\ pin until V_{CC} rises to V_{CCTP}. As a result, any potential NMI\ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the NMI\ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the NMI\ signal results in an NMI\ pulse of 0 us minimum to 500 us maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 us minimum to 500 us maximum. In contrast, if the IN pin is tied to V_{CCO}, NMI\ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power

NONVOLATILE SRAM Figure 7



CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low-power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236 issues no NMI\ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236 provides a pulsed NMI\ for early power failure warning. Waiting to initiate a Stop mode until after the NMI\ pin has returned high will guarantee the processor that no other active NMI\ or RST/RST\ will be issued by the DS1236 until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and RST\. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CC0}, RST and RST\ are not forced active as V_{CC} collapses to V_{CCTP}. The RST\ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from NMI\ at an earlier voltage level. The NMI\ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, NMI\ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and RST\ are held inactive until V_{CC} reaches V_{BAT}, then RST and RST\ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the NMI\ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the ST pin will result in additional NMI\ pulses. In this way, the ST\ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated above in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figures 10, 11, 12, and 13. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 10 illustrates the relationship for power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active NMI\, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236 is in CMOS mode, no reset is generated. The RST\ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, CEO\ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF and PF\ pins.

Figure 11 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an NMI\ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and RST\ are given. The RST voltage will follow V_{CC} as it falls. CEO\, PF, and PF\ will operate in a similar manner to CMOS mode. Notice that the NMI\ will tri-state to prevent a loss of battery power.

Figure 12 shows the power-up sequence for the

NMOS mode. As V_{CC} slews above V_{BAT}, the PF and PF\ pins are deactivated. An active reset occurs as well as an NMI\. Although the NMI\ may be short due to slew rates, reset will be maintained for the standard t_{RST} time-out period. At a later time, if the IN pin falls below V_{TP}, a new NMI\ will occur. If the processor does not issue a ST\, a watchdog reset will also occur. The second NMI\ and RST are provided to illustrate these possibilities.

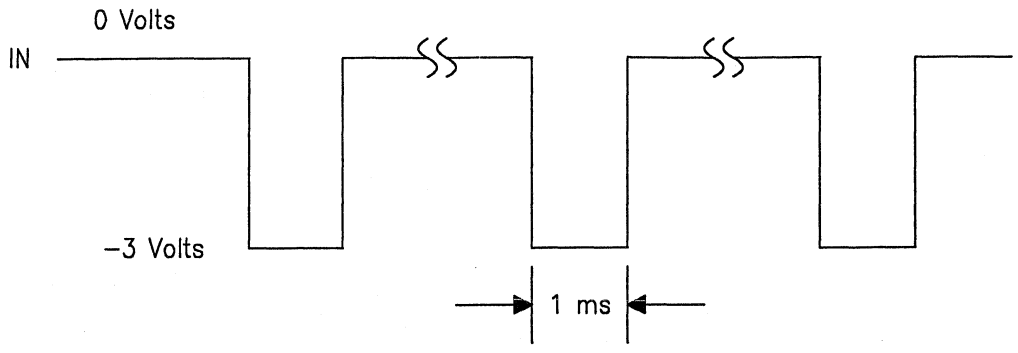
Figure 13 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236 issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the NMI\ may terminate the Stop mode in the processor.

WAKE CONTROL/SLEEP CONTROL

The Wake/Sleep Control input (WC/SC\) allows the processor to disable all comparators on the DS1236 before entering the Stop mode. This feature allows the DS1236, processor, and non-volatile static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 14. The DS1236 may subsequently be restarted by a high to low transition on the PBRST\ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the Watch-dog times out and drives RST and RST\ active. The DS1236 can also be started up by forcing the WC/SC\ pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor and system power is lost, the DS1236 will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 15.

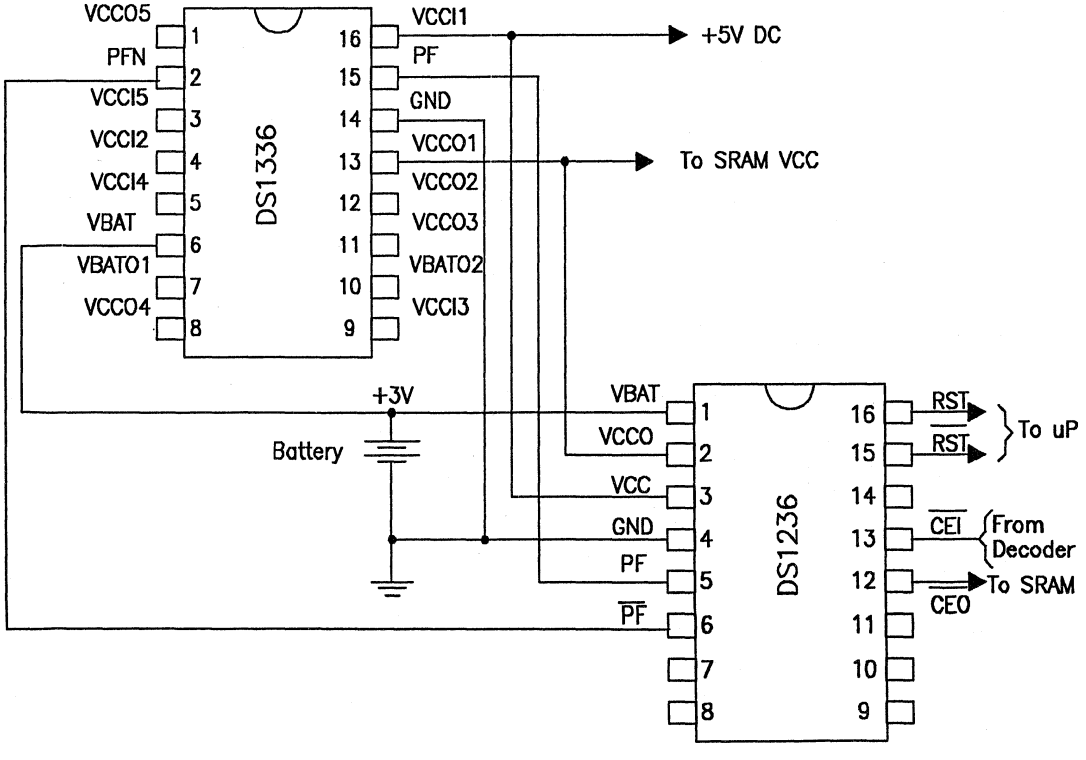
When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236 is disabled, thus leaving the NMI\, RST, and RST\ outputs disabled as well as the ST\ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and RST\ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and RST\ pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the PBRST\ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and RST\ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/SC\ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236.

FRESHNESS SEAL Figure 8

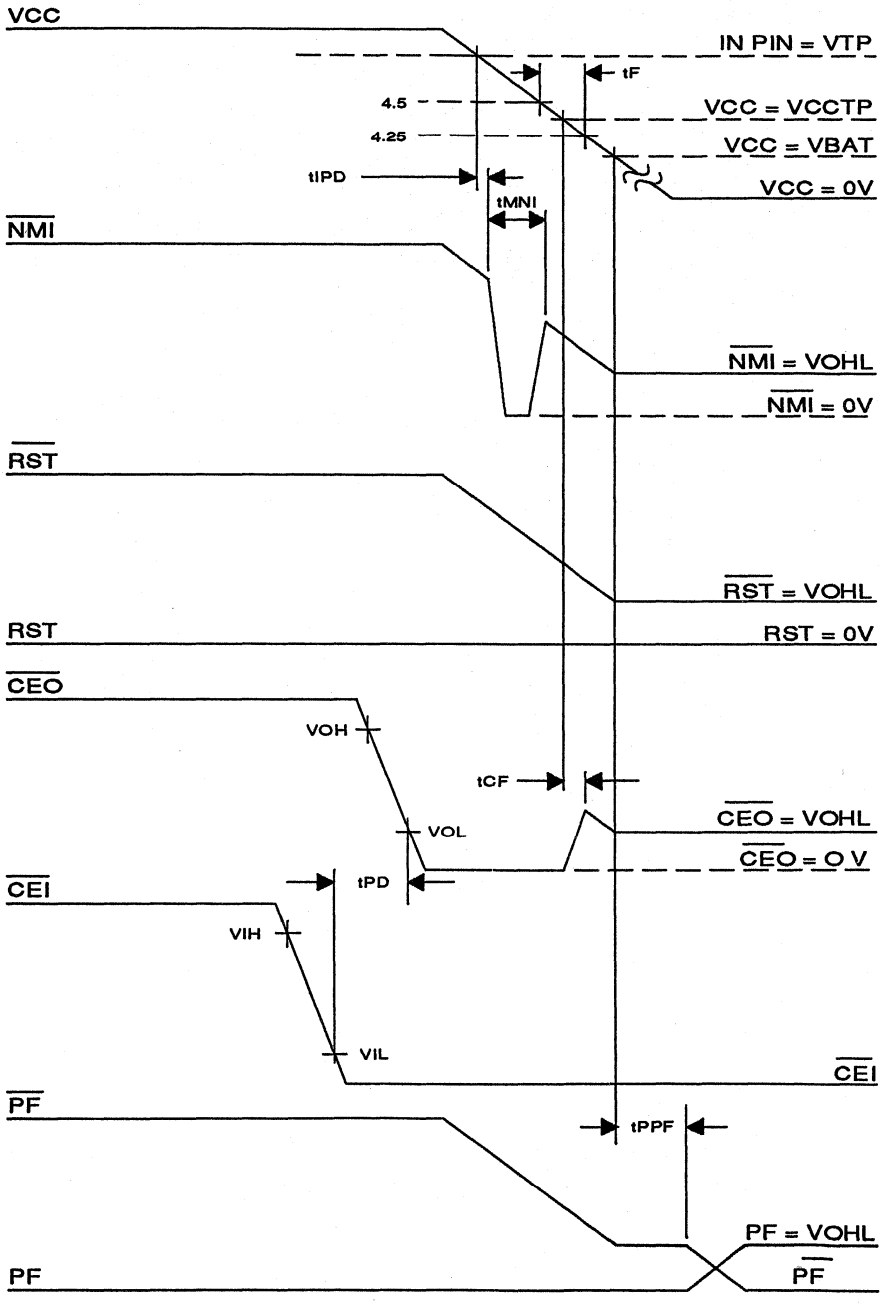


Note: This series of pulses must be applied during normal +5 volt operation.

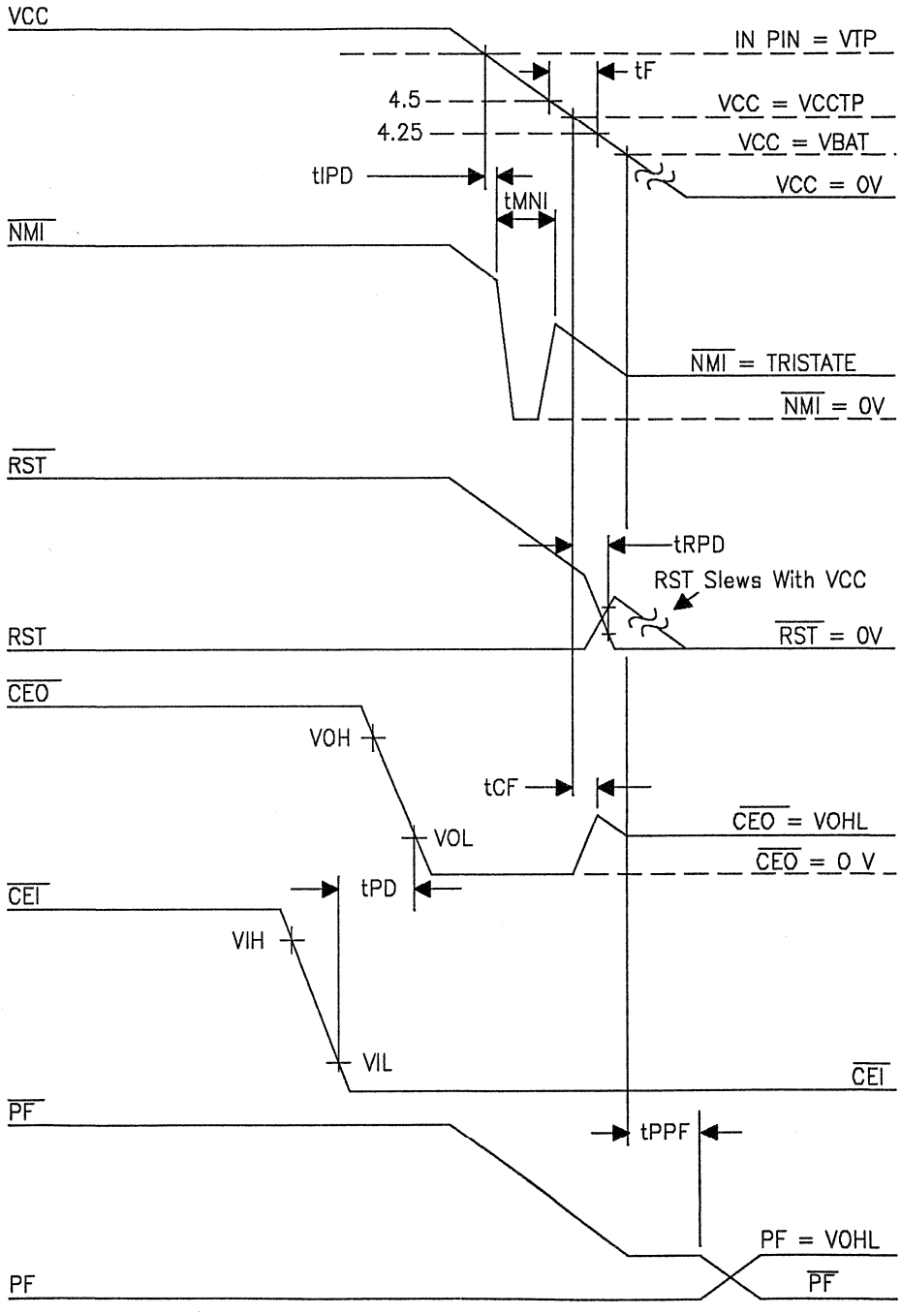
POWER SWITCHING Figure 9



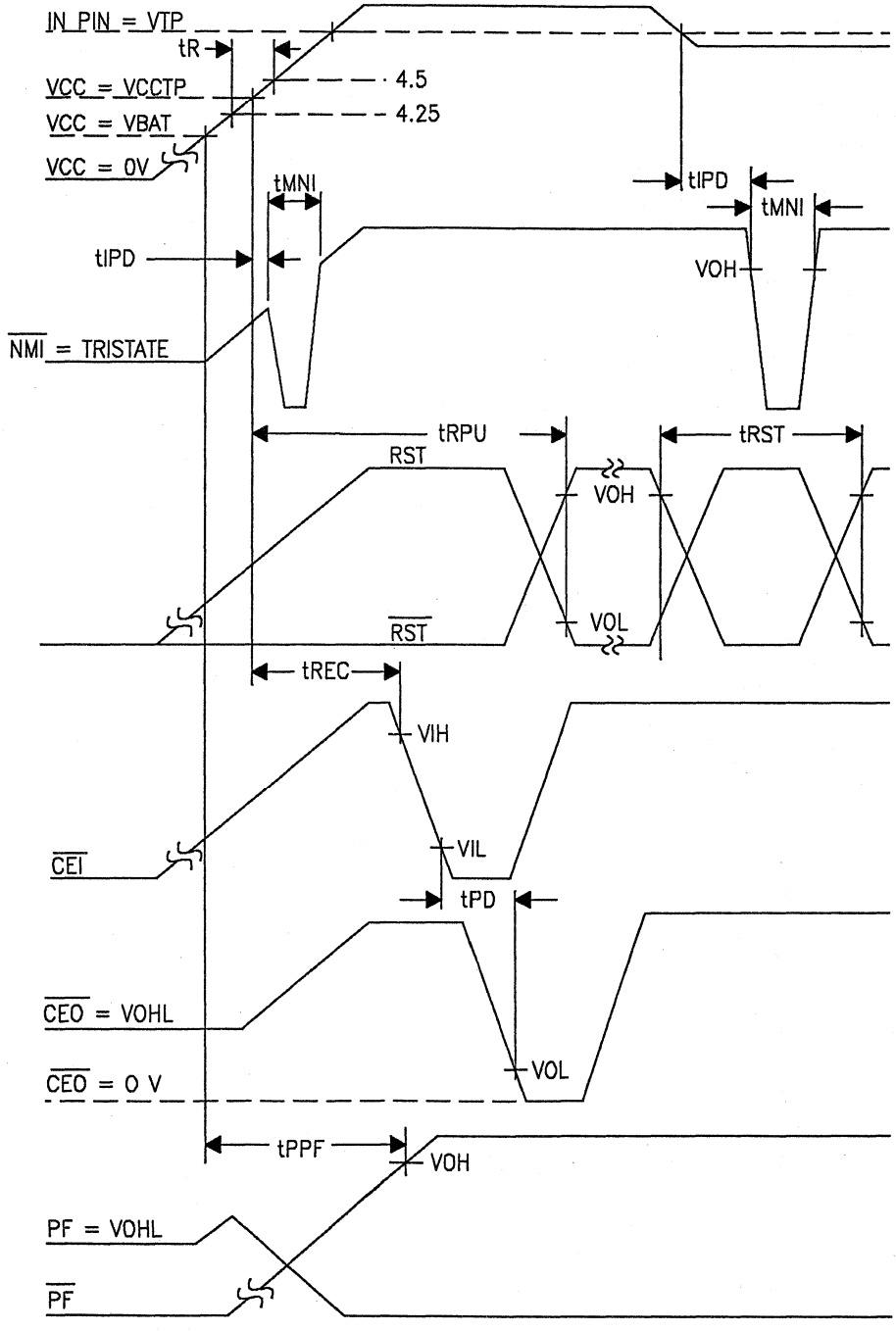
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 10



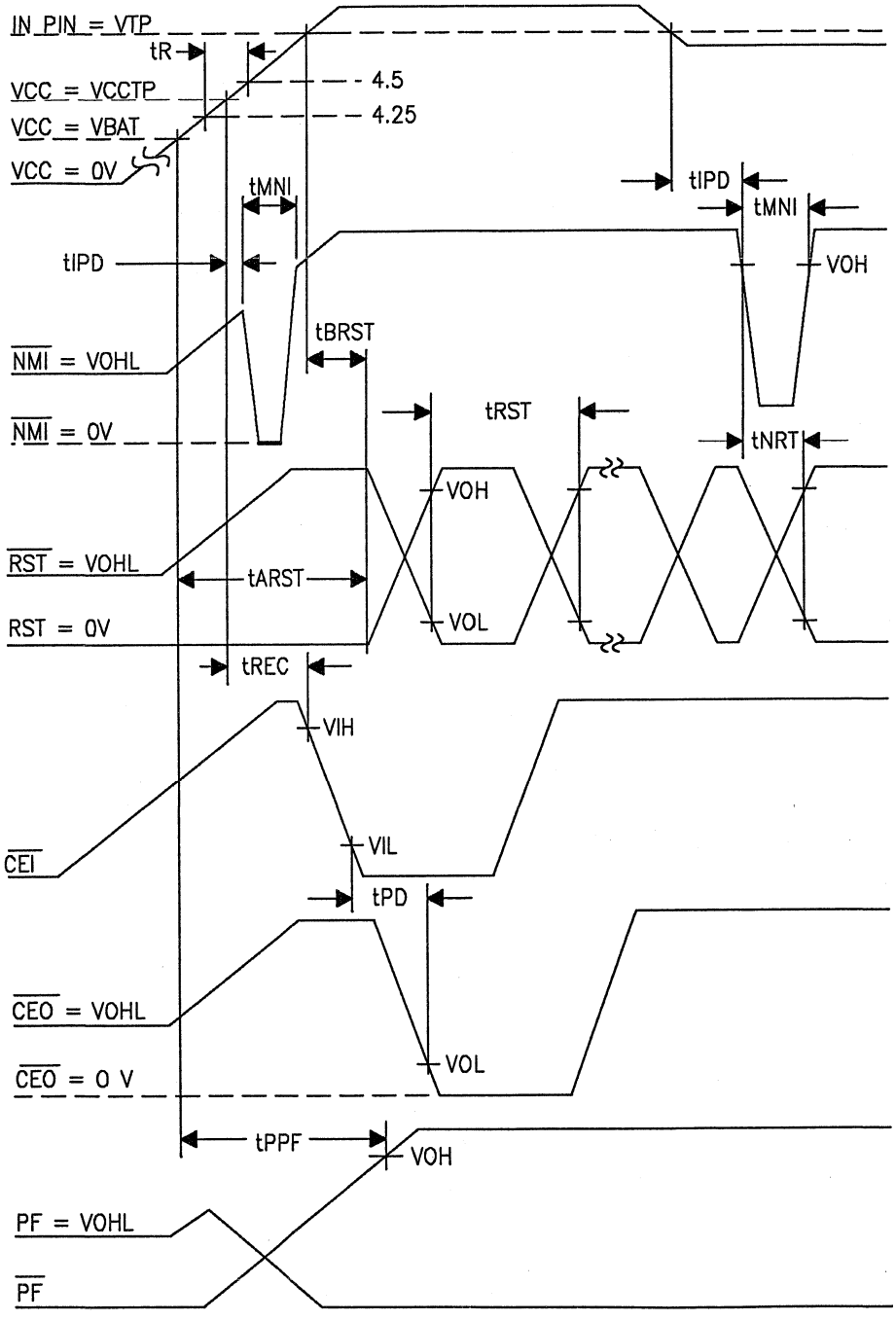
NMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 11



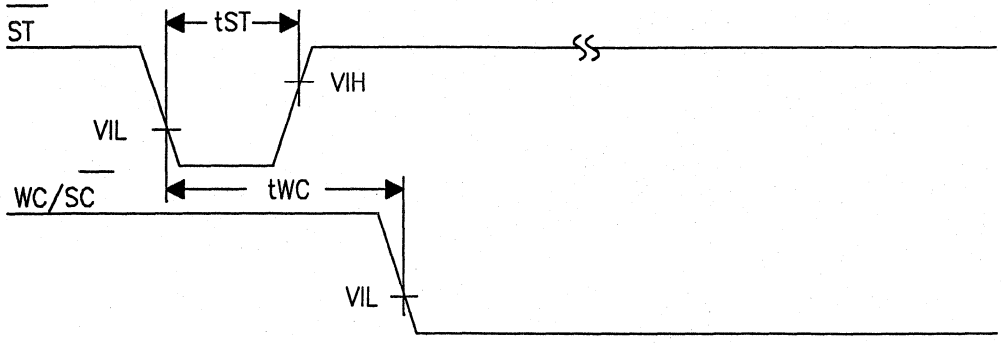
NMOS MODE POWER-UP (RC = GND) Figure 12



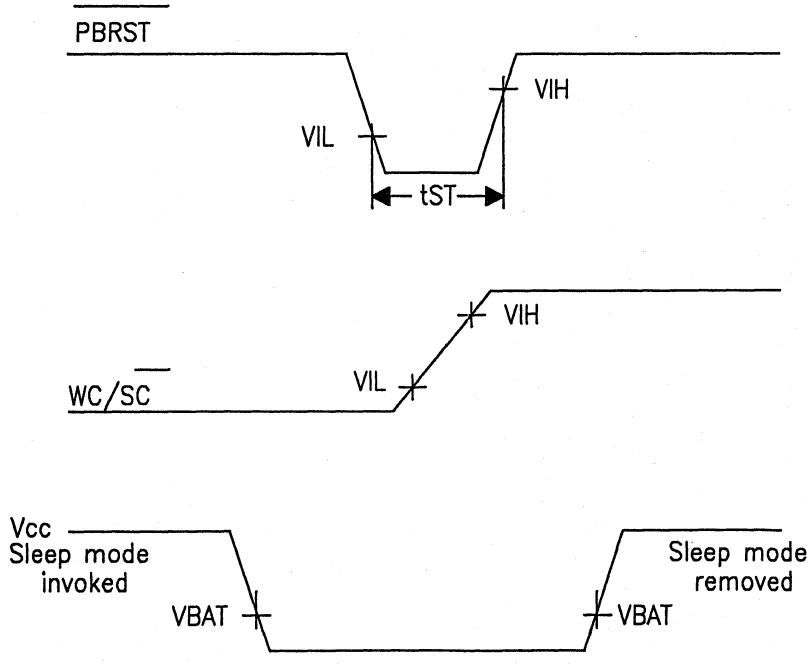
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 13



WAKE/SLEEP CONTROL Figure 14



OPTIONS FOR INVOKING WAKEUP Figure 15



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature on the Leads	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC} +0.3	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS (0°C To 70°C, V_{CC}=4.5 V To 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep mode	I_{CC}			20	uA	
Battery Current	I_{BAT}			.1	uA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC} -0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT}-0.7		V	1,6
CEO\ and PF Output	V_{OHL}		V_{BAT}-0.7		V	1,6
PBRST\ Pull Up Resist	R_{PBRST}	10K			Ohms	
Input Leakage Current	I_{LI}	-1.0		+1.0	uA	18
Output Leakage	I_{LO}	-1.0		+1.0	uA	18
Output Current @0.4V	I_{OL}			4.0	mA	12
Output Current @2.4V	I_{OH}	-1.0			mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	uA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C To 70°C, VCC = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, RST\	t_{RPD}	40	100	175	uS	
V_{TP} to NMI\	t_{IPD}	40	100	175	uS	
RESET Active Time	t_{RST}	25	100	150	mS	
NMI\ Pulse Width	t_{NMI}	200	300	500	uS	14
ST\ Pulse Width	t_{ST}	20			nS	
PBRST\ @ V_{IL}	t_{PB}	30			mS	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			uS	
Chip Enable Propagation Delay	t_{PD}			20	nS	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	uS	17
V_{CC} Valid to RST, RST\ (RC=1)	t_{FPU}		100	nS		
V_{CC} Valid to RST & RST\	t_{RPU}	25	100	150	mS	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			uS	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			uS	8
Chip Enable Output Recovery Time	t_{REC}	.1			uS	9
V_{CC} Slew 4.25 to 4.75	t_R	0			uS	
Chip Enable Pulse Width	t_{CE}			5	uS	10
Watchdog Time Delay	t_{TD}	100	400	600	mS	
ST\ to WC/SC\	t_{WC}	0.1		50	uS	
V_{BAT} Detect to PF, PF\	t_{PPF}			2	uS	7
ST\ to NMI\	t_{STN}			30	nS	11
NMI\ to RST & RST\	t_{NRT}			30	nS	
V_{BAT} Detect to RST & RST\	t_{ARST}			200	uS	15
V_{CC} Valid to RST, RST\	t_{BRST}	30	100	150	uS	16

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 uF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, CEO\, PF, ST\, PBRST\, RST, RST\, and NMI\ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236 can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5 volt operation.
4. I_{CCO2} is the maximum average load which the DS1236 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 *us*.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 *u*A load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before CEI\CEO memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 uA maximum.
13. All outputs except RST\ which is 25 uA minimum.
14. Pulse width of NMI\ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the NMI\ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. CEI\ low.
18. The WC/SC\ pin contains an internal latch which drives back on to the pin. This latch requires ± 200 uamps to switch states. The ST\ pin will sink ± 50 uamps in normal operation and ± 1 uamp in the sleep mode.

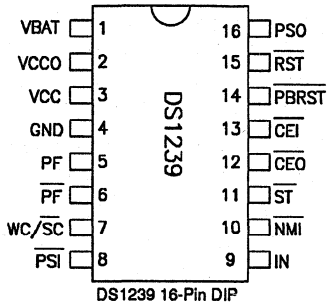
DALLAS SEMICONDUCTOR

DS1239
MicroManager Chip

FEATURES

- Provides necessary control for start up and shutdown of power supply from keyboard
- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors push button for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1239-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operate hand-held applications
- Standard 16-Pin DIP or space-saving 16-Pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN DESCRIPTION



DS1239 16-Pin DIP
(300 Mil.)

PIN NAMES(\ Denotes Condition Low)

V_{BAT}	+3 Volt Battery Input
V_{CCO}	Switched SRAM Supply Output
V_{CC}	+5 Volt Power Supply Input
GND	Ground
PF	Power Fail (Active High)
PF\	Power Fail (Active Low)
WC/SC\	Wake-Up Control (Sleep)
PSI\	Power Supply Control Input
IN	Early Warning Input
NMI\	Non-Maskable Interrupt
ST\	Strobe Input
CEO\	Chip Enable Output
CEI \	Chip Enable Input
PBRST \	Push Button Reset Input
RST\	Reset Output (Active low)
PSO	Power Supply Control Outputs

DESCRIPTION

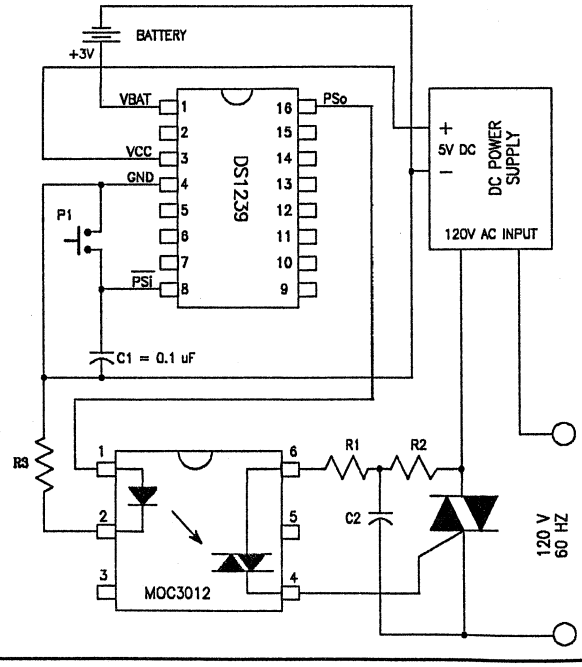
The DS1239 MicroManager provides all the necessary functions for power supply control and monitoring, reset control, and memory back-up in microprocessor-based systems. Using the DS1239, an AC power switch is no longer required for microprocessor-based systems. A keyboard control system for power supply start up and shutdown is provided through the use of the Power Supply Control Input and Output. In other respects, the DS1239 is functionally identical to a DS1236 in the NMOS mode. For a complete description of the other DS1239 fea-

tures, refer to the DS1236 data sheet. Pin-out of the DS1239 is identical to the DS1236 with two execptions. The RC and RST pins have been replaced with PSI\ and PSO respectively. Other pins and functions operate exactly as the DS1236 in NMOS mode. Operation of the power supply control function is decribed below.

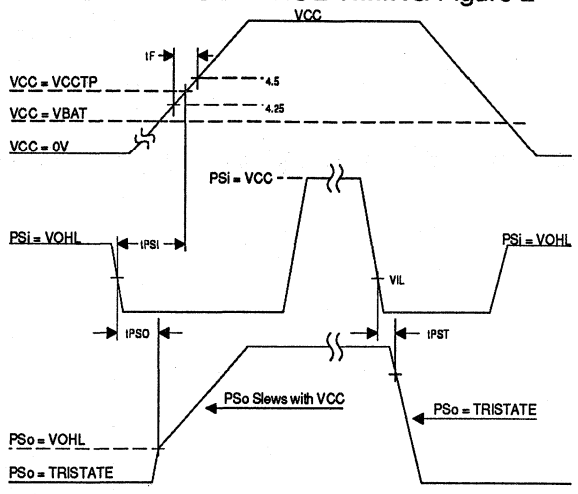
POWER SUPPLY CONTROL

The DS1239 facilitates the power-up and power down sequencing of a main power supply from a keyboard or push button. The Power Supply Control Input (PSI\) and Power Supply Control Output (PSO) are used for this purpose. Prior to establishing a voltage on V_{CC} (+5V), the PSI\ is internally held at a high level at all times with the V_{BAT} supply. When PSI\ is forced low via a key pad or other source, the PSO is connected to the V_{BAT} to provide a high level. As shown in Figure 1, this active high signal can be wired directly to an optically isolated SCR to initiate an AC to DC power-up sequence. This in turn will provide the supply voltage for V_{CC}. The timing is illustrated in Figure 2. Holding the PSI\ input low, the PSO output will supply a connection to the V_{BAT} pin until the V_{CC} reaches V_{BAT}, or a maximum of 200 mS. If the supply voltage on V_{CC} rises above the V_{BAT} level before the t_{PSI} time-out, the PSO pin will remain high and track the V_{CC} input. If V_{CC} does not rise above V_{BAT} before either t_{PSI} or PSI\ is allowed to return to a high level, the PSO output will return to tristate. Once the PSO output and V_{CC} are set at a high level, a subsequent falling edge on PSI\ will tristate PSO to initiate a shut down condition. The 10 microamp current supplied by the PSI\ pin allows the use of a 0.1 uF capacitor as a simple push button debounce circuit. The battery size for this application must be selected to provide the SCR on-current for the power supply response time, and is consequently application-specific.

POWER SUPPLY CONTROL Figure 1



POWER SUPPLY CONTROL TIMING Figure 2



NOTES:

1. Minimum turn-on response time for AC-to-DC power supply.
2. PSO pulse width for V_{CC} held below V_{BAT}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55° C to +125°C
Soldering Temperature on the Leads	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

These specifications reflect the power supply control feature of the DS1239. For complete electrical specifications, refer to the DS1236 data sheet.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
PSI\ Output Current	I_{PSI}		10		uA	
PSO Output Current	I_{PSO}	10			mA	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
PSI\ to Valid V_{CC}	t_{PSI}			200	ms	1
PSI\ to PSO Tri-state	t_{PST}			20	ns	
PSI\ to Valid PSO	t_{PSO}			100	ns	
PSO Pulse Width	t_{PSP}		200	500	ms	2

DALLAS SEMICONDUCTOR

DS1267
Dual Digital Potentiometer Chip

FEATURES

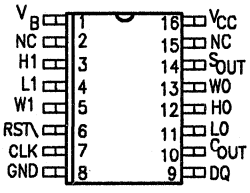
- Two digitally controlled 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power-up is 50%
- Resistive elements are temperature-compensated to +/- 20% end-to-end
- Operating temperature range of 0° C to 70° C
- 16-Pin SOIC for surface-mount applications
- Low-power CMOS design
- Resistance values:

	Resolution	-3dB Point
DS1267-10: 10K	39 ohms	250 KHz
DS1267-50: 50K	195 ohms	50 KHz
DS1267-100: 100K	390 ohms	40 KHz

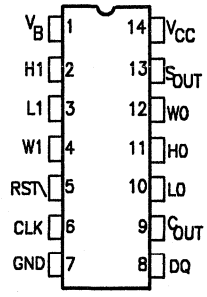
DESCRIPTION

The DS1267 is a dual solid-state potentiometer that is set to value by digitally selected resistive elements. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistance array is set by an 8-bit register that controls which tap point is connected to the wiper output. Each 8-bit register can be read or written by sending or receiving data bits over a three-wire serial port.

PIN DESCRIPTION



DS1267S 16-Pin SOIC
(300 mil)



DS1267 14-Pin DIP
(300 mil)

PIN NAMES (\ Denotes Condition Low)

L0, L1	Low end of resistor
H0, H1	High end of resistor
W1, W2	Wiper end of resistor
V_B	Substrate bias
S_{OUT}	Wiper for stacked configuration
RST \	Serial port reset input
DQ	Serial port data input/output
CLK	Serial port clock input
C_{OUT}	Cascade serial port output
V_{CC}	+5 volt input
GND	Ground
NC	No connection

In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1267 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same.

OPERATION

The DS1267 contains two potentiometers, each of which has its wiper set by a value contained in an 8-bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end. An 8-bit wiper register controls a 256-to-1 multiplexer that selects which tap point is connected to the wiper output.

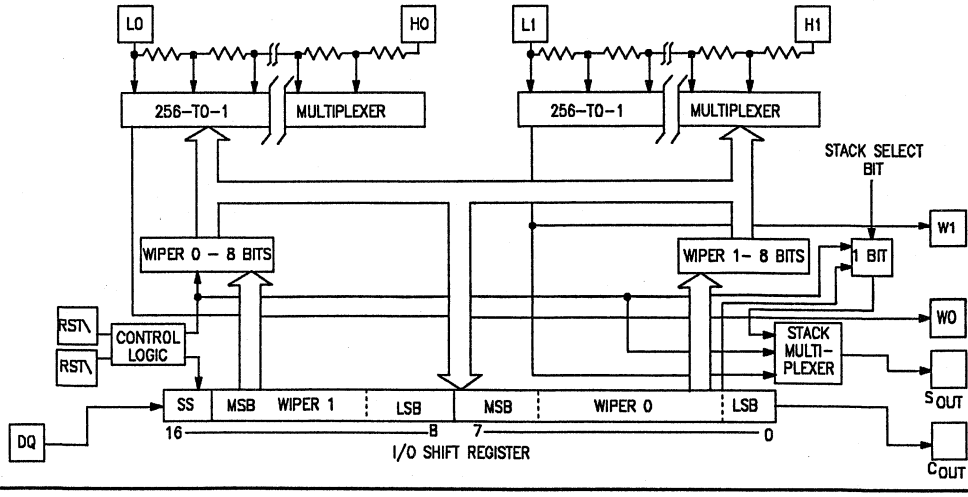
In addition, the potentiometers can be stacked by connecting them in series such that the high end of Potentiometer 0 is connected to the low end of Potentiometer 1. When stacking potentiometers, the stack select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (S_{OUT}). A zero written to the stack multiplexer will connect Wiper 0 to the S_{OUT} pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, Wiper 1 is selected and the upper 256 taps of the stacked potentiometer are present at the S_{OUT} pin.

Information is written and read from the Wiper 0 and Wiper 1 register and the stack select bit via the 17-bit I/O shift register. The I/O shift register is always serially loaded by a 3-wire serial port consisting of RST\, DQ, and clock. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17-bit shift register only when the RST\ input is at a high level. While at a high level, the RST\ function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until RST\ is taken to low a level, which terminates data transfer. While RST\ input is low, the DQ and CLK inputs are ignored.

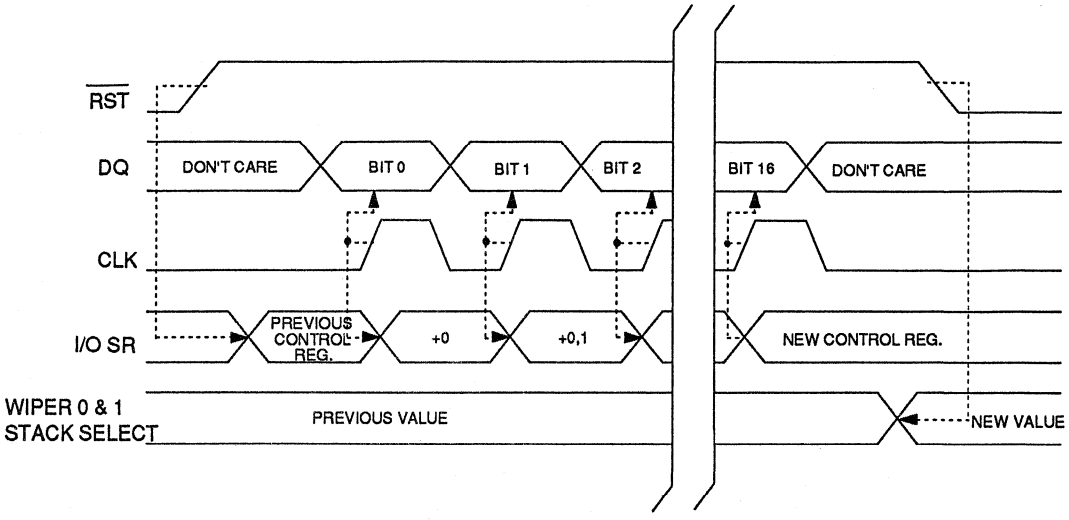
Valid data is entered into the I/O shift register while RST\ is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the stack select bit. The 17th bit to be entered, therefore, will be the least significant of the Wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, not sending 17 bits will produce indeterminate potentiometer settings.

As bits are entered into the shift register, the previous value is shifted out bit by bit on the

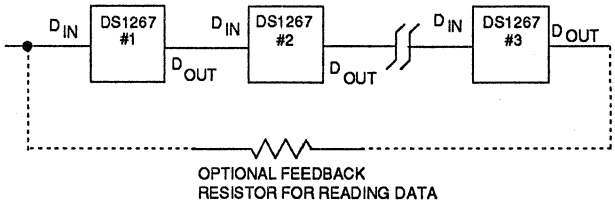
BLOCK DIAGRAM Figure 1



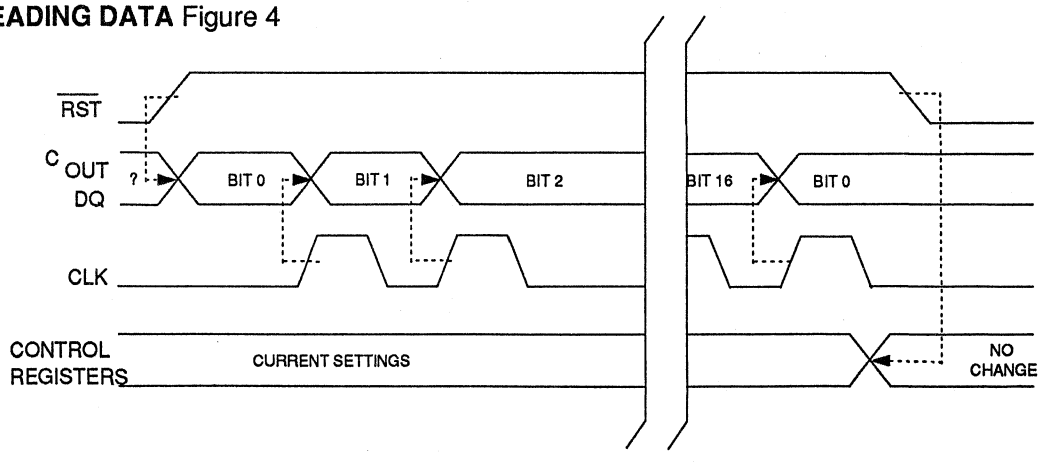
WRITING DATA Figure 2



CASCADING MULTIPLE DEVICES Figure 3



READING DATA Figure 4



cascade serial port pin (C_{OUT}). By connecting the C_{OUT} pin to the DQ pin of a second DS1267, multiple devices can be daisy chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1267s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the C_{OUT} pin of the last device connected in a daisy chain (one or more) must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between C_{OUT} and DQ when writing to the device (see Figure 3).

When reading data, the DQ line is left floating by the reading device. When RST\ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the resistor. This data bit can now be read by the reading device. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ. After 17 bits (17X devices for daisy chain), the data has shifted completely around and back to its original position. When RST\ is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the Wiper 0 and Wiper 1 register and the stack select bit is loaded from the I/O shift register.

When power is applied to the DS1267, the device always has the wiper settings at half position and the stack select bit is at zero.

DS1267 LINEARITY MEASUREMENTS

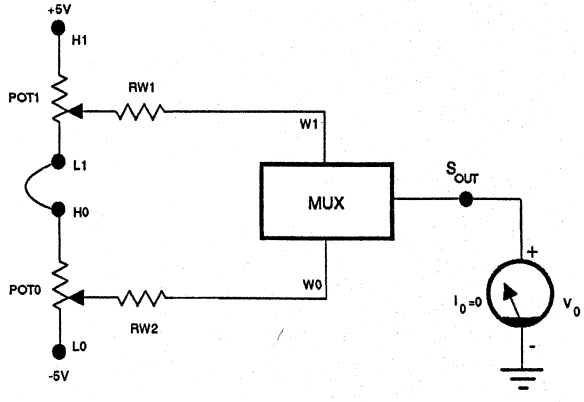
An important specification for the DS1267 is linearity, that is, for a given digital input, how close the analog output is to that which is expected.

The test circuit used to measure the linearity of the DS1267 is shown in Figure 5. The part is set up in a worst case situation for linearity, which is the stacked configuration. This gives 512 possible settings for the composite potentiometer. Note that to get an accurate output voltage it is necessary to assure that the output current is 0, in order to negate the effects of wiper impedance RW1 and RW0, which are typically 400 ohms. For any given setting N for the pot, the expected voltage output at S_{OUT} is:

$$Vo = -5 + (10 \times [N/512]) \text{ [in volts]}$$

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above, and is given in terms of an LSB, which is the change in expected output when the digital input is incre-

LINEARITY MEASUREMENT CONFIGURATION Figure 5



mented by 1. In this case the LSB is 10/512 or 0.01953 volts. The equation for the absolute linearity of the DS1267 is:

$$\frac{Vo(actual) - Vo(expected)}{LSB} = AL \text{ (in LSBs)}$$

The specification for absolute linearity of the DS1267 is +/- .5 LSB maximum.

Figure 6 is a plot of absolute linearity (AL) and relative linearity (rel) versus wiper setting for a typical DS1267 at 25°C.

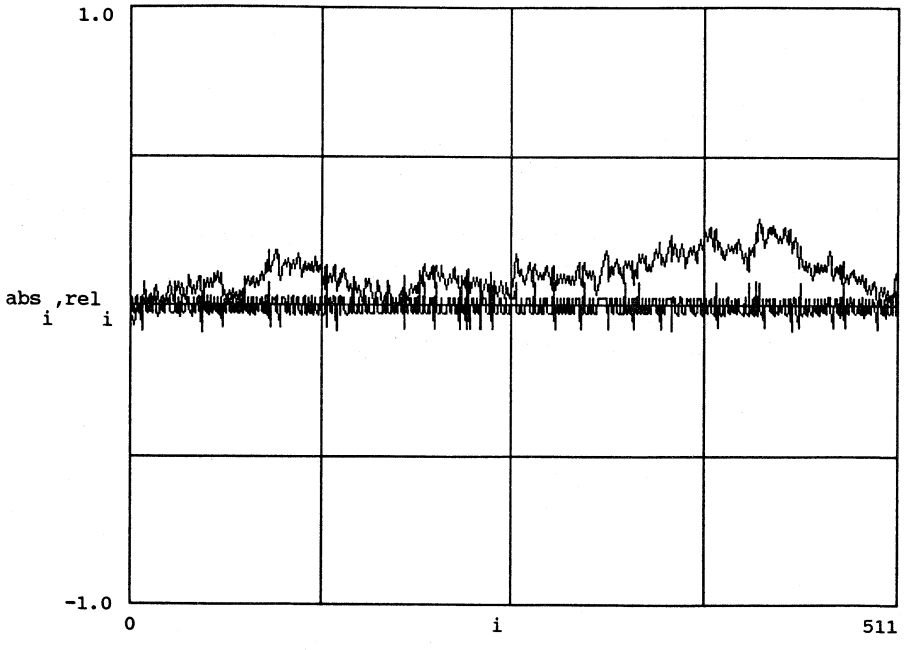
ANALOG CHARACTERISTICS

End-to-End Resistance Tolerance = +/- 20%
Typical Noise = < -120dB/ Hz Ref: 1V
Absolute Linearity = +/- 0.5 LSB maximum
Relative Linearity = +/- 0.2 LSB maximum
Temperature Coefficient = +/- 800 PPM/°C typical

NOTES:

1. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
2. Relative linearity is used to determine the change in voltage between successive tap positions.
3. Typical values are for t_A = 25°C and nominal supply voltage.

DS1267 ABSOLUTE AND RELATIVE LINEARITY Figure 6



Legend: Horizontal axis -- wiper setting.
Vertical axis -- error in LSB's.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground (V_B=GND)	-1.0V to +7.0V
Voltage on Resistor Pins when V_B= -5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+4.5	5.0	5.0	Volts	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	Volts	1
Input Logic 0	V_{IL}	-0.5		+0.8	Volts	1
Substrate Bias	V_B	GND		-5.5	Volts	1
Resistor Inputs	L,H,W	-5.0		+5.5	Volts	2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC}=5.0V ± 10%, V_B =-5.0V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		1	5	mA	
Input Leakage	I_{LI}	-1		+1	uA	3
Wiper Resistance	R_W		400	1000	Ohms	
Wiper Current	I_W		1		mA	
Output Leakage	I_{LO}	-1		+1	uA	
Logic 1 Output @ 2.4 Volts	I_{OH}	-1.0			mA	4
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	4

CAPACITANCE

(t_A = 25°C)

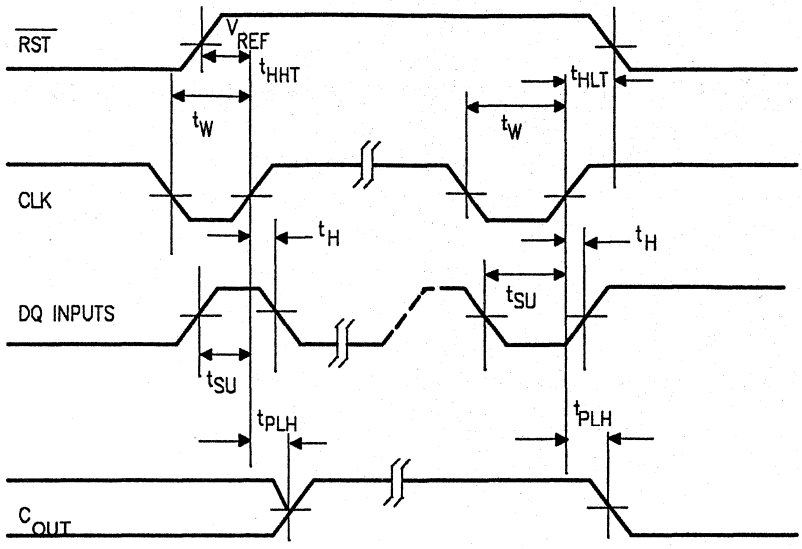
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}			10	MHz	
Width of CLK Pulse	t_W	50			ns	
Data Setup Time	t_{SU}	30			ns	
Data Hold Time	t_H	10			ns	
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	
Propagation Delay Time High to Low Level t_{PLH}		50			ns	
RST\ High to Clock Input High	t_{HHT}	50			ns	
RST\ Low from Clock Input High	t_{HLT}	50			ns	

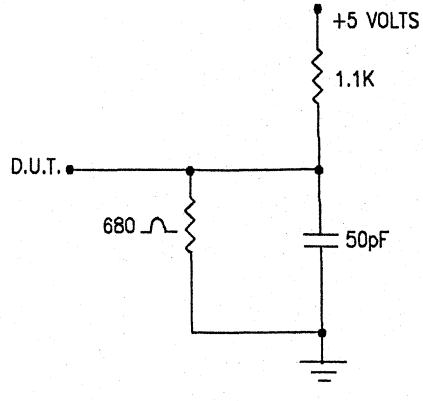
TIMING DIAGRAM Figure 7



NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction.
3. RST\ and CLK inputs have internal pull down resistors of 20K ohm typical.
4. Measured with a load as shown in Figure 8.
5. V_{REF} = 1.5 Volts.

LOAD SCHEMATIC Figure 8

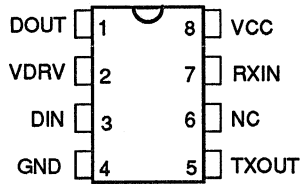


DALLAS SEMICONDUCTOR

DS1275
Line-Powered RS-232 Transceiver Chip

FEATURES
- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals power from receive signal line to save power
- Ultra-low static current, even when connected to RS-232-C port
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232-C signals
- Available in 8-pin, 150-mil wide SOIC package (DS1275S)
- Low-power CMOS

PIN DESCRIPTION



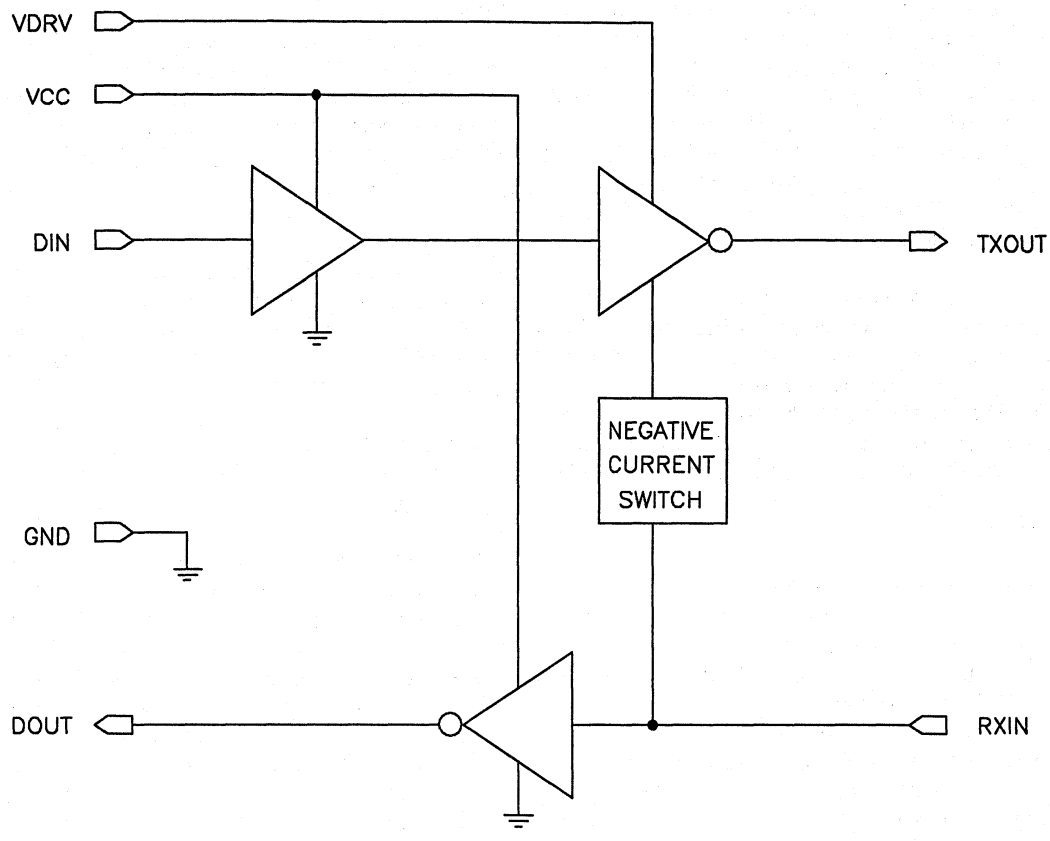
DS1275 8-Pin DIP
(300 Mil.)

PIN NAMES

DOUT	- Digital data out
VDRV	- Transmit driver +V
DIN	- Digital data in
GND	- System ground (0V)
TXOUT	- Transmit RS-232 out
NC	- No connection
RXIN	- Receive RS-232 in
V_{CC}	- System logic supply (+5V)

DESCRIPTION
The DS1275 Line-Powered RS-232 Transceiver Chip is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statically, using the receive signal for negative power greatly reduces the DS1275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors, and portable medical instruments. During an actual communication session, the DS1275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

DS1275 BLOCK DIAGRAM Figure 1



OPERATION

Designed for the unique requirements of battery-backed systems, the DS1275 provides a low-power half-duplex interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses his system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended, power will statically flow into that port, draining the battery capacity. The DS1275 eliminates this static current drain by stealing current from the receive line (RXIN) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS1275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TXOUT) when data is sent. However, since asynchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

RECEIVER SECTION

The RXIN pin is the receive input for an RS-232 signal whose levels can range from ± 3 to ± 15 volts. A negative data signal is called a mark while a positive data signal is called a space. These signals are inverted and then level-shifted to normal +5 volt CMOS/TTL logic levels. The logic output associated with RXIN is DOUT which swings from $+V_{CC}$ to ground. Therefore, a mark on RXIN produces a logic 1 at DOUT; a space produces a logic 0.

The input threshold of RXIN is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause DOUT to switch states. A negative-going signal must now be lower than 1.3 volts (typically) to cause DOUT to switch again. An open on RXIN is interpreted as a mark, producing a logic 1 at DOUT.

TRANSMITTER SECTION

DIN is the CMOS/TTL-compatible input for digital data from the user system. A logic one at DIN produces a mark (negative data signal) at TXOUT while a logic 0 produces a space (positive data signal). As mentioned earlier, the transmitter section employs a unique driver design that uses the RXIN line for swinging to negative levels. The RXIN line must be in a marking or idle state to take advantage of this design; if RXIN is in a spacing state, TXOUT will only swing to ground. When TXOUT needs to transition to a positive level, it uses the VDRV power pin for this level. VDRV can be a voltage supply between 5 to 12 volts, and in many situations it can be tied directly to the +5 volt V_{CC} supply. *It is important to note that VDRV must be greater than or equal to V_{CC} at all times.*

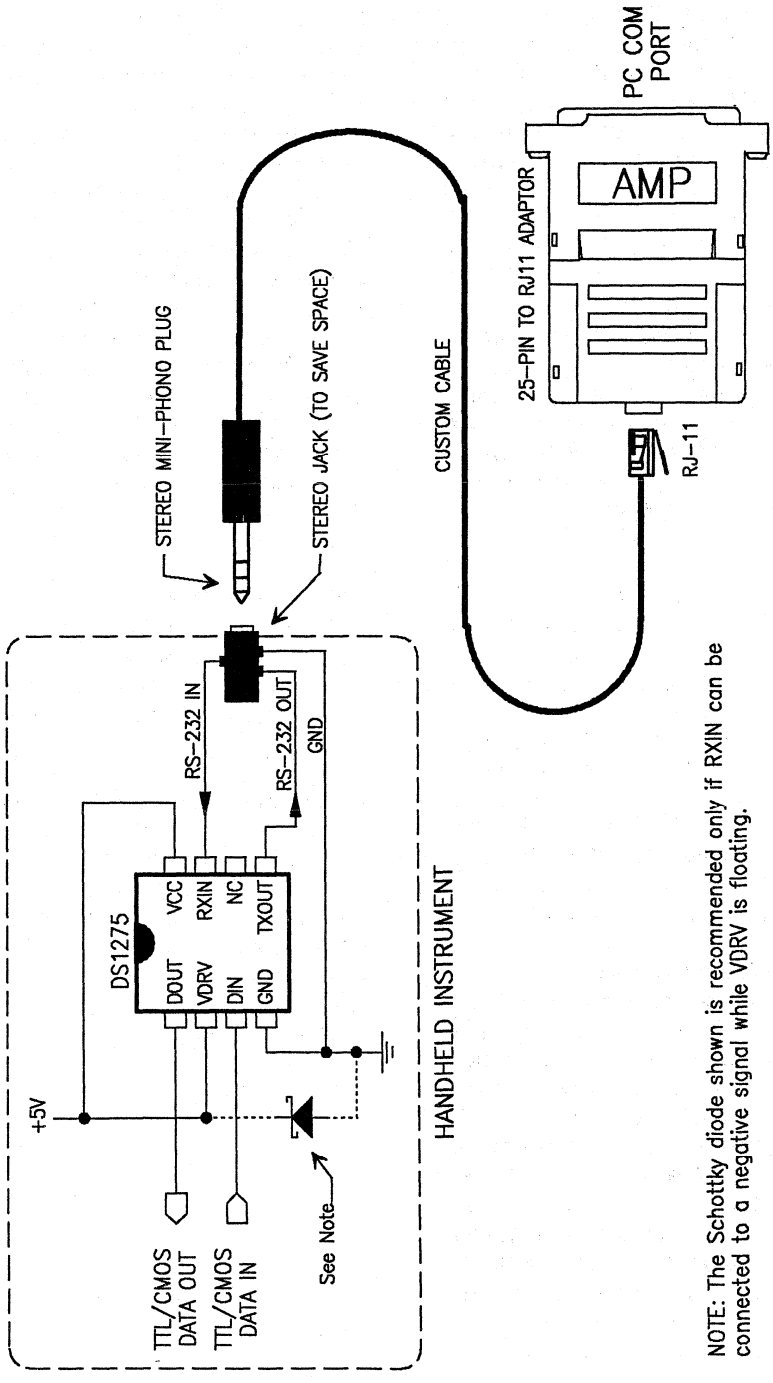
The voltage range on VDRV permits the use of a 9-volt battery in order to provide a higher voltage level when TXOUT is in a space state. When V_{CC} is shut off to the DS1275 and VDRV is still powered (as might happen in a battery-backed condition), only a small leakage current (about 50-100 nA) will be drawn. If TXOUT is loaded during such a condition, VDRV will draw current *only* if RXIN is not in a negative state. During normal operation (V_{CC}=5 volts), VDRV will draw less than 2 uA when TXOUT is marking. Of course, when TXOUT is spacing, VRDV will draw substantially more current -- about 3 mA depending upon its voltage and the impedance that TXOUT sees.

The TXOUT output is slew-rate limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TXOUT should be inadvertantly shorted to ground, internal current-limiting circuitry prevents damage, even if continuously shorted.

RS-232 COMPATIBILITY

The intent of the DS1275 is not so much to meet all the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS1275 will not meet the RS-232 requirement that the signal levels be at least ± 5 volts minimum when terminated by a 3 K ohm load and VDRV= +5 volts. Typically a voltage of 4 volts will be present at TXOUT when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

HANDHELD RS-232-C APPLICATION USING A STEREO MINI-JACK Figure 2



APPLICATIONS INFORMATION

The DS1275 is designed as a low-cost, RS-232-C interface expressly tailored for the unique requirements of battery-operated handheld products. As shown in the electrical specifications, the DS1275 draws exceptionally low operating and static current. During normal operation when data from the handheld system is sent from the TXOUT output, the DS1275 only draws significant VDRV current when TXOUT transitions positively (spacing). This current flows primarily into the RS-232 receiver's 3-7K ohm load at the other end of the attaching cable. When TXOUT is marking (a negative data signal), the VDRV current falls dramatically since the negative voltage is provided by the transmit signal from the other end of the cable. This represents a large reduction in overall operating current, since typical RS-232 interface chips use charge-pump circuits to establish both positive and negative levels at the transmit driver output.

To obtain the lowest power consumption from the DS1275, observe the following guidelines. First, to minimize VDRV current when connected to an RS-232 port, always maintain DIN at a logic 1 when data is not being transmitted (idle state). This will force TXOUT into the marking state, minimizing VDRV current. Second, VDRV current will drop to less than 100 nA when V_{CC} is grounded. Therefore, if VDRV is tied directly to the system battery, the logic +5 volts can be turned off to achieve the lowest possible power state.

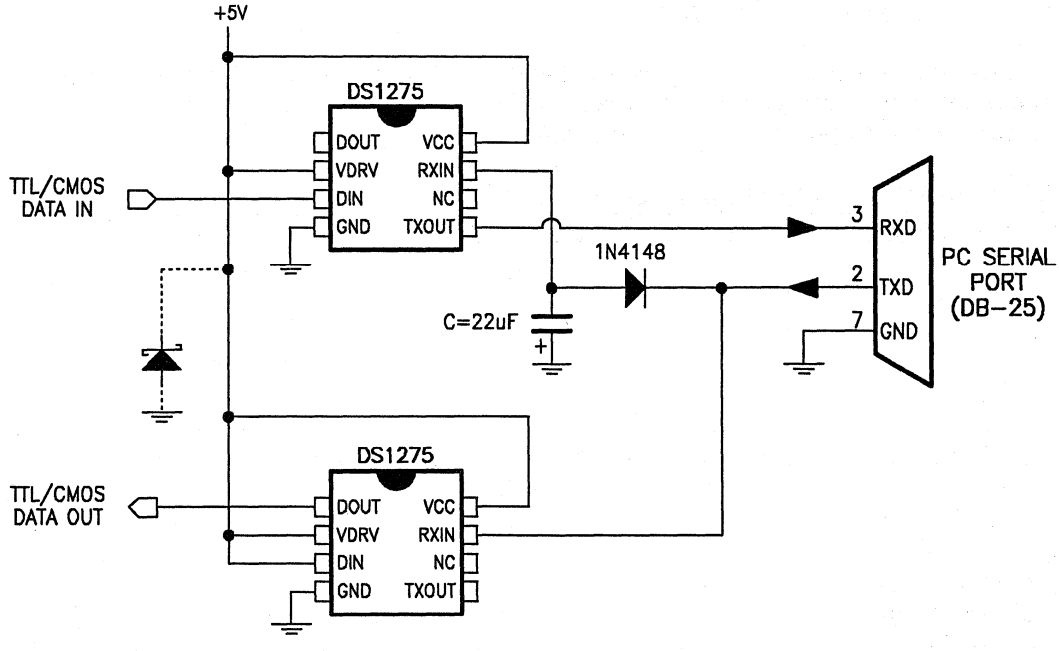
FULL-DUPLEX OPERATION

The DS1275 is intended primarily for half-duplex operation; that is, RXIN should remain idle in the marking state when transmitting data out TXOUT and visa versa. However, the part can be operated full-duplex with most RS-232-C serial ports since signals swinging between 0 and +5V will usually be correctly interpreted by an RS-232-C receiver device. The 5-volt swing occurs when TXOUT attempts to swing negative while RXIN is at a positive voltage, which turns on an internal weak pull-down to ground for the TXOUT driver's negative reference. So, transmit mark signals at TXOUT may have voltage jumps from some negative value (corresponding to RXIN marking) to approximately ground. One possible problem that may occur in this case is if the receiver at the other end requires a negative voltage for recognizing a mark. In this situation, the full- duplex circuit shown in Figure 3 can be used as an alternative. The 22uF capacitor forms a negative-charge reservoir; consequently, when the TXD line is spacing (positive), TXOUT still has a negative source available for a time period determined by the capacitor and the load resistance at the other end (3-7K ohms). This circuit was tested from 150-19,200 bps with error-free operation using a SN75154 Quad Line Receiver as the receiver for the TXOUT signal. Note that the SN75154 can have a marking input threshold below ground; hence there is the need for TXOUT to swing both positive and negative in full-duplex operation with this device.

LATCHUP PROTECTION

In most cases the DS1275 offers a high level of ESD and latchup protection. However, latchup can occur if VDRV is left floating (high impedance) while a negative signal is attached to RXIN. One possible scenario for this is as follows: if the handheld device is powered off with a FET switch, floating VDRV, and at the same time the user still has the the RS-232-C port connected. In order to eliminate this latchup potential, a Schottky diode from VDRV to ground is recommended as shown in Figure 2. The lower clamp voltage of the Schottky (300 mV) is required to prevent an internal silicon diode on the DS1275 from turning on, which precipitates the latchup condition.

FULL-DUPLEX CIRCUIT USING NEGATIVE-CHARGE STORAGE Figure 3



NOTE:
The capacitor stores negative charge whenever the TXD signal from the PC serial port is in a marking data state (a negative voltage that is typically -10 volts). The top DS1275's TXOUT uses this negative charge reservoir when it is in a marking state. The capacitor will discharge to 0 volts when the TXD line is spacing (and TXOUT is still marking) at a time constant determined by its value and the value of the load resistance reflected back to TXOUT. However, when TXD is marking, the capacitor will quickly charge back to -10 volts. Note that TXD remains in a marking state when idle, which improves the performance of this circuit.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	-0.3 to +7 volts
VDRV	-0.3 to +13 volts
RXIN	+/- 15 volts
DIN	-0.3 to V_{CC} + 0.3 volts
TXOUT	+/- 15 volts
DOUT	-0.3 to V_{CC} + 0.3 volts
Storage Temperature	-55° to + 125°C
Operating Temperature	0° - 70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Logic Supply	V_{CC}	4.5	5.0	5.5	volts	1
Transmit Driver Supply	V_{DRV}	4.5	5-12	13.0	volts	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	volts	2
Logic 0 Input	V_{IL}	-0.3		+ 0.8	volts	
RS-232 Input Range (RXIN)	V_{RS}	-15		+15	volts	
Dynamic Supply Current DIN = V_{CC} DIN = GND	 I_{DRV1} I_{CC1} I_{DRV1} I_{CC1}		 0.1 0.5 3.3 0.5	 1.0 2.0 5.0 2.0	 mA mA mA mA	3
Static Supply Current DIN = V_{CC} DIN = GND	 I_{DRV2} I_{CC2} I_{DRV2} I_{CC2}		 1.5 5.0 3.3 5.0	 15.0 20.0 5.0 20.0	 uA uA mA uA	4
Driver Leakage Current (V_{CC}= 0V)	I_{DRV3}		0.05	1.0	uA	5

DC ELECTRICAL CHARACTERISTICS

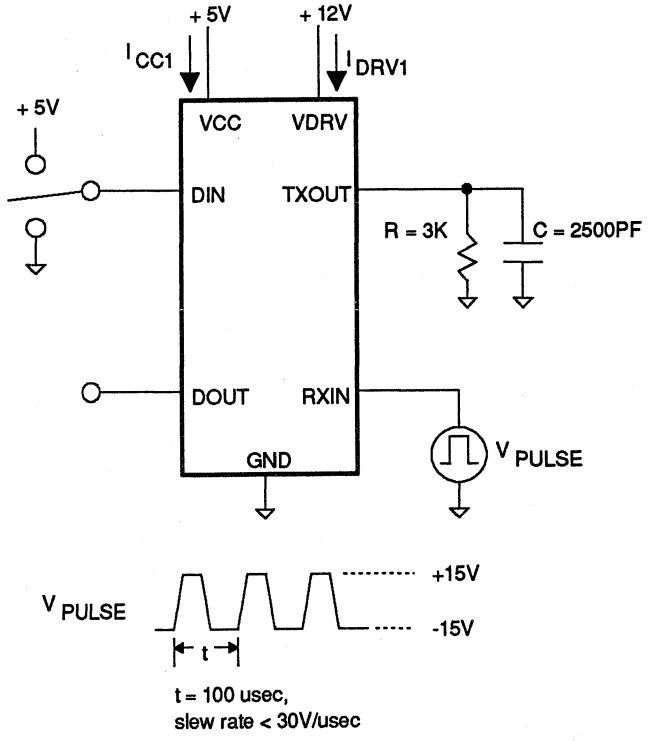
(0° - 70°C, V_{CC}=VDRV=5V ± 10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
TXOUT Level High	V_{OTXH}	3.5	4.0	4.5	volts	5
TXOUT Level Low	V_{OTXL}	-8.5	-9.0		volts	6
TXOUT Short-Circuit Current	I_{SC}		±60	±85	mA	
TXOUT Output Slew Rate	t_{SR}			30	V/us	
Propagation Delay	t_{PD}		5		us	7
RXIN Input Threshold Low	V_{TL}	0.8	1.2	1.6	volts	
RXIN Input Threshold High	V_{TH}	1.6	2.0	2.4	volts	
RXIN Threshold Hysteresis	V_{HYS}	0.5	0.8		volts	8
DOUT Output Current @ 2.4 V	I_{OH}	-1.0			mA	
DOUT Output Current @ 0.4 V	I_{OL}			3.2	mA	

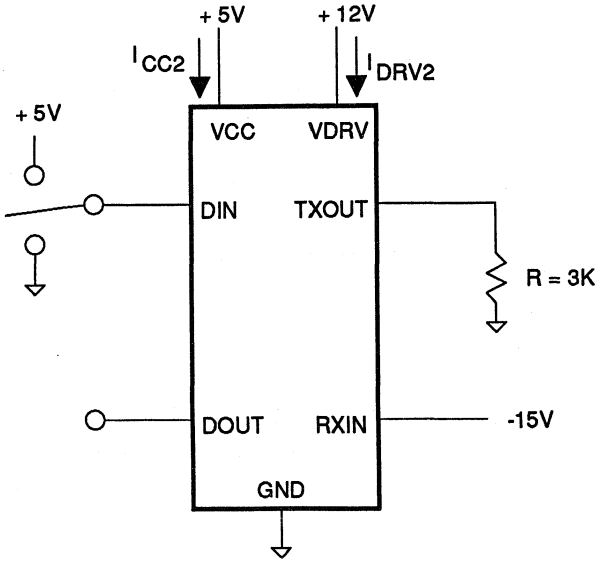
NOTES:

1. VDRV must be greater than or equal to V_{CC}.
2. V_{CC}=VDRV= 5V ± 10%.
3. See test circuit in Figure 4.
4. See test circuit in Figure 5.
5. See test circuit in Figure 6.
5. DIN = V_{IL} and TXOUT loaded by 3K ohms to ground.
6. DIN = V_{IH} , RXIN = -10 volts and TXOUT loaded by 3K ohms to ground.
7. DIN to TXOUT-- see Figure 7.
8. $V_{HYS} = V_{TH} - V_{TL}$.

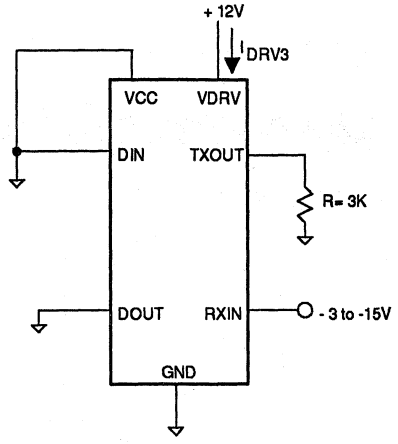
DYNAMIC OPERATING CURRENT TEST CIRCUIT Figure 4



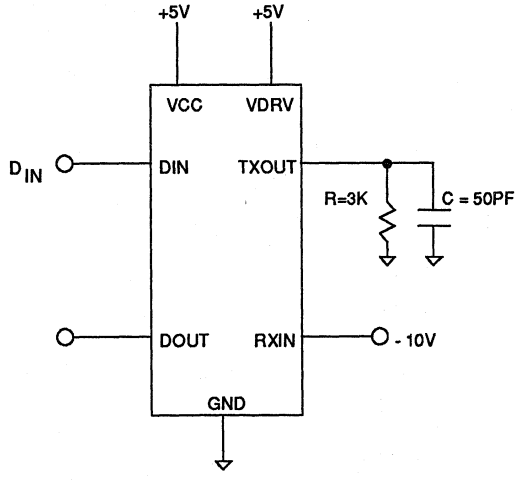
STATIC OPERATING CURRENT TEST CIRCUIT Figure 5

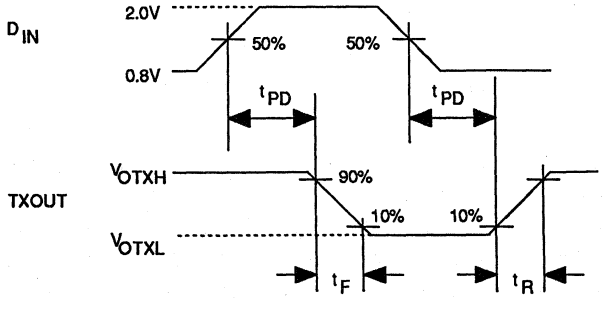


DRIVER LEAKAGE TEST CIRCUIT Figure 6



PROPAGATION DELAY TEST CIRCUIT Figure 7





$$t_{SR} = \frac{0.8\ (V_{OTXH} - V_{OTXL})}{t_F \text{ or } t_R}$$

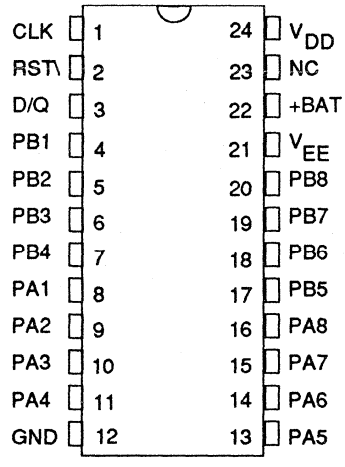
DALLAS SEMICONDUCTOR

DS1277
8-Channel Crosspoint Switch Chip

FEATURES

- Any port A input/output can be programmed for connection to any port B input/output
- Registers which define port connections are programmable via a 3-wire serial port
- All port input/output pins will accept both analog and digital signals
- Optional +5 volt and +/- 5 volt operation
- Switch registers can be made nonvolatile with external connection of a 3 volt lithium battery
- Applications include:
  - digital/analog switching and multiplexing
  - data scrambling for secure transmission

PIN DESCRIPTION



24-PIN DIP (600 Mil)

PIN NAMES (\ Denotes Condition Low)

+BAT	Battery Input
NC	No Connection
V_{EE}	Optional 5 Volt Supply Input
PA1-PA8	Port A Input/Output
GND	Ground
PB1-PB8	Port B Input/Output
D/Q	Serial Port Data Input/Output
CLK	Serial Port Clock
RST\	Serial Port Reset
V_{DD}	5 Volt Power Supply

DESCRIPTION

The DS1277 8-Channel Crosspoint Switch Chip is a programmable, low-power CMOS switching device which has the capacity to interconnect eight digital or analog signals in any combination. Interconnection is controlled by eight data registers of eight bits each which are read and written via a 3-wire serial port. The eight registers define the 64 possible combinations of the internal crosspoint switch. The DS1277 can be operated from a single +5 volt supply or optional +/- 5 volt operation can be selected to allow inputs and outputs to swing above and below ground.

OPERATION - GENERAL

With the -5 volt input grounded and +5 volts applied to pin 24, input/output pins of ports A and B will accept voltage levels between 0 and 5 volts. When V_{EE} is connected to -5 volts with +5 volts applied to pin 24, the input/output pins of ports A and B will accept voltage levels between -5 and +5 volts. Regardless of the voltage selections, applied voltages on port pins will be reproduced on pins which are interconnected by the internal crosspoint switch as defined by the data register settings.

The data registers are shown in Figure 1. As defined, each register specifies one port A I/O pin. Each of the eight bits of the register specifies connection or no connection to each of the port B I/O pins. A logic 1 causes a connection and a logic 0 is a no connection. When the DS1277 is powered up, all register bits are forced to a zero unless a battery voltage of greater than 2 volts is present on pin 1. With proper battery voltage, all registers are retained in the programmable state. If the nonvolatile feature is not used then pin 1 must be grounded.

OPERATION - SERIAL PORT

The eight data registers of the DS1277 are written and read via a 3-wire serial port consisting of RST\, CLK, and D/Q. To initiate data transfer with the DS1277, RST\ is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input (see Figure 2). The command register must match the exact bit pattern which defines either a read or a write. If a match does not exist communication will be ignored. If the command register is properly loaded then communication is allowed to continue and the next 64 cycles to the DS1277 will either update the data registers or read the data register content when the data registers are being updated. Switch settings are not affected until RST\ is driven low at the end of the 64-bit data transfer.

COMMAND WORD

Each data transfer begins with a three byte command word as shown in Figure 3. The first byte of the command word specifies whether the 64-bit data registers will be written or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted. The eight bit pattern for read is 01000110. The pattern for write is 10111001. The second and third bytes of the command word must match the exact pattern of 00000000, 11110000 or data transfer is aborted.

RESET AND CLOCK CONTROLS

All data transfers are initiated by driving the RST\ input high. RST\ must remain high for the entire 24-bit command word and the 64-bit data stream. The RST\ input terminates communication and updates the switch settings only after all 64 bits of the data registers have been written when reset is driven low. Reading of registers can be terminated at any time by driving RST\ low.

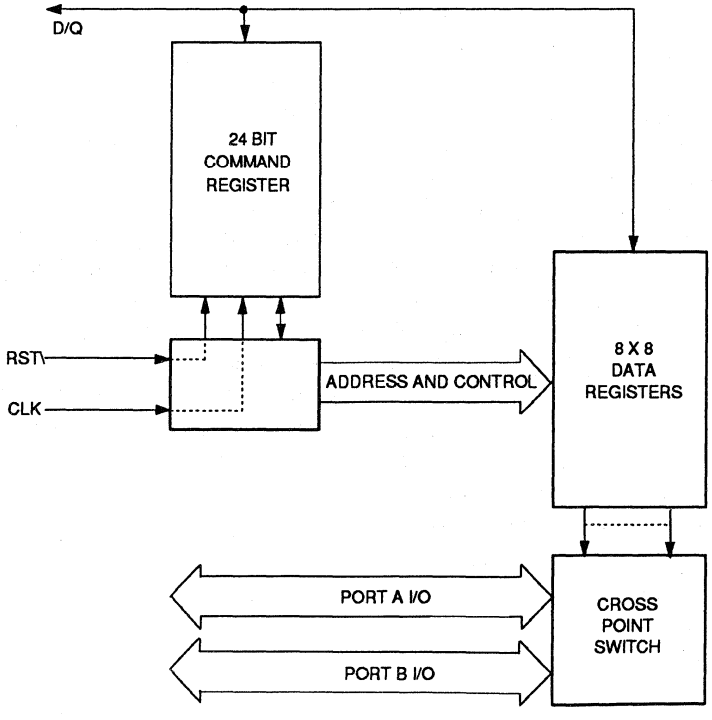
A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate and D/Q goes to a high impedance state if the RST\ input is low. Transfer of register data to switches occurs as RST\ is driven low only if 64 bits of data have been written. RST\ has no other effect on the register content. Data transfer is illustrated in Figures 4, 5, and 6.

DATA REGISTERS Figure 1

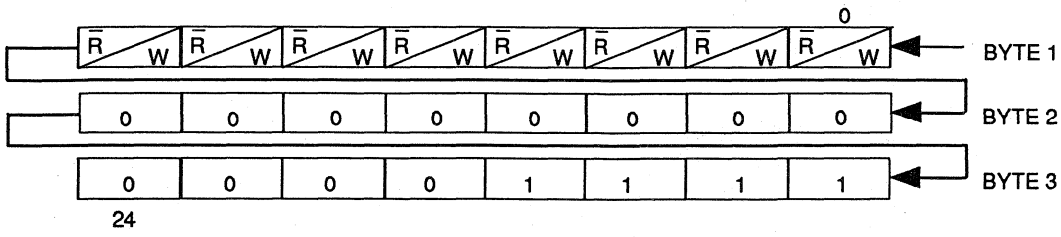
	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1
PB1	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
PB2	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
PB3	BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
PB4	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24
PB5	BIT39	BIT38	BIT37	BIT36	BIT35	BIT34	BIT33	BIT32
PB6	BIT47	BIT46	BIT45	BIT44	BIT43	BIT42	BIT41	BIT40
PB7	BIT55	BIT54	BIT53	BIT52	BIT51	BIT50	BIT49	BIT48
PB8	BIT63	BIT62	BIT61	BIT60	BIT59	BIT58	BIT57	BIT56

NOTE: Logic 1 closes switch
Logic 0 opens switch

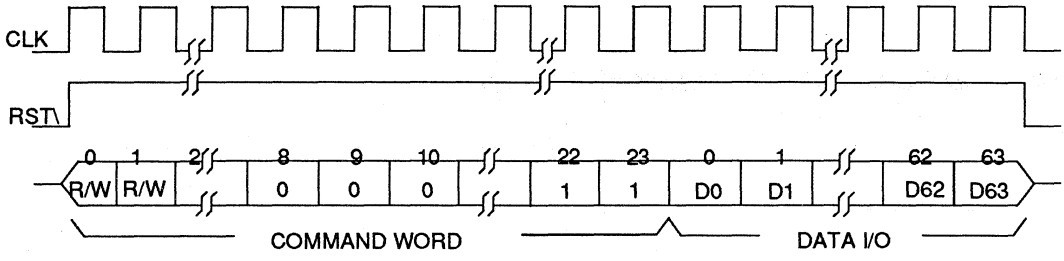
BLOCK DIAGRAM Figure 2



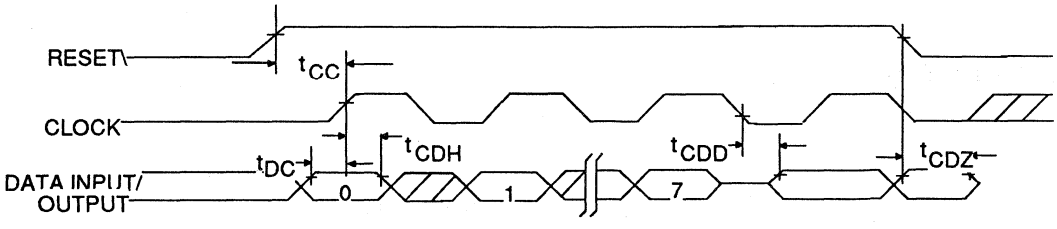
COMMAND REGISTER Figure 3



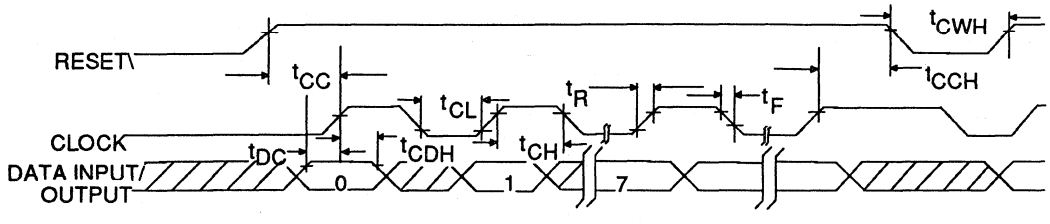
COMMAND WORD/DATA TRANSFER Figure 4



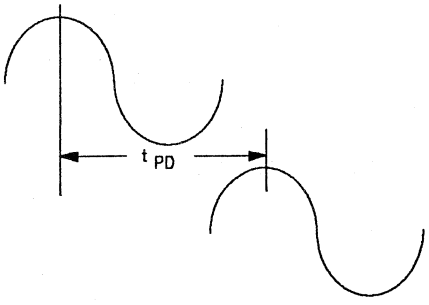
READ DATA TRANSFER Figure 5



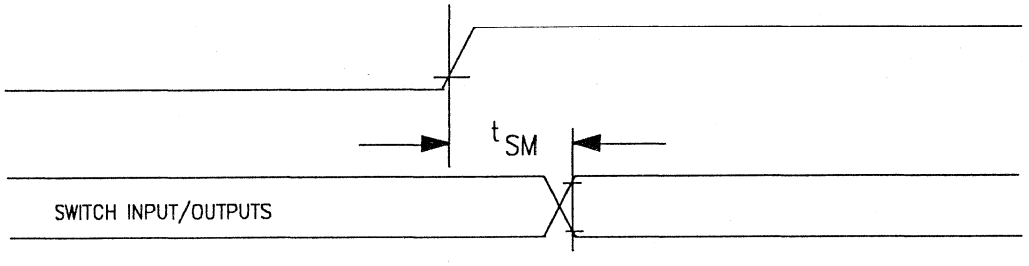
WRITE DATA TRANSFER Figure 6



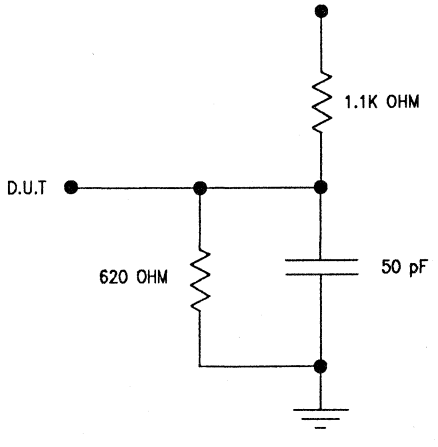
TIMING DIAGRAM: SWITCH PROPAGATION DELAY Figure 7



TIMING DIAGRAM: SWITCH CONNECT t_{pd} Figure 8



OUTPUT LOAD Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-5.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	V_{DD}	4.5	5.0	5.5	Volts	1
- Supply Voltage	V_{EE}	0	-5.0	-5.5	Volts	1
Serial Port Logic 0	V_{IL}	-0.3		0.8	Volts	1
Serial Port Logic 1	V_{IH}	2.0		V_{DD}+0.3	Volts	1
A @ B Port Input	V_{IN}	0		V_{DD}	Volts	-Supply = GND
A @ B Port Input	V_{IN}	$-V_{EE}$		V_{DD}	Volts	-Supply = -5.0V

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{EE}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
D/Q Output Current @ 2.4V	I_{OH}	-1			mA	2
D/Q Output Current @ 0.4V	I_{OL}			+4	mA	2
Input Leakage	I_{IL}	-1		+1	uA	3
Output Leakage	I_{OH}	-1		+1	uA	3
X Switch On Impedance	X_{ON}		250	500	Ohms	4
+Supply Current Active	I_{DD1}			10	mA	
+ Supply Current Quiescent	I_{DD2}			1	mA	5
-Supply Current	I_{EE}			1	mA	
X Switch Off Impedance	X_{OFF}	1 Meg			Ohms	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	COND.	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5		
Output Capacitance	C_{OUT}			7		
Feedthrough Capacitance	C_{IN}-C_{OUT}			10		

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	6
CLK to Data Hold	t_{CDH}	50			ns	6
CLK to Data Delay	t_{CDD}			200	ns	2,6,7
CLK Low Time	t_{CL}	250			ns	6
CLK High Time	t_{CH}	250			ns	6
CLK Frequency	s_{CLK}	DC		2.0	MHz	6
CLK Rise and Fall	t_{RTF}			500	ns	6
RST\ to CLK Setup	t_{CC}	1			uS	6
CLK to RST\ Hold	t_{CCW}	50			ns	6
RST to I/O High Z	t_{CDZ}			75	ns	6
Input to Output Delay	t_{PO}			50	ns	
RST\ Low to Switch Transition	t_{SM}			50	ns	

NOTES

1. All voltages are referenced to ground (V_{SS}).
2. Measured with a load as shown in Figure 5.
3. V_{DD} = +5 volts. V_{EE} = -5 volts. V_{SS} = GND: all other pins open.
4. X switch impedance is the terminal resistance of connected switch inputs to outputs.
5. V_{DD} = +5 volts. V_{EE} = -5 volts. V_{SS} = Ground, RST\ = V_{IL}. All other pins open.
6. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10 ns maximum rise and fall times.
7. Measured at V_{OH} = 2.4 volts and V_{OL} = 0.4 volts.

DALLAS SEMICONDUCTOR

DS129X
Eliminator

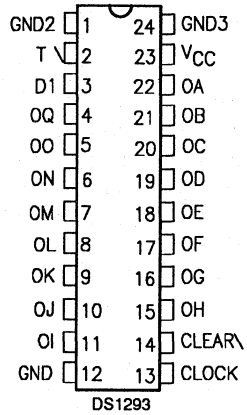
FEATURES

- Replaces 8 or 16 hard-to-get-at manual switches
- Options printed circuit board via software
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Serial Interface Chip
- Low-power CMOS
- Switch setting changes occur simultaneously
- DS1290 and DS1292 maintain settings in the absence of power; DS1291 and DS1293 are volatile
- Over 10 years of data retention

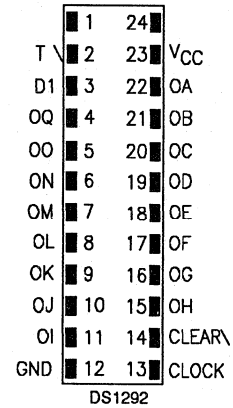
DESCRIPTION

The DS129x Eliminators replaces manual switches used to option printed circuit boards. Up to sixteen output pins can be set to a logic level or interrogated by three signals: clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 and DS1292 will maintain high or low level outputs, duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

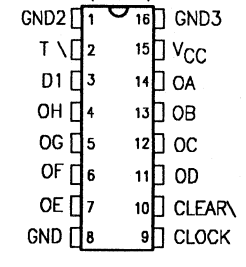
PIN DESCRIPTION



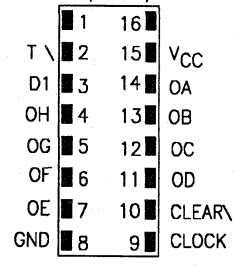
DS1293
24-Pin DIP
(300 Mil)



DS1292
24-Pin Encapsulated Package
(390 Mil)



DS1291
16-Pin DIP
(300 Mil)



DS1290
16-Pin Encapsulated Package
(400 Mil)

PIN NAMES

T\	Transfer
DI	Data Input
$O_A O_Q$	Switch Outputs
CLOCK	Clock Input
CLEAR\	All Outputs Set Low
V_{CC}	+5 Volts
GND	Ground
GND2	Missing on DS1292 Must Be Grounded on DS1293
GND3	Missing on DS1292 Must be Grounded on DS1293

OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control (see the block diagram in Figure 1). The DS1290/DS1291 Eliminator is a 8-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control. Data can be entered into the registers only when the transfer input (T\) is at a high level. While at a high level, the transfer function allows serial entry of data via the data input pin (DI). The outputs 0_Q through 0_B remain in the state that was set prior to T\ being driven to a high level. Output 0_A will change state as new data is entered. This output provides a method of feeding back actual output settings prior to setting the T\ input low (Figure 2). When the T\ input is driven low, new data that has been input into the 16-bit shift register is now locked at outputs 0_Q through 0_A. When the T\ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while T\ is high on the low-to-high transition of the CLOCK input. Data can be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The CLEAR\ input will always set all outputs to low level regardless of the level of the CLOCK or T\ input.

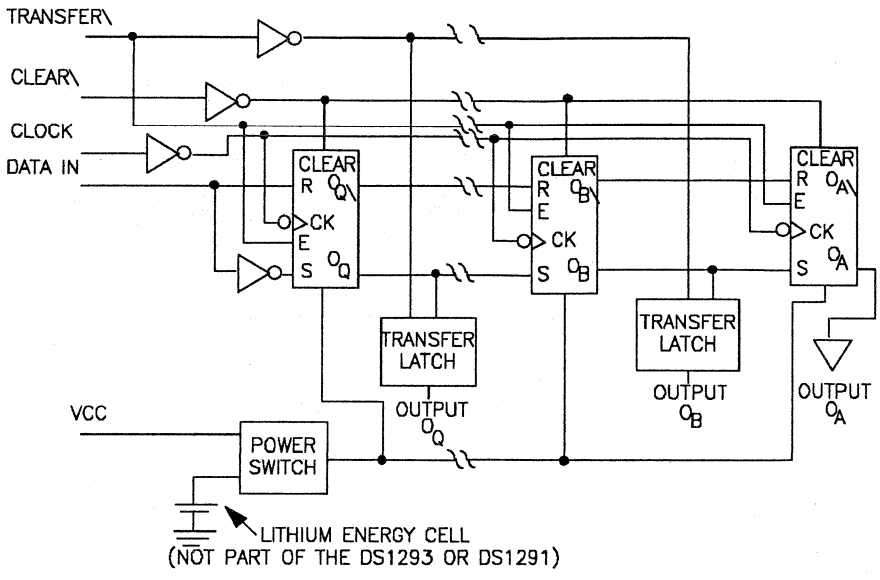
DATA RETENTION MODE

The DS129x Eliminators provides full functional capability when V_{CC} is greater than 4.5 volts and will ignore all inputs when V_{CC} reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As V_{CC} falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power-up when V_{CC} rises above approximately 3 volts, the power switching circuit connects external V_{CC} to the shift register and disconnects the lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for 10 ms minimum. During power transients the 16 outputs will track the level of V_{CC} if set to Logic 1 and will remain at ground level if set to Logic 0.

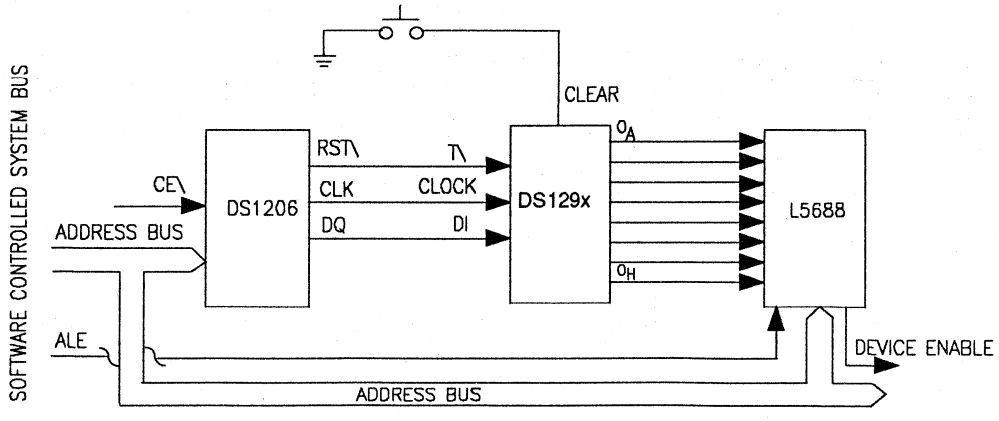
TYPICAL APPLICATION - ELIMINATOR

The DS129x and DS1206 combine to make a programmable nonvolatile DIP switch that can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, they need only be set once; they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Serial Interface Chip. The DS1206 samples four address lines and the chip enable signal looking for a special pattern for 24 consecutive cycles (see the DS1206 data sheet). When a proper match is found, the address lines and one data line become control and data signals that are used to program and verify the settings of the DS129x. All of the signaling sent to the DS1206 and subsequently to the DS1292 is generated by software-controlled read cycles that have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

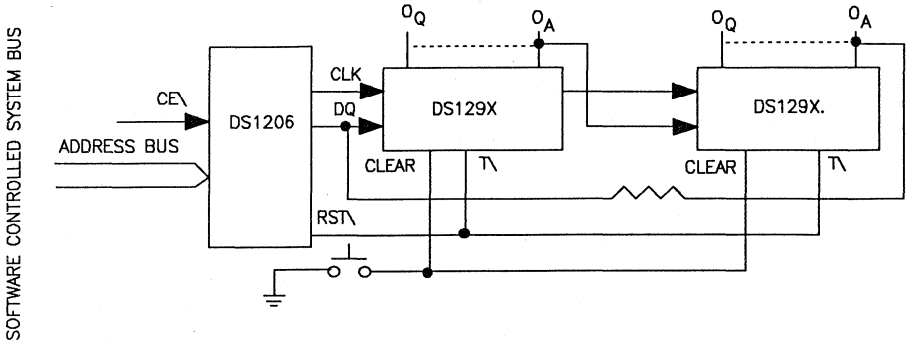
BLOCK DIAGRAM - DS129x Figure 1



PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



MODULAR EXPANSION OF THE ELIMINATOR Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-3.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		3	5	mA	
Input Leakage	I_{IL}	-1.0		+1.0	uA	4
Output Leakage	I_{LO}	-1.0		+1.0	uA	
Logic 1 Output @ 2.4V	I_{OH}	-1.0			mA	2
Logic 0 Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

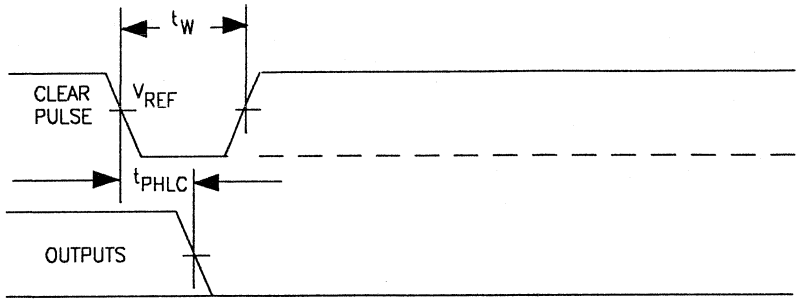
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

AC ELECTRICAL CHARACTERISTICS

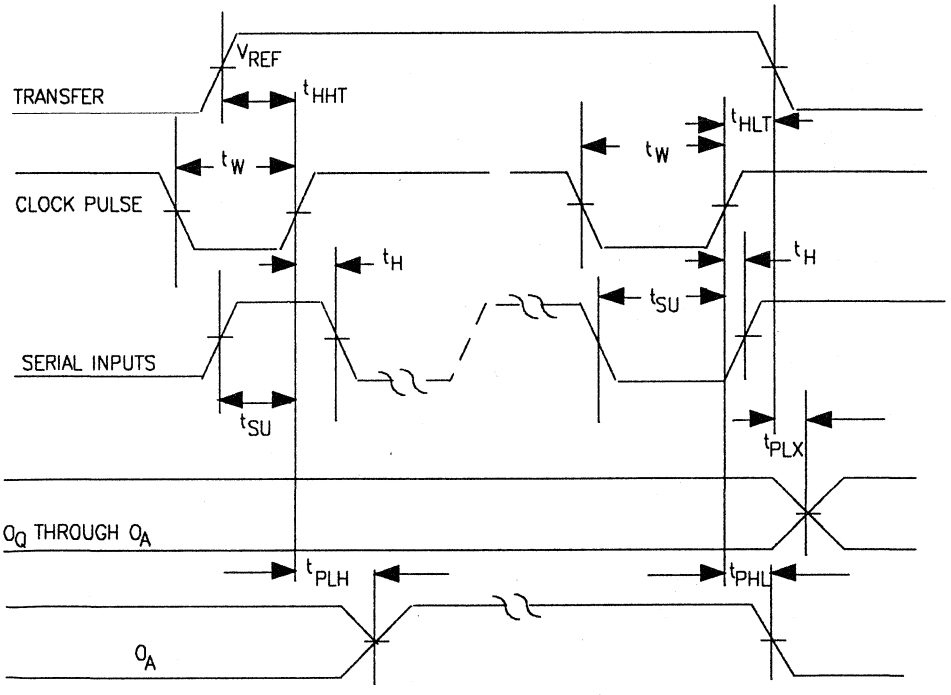
(0°C to 70°C; V_{CC} = 5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLOCK}			10	MHz	
Width of Clock Pulse	tw_{CLOCK}	50			ns	3
Width of Clear Pulse	tw_{CLEAR}	50			ns	3
Data Setup Time	t_{SU}	30			ns	3
Data Hold Time	t_H	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	t_{PHLC}			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			50	ns	3
Recovering on Power-Up	t_{REC}	10			ms	
Propagation Delay Time High to Low Level Transfer to O Out	t_{PLX}			50	ns	3
Transfer High to Clock Input High	t_{HHT}	50			ns	3
Transfer Low from Clock Input High	t_{HLT}	50			ns	3

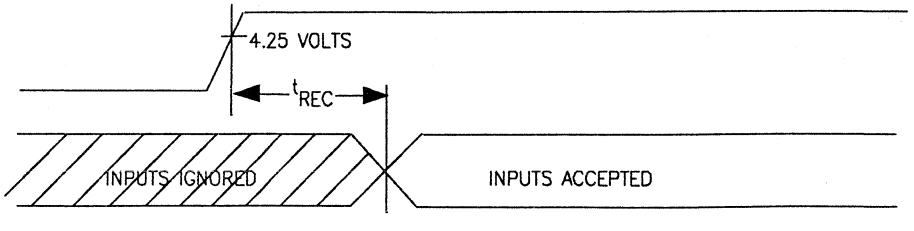
TIMING DIAGRAM - CLEAR CONTROL (3)



TIMING DIAGRAM - TRANSFER DATA (3)



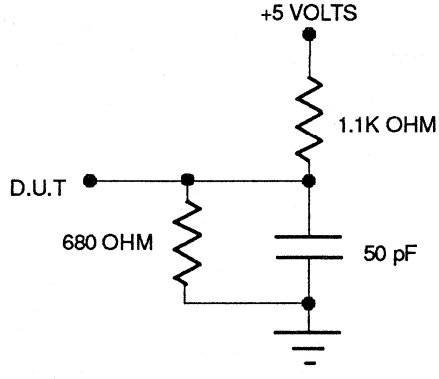
TIMING DIAGRAM - POWER-UP (3)



NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. V_{REF} = 1.5 volts.
4. Clock and transfer inputs have internal pull-down resistors of 20K ohms typical. Clear has an internal pull-up resistor of 20K ohms typical.

OUTPUT LOAD Figure 4



DALLAS SEMICONDUCTOR

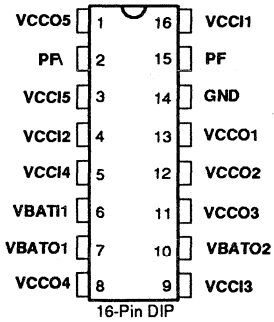
DS1336
Afterburner Chip

FEATURES

- Provides power switching up to 1.5 amps at 5 volts, with less than a 200 mV drop
- Five separate power switches
- Selectable battery switches for use with battery-backed systems
- Battery backup current of 10 mA
- Diode isolated battery path
- Low-voltage drop battery path
- Directly controlled by :

DS1211	DS1212	DS1231
DS1232	DS1234	DS1236
DS1237	DS1239	DS1259
DS1260	DS5001	DS5340

PIN DESCRIPTION



16-Pin DIP
(300 Mil.)

PIN NAMES

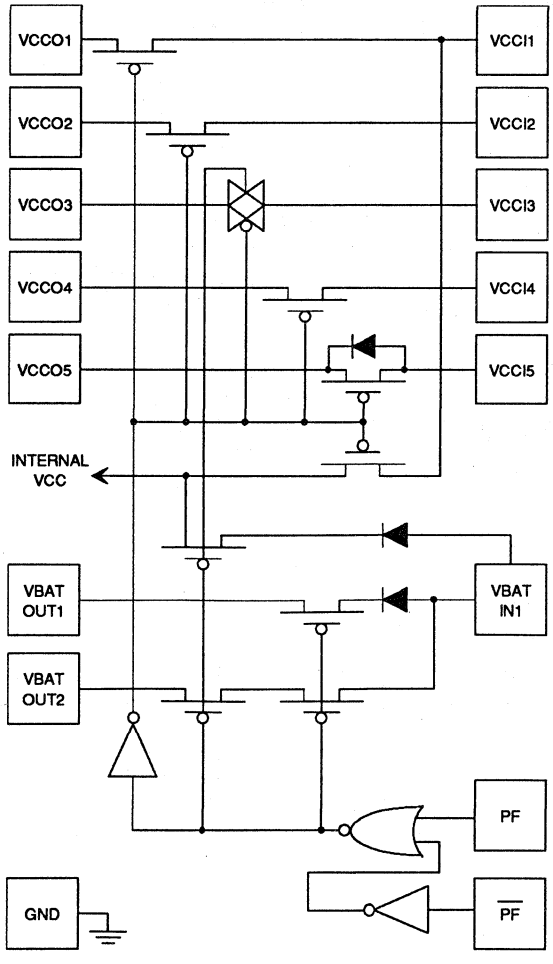
V_{CCO1}	V_{CC} switched output 1
V_{CCI3}	V_{CC} input 3
V_{CCO3}	V_{CC} switched output 3
V_{CCI5}	V_{CC} input 5
V_{CCO5}	V_{CC} switched output 5 w/ parallel diode
V_{BATO1}	Diode protected battery output
V_{BATO2}	Low voltage drop battery output
GND	Ground
PF\	Input command to switch between V_{CC} and V_{BAT}, active low
PF	Input command to switch between V_{CC} and V_{BAT}, active high
V_{BATI}	Battery input
V_{CCO4}	V_{CC} switched output 4
V_{CCI4}	V_{CC} input 4
V_{CCO2}	V_{CC} switched output 2
V_{CCI2}	V_{CC} input 2
V_{CCI1}	V_{CC} input 1 & internal supply

DESCRIPTION

The DS1336 Afterburner Chip provides power switching capability for nonvolatile operation and power supply isolation of large loads such as SRAM networks. When used with one of the power supply monitors listed above, the DS1336 allows a load to be switched from main power supply V_{CC} to battery backup when the supply voltage drops out of tolerance. This is accomplished by connecting one or more V_{CCO}s to a V_{BATO}. Depending on load requirements, the diode isolated battery path or low voltage drop battery path can be used.

All of the devices listed above provide switch-over outputs (PF\, RST\, V3.0, etc.) which indicate the loss of in-tolerance V_{CC}. These outputs occur in two classes, but all connect directly to the PF\ input. In cases where the PF signal is unavailable, the PF pin should be connected to a V_{CCO}. The first class provides a power fail notification when V_{CC} reaches 3.0 V, or V_{BAT}. The second provides notification at a voltage greater than V_{BAT}. Each device switch point is shown in Table 1. When using devices which switch over at a voltage greater than V_{BAT}, a diode should be placed in parallel with the DS1336 to provide a gradual transition to V_{BAT}. For convenience, V_{CCO5} provides such a diode path internally. The block diagram in Figure 1 illustrates the operation of the DS1336. V_{CCO} outputs can be connected in parallel to provide increased current capability. If V_{CCO5} is used, the internal diode will accommodate all channels. However, if true tri-state capability is desired, then V_{CCO5} should be omitted. Both V_{BAT} outputs are available when the PF\ is low and the PF is high, but would never be connected together. The low voltage drop battery output accommodates voltages sensitive devices such as timekeepers, where as the diode isolated path provides increased protection.

DS1336 BLOCK DIAGRAM Figure 1



APPLICATION OF THE DS1336 Figure 2

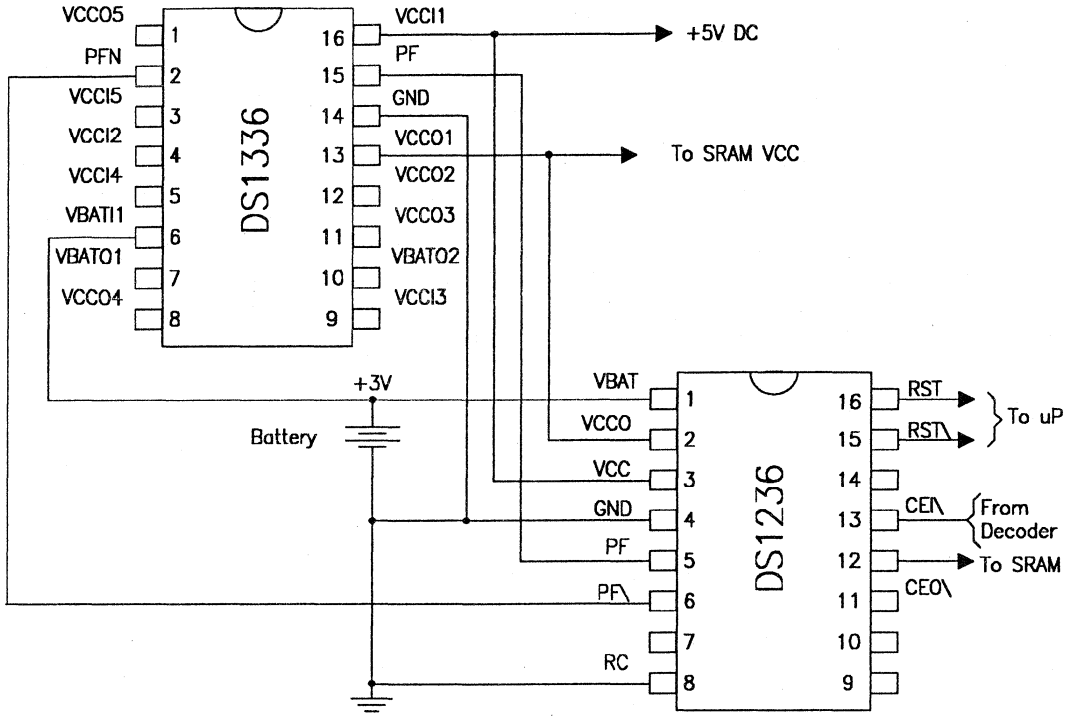


Table 1

Device	Switch > VBAT	Switch at 3.0 V
DS1211	X	
DS1212	X	
DS1231	X	
DS1232	X	
DS1234	X	
DS1236	X	X
DS1237	X	
DS1239	X	X
DS1259	X	
DS1260	X	
DS5001	X	X
DS5340	X	X

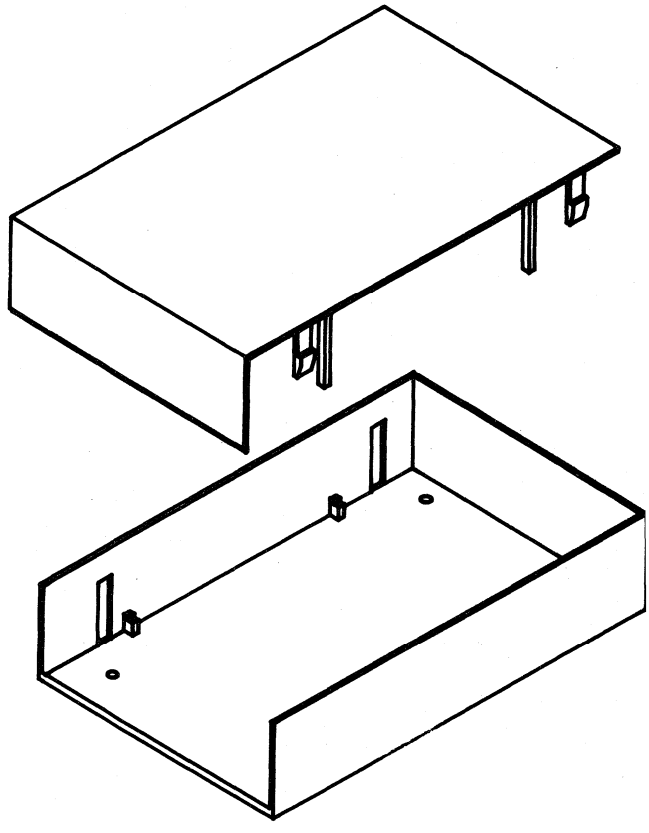
SIP Stik™ Prefabs

DALLAS SEMICONDUCTOR

DS9005
Eurocard Enclosure

FEATURES

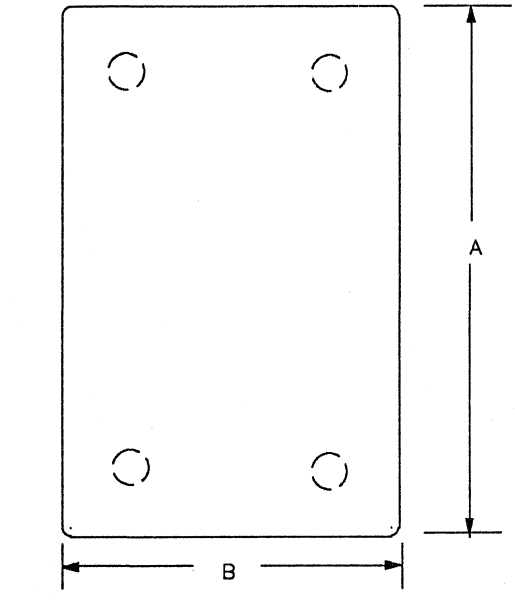
- Low cost molded enclosure
- Two-piece, snap together construction
- Made of rugged, flame-retardant polyester PBT plastic
- Accepts DS9006 SIP Stik Motherboard or any other single size Eurocard printed circuit board
- Can be custom machined to allow for connector requirements
- Component clearance of .230" solder side, 1.000" circuit side using .062" board
- Smooth indents on bottom side for rubber bumpers
- Hole knockouts for mounting



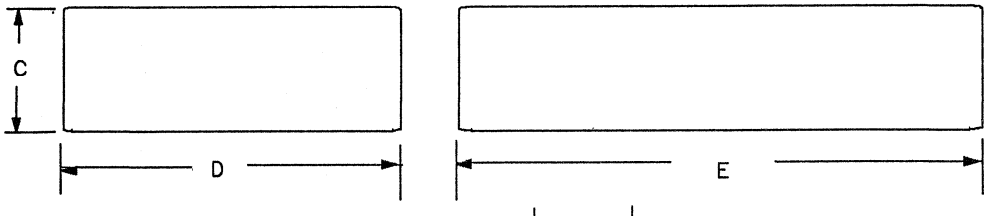
DESCRIPTION

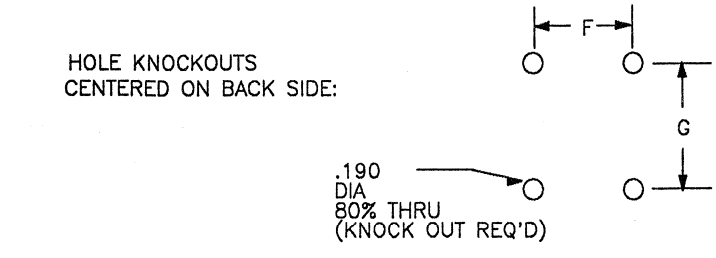
The DS9005 Eurocard Enclosure is a rugged, two-piece snap together plastic enclosure for any standalone system application. The PCB is offset in the enclosure to allow for components such as transformers and SIP Stiks to be positioned on the topside of the board while still leaving room for standard IC packages and discretes on the bottom side of the board. The housing is constructed of flame-retardant polyester PBT plastic to allow for applications requiring a very wide range of temperatures and is highly resistant to most chemicals. The size of the board and location of I/O connectors should match the DS9006 SIP Stik Motherboard. Applications include control units, handheld remote communications, and security systems.

DS9005
EUROCARD ENCLOSURE



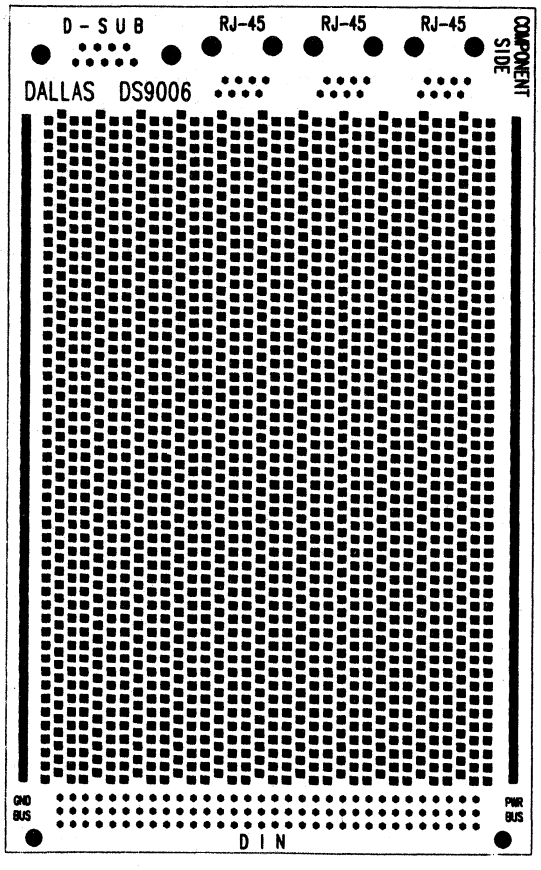
DIM.	INCHES	
	MIN.	MAX.
A	6.745	6.775
B	4.367	4.397
C	1.580	1.610
D	4.283	4.313
E	6.691	6.721
F	2.990	3.010
G	5.290	5.310





DALLAS SEMICONDUCTOR

DS9006
SIP Stik™ Motherboard



FEATURES

- Fits into DS9005 Eurocard Enclosure
- Plated through-hole pattern for wire wrap or solder mount development
- Allowance for up to 12 Stik connectors
- Hole layout for RJ45, D-SUB, and Eurocard DIN connectors
- Full length buses for distributing power and ground
- 1700 hole array for 0.1" center ICs and Stiks

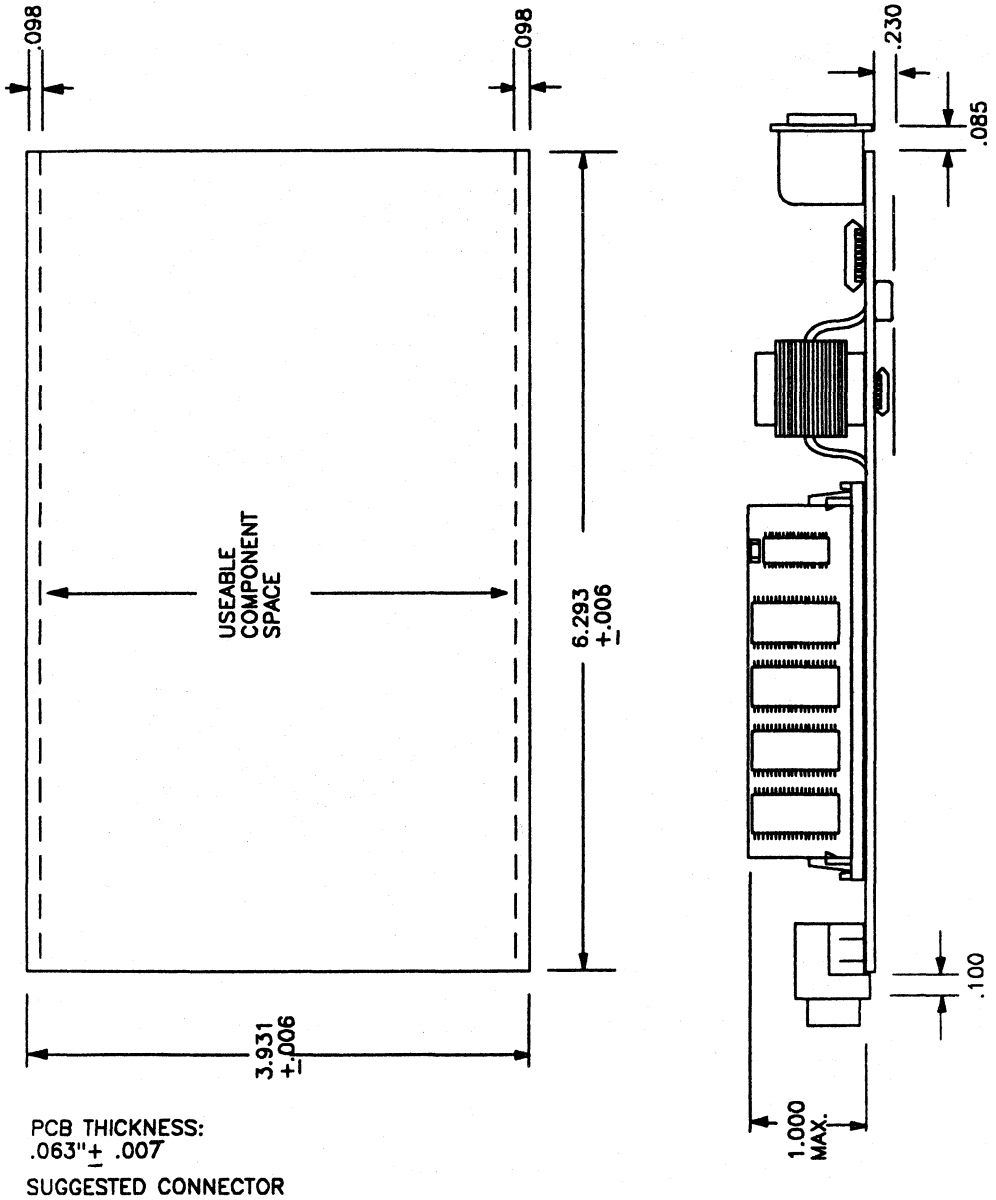
DESCRIPTION

The DS9006 SIP Stik Motherboard is a developmental printed circuit board for prototyping circuit designs which utilize Stik prefabs and/or RJ11/45 connector schemes. Many SIP Stiks mate with connectors that have staggered rows of pins. This makes it difficult to prototype these modules since most off-the-shelf wire wrap boards have a grid of 0.1" center holes. The DS9006 contains several rows of holes that are offset to accommodate both SIP Stiks and standard 300 mil and 600 mil DIPs.

Hole patterns for three RJ11/45, one 9-pin D-SUB, and 64/96-pin Eurocard connectors are located on the ends of the PCB in a right angle fashion to enable the finished circuit board assembly to mount in the DS9005 enclosure. This allows the designer to have a "complete" looking unit for presentation while still in the prototyping stage of design.

DS9006

ALL DIMENSIONS IN INCHES



PCB THICKNESS:
.063" ± .007

SUGGESTED CONNECTOR

PART NUMBERS:

RJ45– AMP #520252–4
9–PIN D–SUB FEMALE– AMP #745781–1
DIN–64 POS. FEMALE AMP# 531796–2

TYPICAL LAYOUT FOR
DS9005 ENCLOSURE

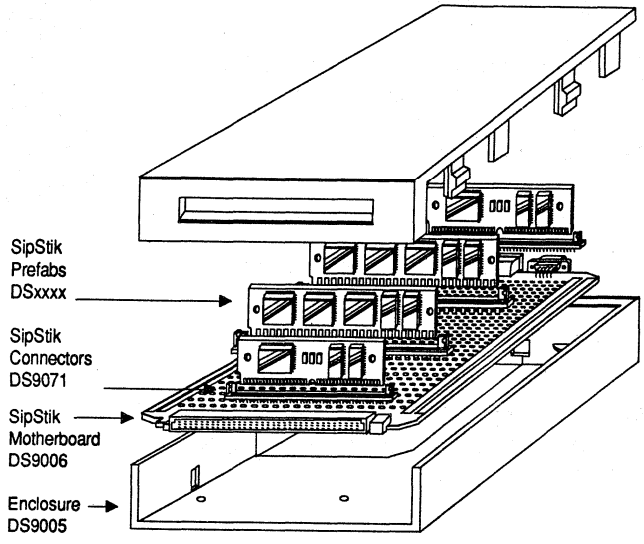
DALLAS SEMICONDUCTOR

DS9006K
SIP Stik™ Prototyping Kit

FEATURES

- DS9005 Eurocard Enclosure
- DS9006 SIP Stik Motherboard
- Sample connectors for 30-, 35-, and 40-contact SIP Stiks
- Adaptor pins for wire wrap
- Application note

3-D PACKAGING BOOSTS DENSITY



Eurocard Form Factor Shown. Stiks, RJ45, D-Sub, and DIN not included.

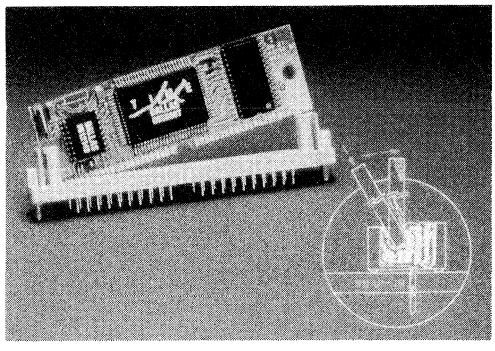
DESCRIPTION

The DS9006K SIP Stik Prototyping Kit includes a printed circuit board for prototyping SIP Stiks. The wire-wrapped unit can then be housed in a molded enclosure for standalone applications. An application note explains how to maximize use of the DS9006 SIP Stik Motherboard printed circuit board using SIP Stiks. See data sheets for the DS9005 Eurocard Enclosure and DS9006 for more information on these items.

DALLAS SEMICONDUCTOR

DS907x
SIP Stik™ Connectors

FEATURES



- Provides snap-in connection between SIP Stiks and motherboard
- Provides 200 grams minimum contact force on JEDEC standard modules
- Redundant contacts
- Low insertion force
- Heat-resistant housing (rated at 200° C)
- .050" and .100" centerlines as specified in table below
- Reference AMP Inc. MICROEDGE™ SIMM connector catalog for more detailed specifications.

Part Number	Description	Ref. AMP Part #	Length in.
DS9071-30V	30 contact vertical position .100" pitch	821828-2	3.800
DS9071-30I	30 contact inclined position .100" pitch	821876-2	3.800
DS9071-35V	35 contact vertical position .100" pitch	821828-3	4.300
DS9071-35I	35 contact inclined position .100" pitch	821876-3	4.300
DS9071H-35R	35 contact high profile right angle position .100" pitch	3-382488-5	4.300
DS9072-40V	40 contact vertical position .050" pitch	821918-2	2.950
DS9072H-40R	40 contact high profile right angle position .050" pitch	4-382486-0	2.950

Part Number	Description	Ref. AMP Part #	Length in.
DS9072L-40R	40 contact low profile right angle position .050" pitch	4-382480-0	2.950
DS9072-68V	68 contact vertical position .050" pitch	821-824-7	4.350
DS9072-68I	68 contact inclined position .050" pitch	821-907-6	4.350
DS9072H-68R	68 contact high profile right angle position .050" pitch	6-382486-8	4.350
DS9072L-68R	68 contact low profile right angle position .050" pitch	6-382480-8	4.350
DS9072-72V	72 contact vertical position .050" pitch	821824-8	4.550
DS9072-72I	72 contact inclined position .050" pitch	821907-7	4.550
DS9072H-72R	72 contact high profile right angle position .050" pitch	7-382486-2	4.550
DS9072L-72R	72 contact low profile right angle position .050" pitch	7-382480-2	4.550

Also available are 40-position DIP-to-SIP and SIP-to-DIP adaptors for development of DS2250 Micro Stik products.

Part Number	Description
DS9075	SIP-to-DIP adaptor
DS9076	DIP-to-SIP adaptor

Automatic Identification

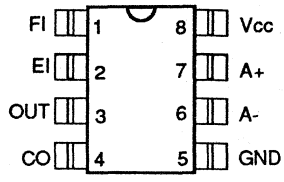
DALLAS SEMICONDUCTOR

DS1203S-B1
MicroPower Receiver Chip

FEATURES

- Input channel continuously listens for input signals up to 250 KHz
- Ultra low-power listening gives longevity to the 3 volt supply
- 30 mV P-P input signal drives output to supply levels
- Electronic freshness seal eliminates power consumption during storage
- Applications include RF, IR, or magnetic front end for wireless devices
- Space-saving , small outline surface mount package

PIN CONNECTIONS



8-PIN SOIC
(150 MIL)

PIN NAMES

Vcc	- 3 volt supply
GND	- Ground
FI	- Freshness Input
EI	- Enable Input
OUT	- Signal Output
CO	- Cycle Output
A+	- Noninverting Input
A-	- Inverting Input

DESCRIPTION

The DS1203S-B1 MicroPower Receiver Chip is an ultra low - power comparator circuit designed to listen for signals of up to 250 KHz. Input signals as small as 25 mV peak-to-peak are presented at the output as full power supply level signals. The DS1203S-B1 makes an ideal front end for wireless communication links via RF, IR, ultrasound or magnetic field. The ultra low power feature allows remote applications to be permanently powered by a single three-volt lithium energy source capable of lasting over ten years. A freshness seal can disconnect the power supply so that energy loss is avoided during periods of storage. The freshness seal is activated or deactivated through the use of a pulse packet protocol and the Freshness Input pin.

OPERATION

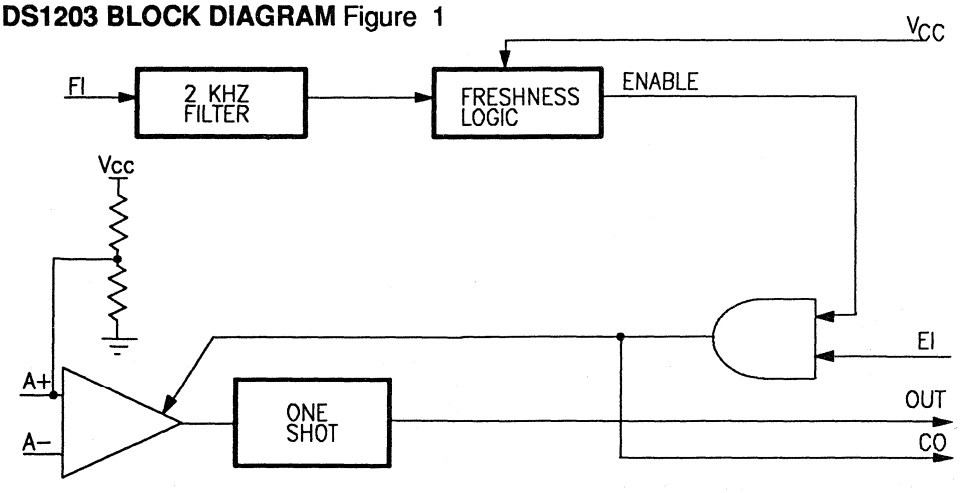
A block diagram of the DS1203S-B1 MicroPower Receiver Chip is illustrated in Figure 1. As shown, the device consists of a comparator which can be enabled by two sources. The enable input (EI) can be used to turn on the comparator directly, provided the freshness seal has been enabled. When the comparator is enabled, signals present at inputs A+ and A- of a magnitude greater than 25 mV peak-to-peak produce voltage swings between power supply input and ground at the output. In addition, the A+ input has a bias resistor of R_B approximately equal to 10M ohms to place the A+ pin at approximately $V_{DD}/2$. This facilitates differential reception.

FRESHNESS SEAL

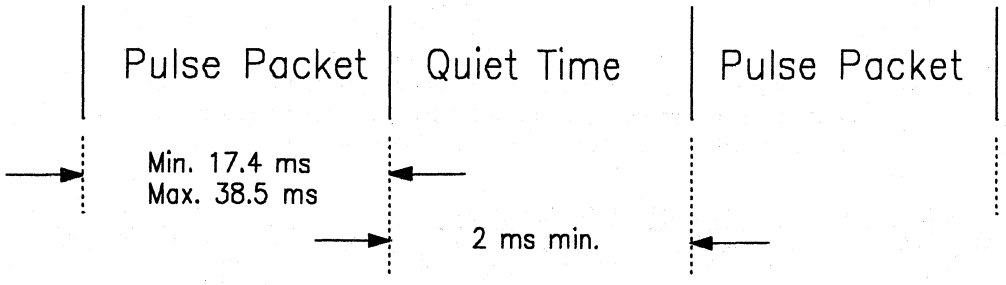
The freshness seal input pin (FI) is used to either stop or start DS1203S-B1 power consumption. This input accepts a pulse packet which is comprised of a series of pulses, representing either a logic 0 or a logic 1, separated by a 2 millisecond quiet time. Each pulse packet has a minimum aperture time of 17.4 milliseconds and a maximum aperture time of 38.5 milliseconds (see Figure 2). When the seal is broken, the comparator continuously listens for activity at the inputs. When the seal is intact, no listening occurs and the DS1203S-B1 enters a no power consumption mode.

Within this aperture time, a logic 0 is represented as 32 to 47 pulses. A logic 1 is represented as 48 to 63 pulses. The type of pulse packet command, either a seal or a break, is illustrated in Figure 3.

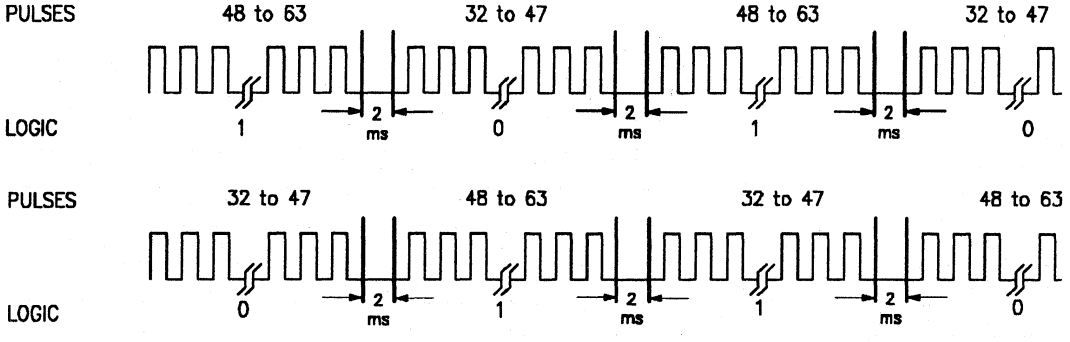
DS1203 BLOCK DIAGRAM Figure 1



FRESHNESS SEAL Figure 2



SEAL AND BREAK COMMAND Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground	0.5V to +7V
Operating temperature	0°C to 70°C
Storage temperature	-55°C to +125°C
Soldering temperature	260°C for 10 sec.

*This is a stress rating only and funtional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	2.5	3.0	5.5	Volts	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	Volts	1,2
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1,2
Input Sensitivity	V_{SIN}	25	20		MVolts	
FI Input Logic 1	V_{IHF}	1.1		V_{CC}+0.3	Volts	1
FI Input Logic 0	V_{ILF}	-0.3		0.4	Volts	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC}=2.5 to 3.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		1.0	uA	
Output Logic 1	V_{OH}	V_{CC}-0.3			Volts	1
Output Logic 0	V_{OL}			0.4	Volts	1
Operating Current	I_{CC}			3	uA	5
Power Down Current	I_{CC1}			50	nA	3
Output Current Logic 1	I_{OH}			250	uA	
Output Current Logic 0	I_{OL}			500	uA	
Propagation Delay	t_{PD}			30	uS	4
Comparator Sensitivity	V_{SINE}	25	20		mVpk-pk	6
Comparator Frequency	C_{FREQ}	0		250	KHz	
Comparator Input Resistance	R_{IMP}	1			M ohm	
Input Capacitance	C_{IMP}			5	pF	

NOTES:

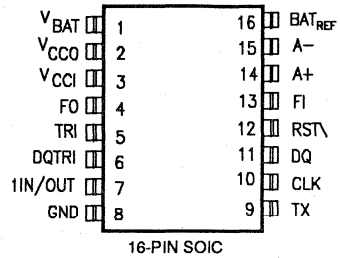
1. All voltages are references to ground.
2. Applies to the EI pin only.
3. Power drain from Vcc input when freshness seal is enabled; 2 uA when freshness seal is broken.
4. Propagation delay from comparator inputs to output.
5. Only for V_{CC}< 3.5 volts.
6. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.

DALLAS SEMICONDUCTOR

DS1209S-B1
Wireless to 3-Wire Converter Chip

FEATURES
- Adapts a wireless device to a 3-wire serial port (DQ, CLK, and RST\ signals)
- Up to 65,536 devices can be uniquely addressed within the same wireless proximity
- Receives IR, RF, or magnetic pulses as small as 25 millivolts peak-to-peak and frequencies up to 250 KHz
- Low-power operation for both battery backup and battery operate modes
- Internal automatic gain control (AGC) raises signal input levels above the noise floor
- Makes allowances for extra or missing pulses induced by noise in transmission path
- Counts input pulse packets to interpret data and commands
- Internal state machine generates commands and routes data to and from the 3-wire serial port
- Output pin can gate a variety of transmitting devices
- Simplex 1-wire port can override comparator inputs for input/output to 3-wire serial port
- 3-wire serial port connects to large family of products: DS1201 Electronic Tag, DS1204u Electronic Key, DS5000 Soft Microcontroller, DS1280 3-Wire to Bytewide Converter Chip

PIN CONNECTIONS



16-PIN SOIC
(300 MIL)

PIN NAMES (\ Denotes Condition Low)

BAT_{REF}	Battery Reference
V_{BAT}	Battery Input
V_{CCO}	Switched Output
V_{CCI}	+5V Input
1IN/OUT	1-Wire Input/Output Port
GND	Ground
TRI	Tristate DQ, CLK, RST\ Input
DQ TRI	Tristate Only DQ Input
TX	Wireless Transmit
RST\	RESET (3-Wire Port)
CLK	Clock (3-Wire Port)
DQ	Data Input/ Output (3-Wire Port)
FI/FO	Freshness Seal Input/Output
A+	Non-Inverting Comparator Input
A-	Inverting Comparator Input

DESCRIPTION
The DS1209S-B1 Wireless to 3-Wire Converter Chip is a low-power CMOS device designed to implement an addressable, full-duplex wireless to 3-wire communications channel. An internal state machine interprets pulse packets which are received at the comparator input pins and routes data to and from the 3-wire serial port. The TX output pin provides a return transmission link for data received from the 3-wire serial port and can gate a variety of transmitting devices. The low-power input comparator internal to the DS1209S-B1 is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz. An internal Automatic Gain Control (AGC) is used to address the problem of operating in a noisy environment where extraneous signals

may be falsely interpreted by the DS1209S-B1 as valid pulse packets. The AGC will automatically set the comparator input thresholds above the noise floor. The DS1209S-B1 also contains a 16-bit chip select value which is stored in the internal command prefix register. This chip select value allows up to 65,536 devices to be uniquely addressed within the same wireless proximity. The 1-wire input/output pin can be used to override the comparator inputs and allow a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. Additionally, a sophisticated power switching circuit is provided which allows for both battery backup and battery operate modes.

PIN DESCRIPTIONS

V_{BAT} - This input is designed to be connected to a battery with a voltage range between 2.5 and 4.0 volts. When V_{CCI} is grounded, the DS1209S-B1 acts as a battery-operate device and power is supplied from the V_{BAT} pin at all times. This input should NEVER be grounded. If single supply operation is selected, this pin MUST be the power input for the device.

V_{CCI} - This input is designed to be connected to a power supply with a voltage range of 4.5 to 5.5 volts. This voltage input is switched to the V_{CCO} pin as long as V_{CCI} is greater than V_{BAT}. However, when V_{BAT} is the greater, its voltage will be outputted. When both V_{CCI} and V_{BAT} inputs are used, the DS1209S-B1 is in the battery backup mode. V_{CCI} should be grounded when not being used.

V_{CCO} - Switched V_{BAT} or V_{CCI} output. V_{CCO} will always be the greater of V_{BAT} or V_{CCI}.

BAT_{REF} - This output pin represents the battery voltage input (V_{BAT}) less 0.6 volts. It is designed to be connected to the battery input pin on the attached 3-wire device.

1IN/OUT - This input/output pin provides an override for the comparator inputs and allows a device to communicate with the DS1209S-B1 in a simplex manner at one-half the frequency of the comparator inputs. The pin acts as an input pin for pulse packets containing both command and data input to the 3-wire serial port. Data is also output on the same pin when memory content is read via the 3-wire serial port.

FI/FO - The FI (Freshness In) and FO (Freshness Out) pins combine to give the DS1209S-B1 a method of conserving battery power until placed in service and determine if the low power consumption mode has been entered. The FI pin is used to start (break freshness seal) or stop (enable freshness seal) the continuous power consumption of the comparator on the DS1209S-B1 that is connected to the comparator input pins A+ and A- (Figure 6).

A+,A- - These are the inputs for the low-power comparator.

TRI - This input is used to tristate the 3-wire outputs CLK, RST\, and DQ. The TRI pin is active in a high state.

DQ TRI - This input is used to tristate the 3-wire DQ pin only. The DQ TRI pin is active in a high state.

TX - This output pin contains the data which is output from the 3-wire serial port. In a typical application this pin is used to key the wireless transmitter which will send data back to a wireless receiver.

RST\ - This output signal is the reset signal for the 3-wire serial port. When RST\ is at high level, the 3-wire port is active and data can be written into or read from the port.

CLK - This output signal is the clock signal for the 3-wire serial port. The clock signal synchronizes data into and out of the DQ line of the 3-wire serial port.

DQ - This input/output is the data input/output for the 3-wire serial port. In a typical application, RST\, CLK, and DQ connect directly to the RST\, CLK, and DQ pins on the DS1204 Electronic Key, DS1201 Electronic Tag, DS1207 TimeKey, or DS1280 3-Wire to Bytewide Converter Chip.

GND - This pin is the ground.

OPERATION

The principle blocks of circuitry contained within the DS1209B-S1 are shown in Figure 1. During normal input conditions, pulse packets present at the comparator input pins pass through the input selector to the pulse counter. The 1-wire port is selected for data input by exception when data is present at the 1-wire port. This data will override the comparator inputs. The 1-wire port pin will be discussed in more detail later in this text. Input pulses arriving at the pulse counter are deciphered into various command codes which affect the command prefix shift register, the state machine, and ultimately the 3-wire serial port. The various command codes are listed in Table 1.

Pulse packets are input to the pulse counter with a 50 *us* dead time after the last pulse in each packet. The DS1209S-B1 uses the dead time to determine how many pulses were sent and the action to be taken. In addition, if input to the pulse counter is low (inactive) for longer than 1.5 ms, the DS1209S-B1 will time out, reset the command prefix shift register, and place the state machine into an inactive state.

As can be seen in the block diagram of Figure 1 and the command codes listed in Table 1, the input pulses are sent in two different directions. If a pulse packet of 100 pulses (greater than 90) arrives at the pulse counter, the next 24 pulse packets are sent to the command prefix shift register, and the state machine is set inactive. The 100-pulse packet always sets the state machine to inactive regardless of any action which may have been occurring (aborts current action/ conversation).

The 24 pulse packets which go to the command prefix shift register will cause a normal wake-up or mask wake-up, a read of the chip select bits, a write of the chip select bits, or a lock of the chip select bits. The chip select bits make up the first 16 bits of the 24-bit command prefix shift register. The last eight bits comprise the function field. See Figure 2 and Table 2.

NORMAL WAKE-UP AND MASK WAKE-UP

The only difference between normal wake-up and mask wake-up is the number of chip select bits which must be matched to wake-up the state machine. For example, if a function code indicates the use of all chip select bits, then all 16 bits must be correctly matched to enable the main state machine. The following step-by-step procedure will illustrate normal and mask wake-up:

1. First a 100-pulse packet is sent to the comparator input pins, which puts the state machine into an inactive state.

2. Issue wake-up or mask wake-up by sending the 8-bit function code followed by the 16 chip select bits to enable the state machine. The command prefix register is always loaded by sending write zeroes (20-pulse packets) or write ones (40-pulse packets). The loaded pulse packets are compared to values stored in the 8-bit Function Code Table and the previously stored 16 chip select bits (storing the chip select values will be covered later). When masking is being used, the first bits entered (LSBs) are the last to be masked. For example, Bits 0 and 1 will be the only bits unmasked if mask 2-15 is selected.

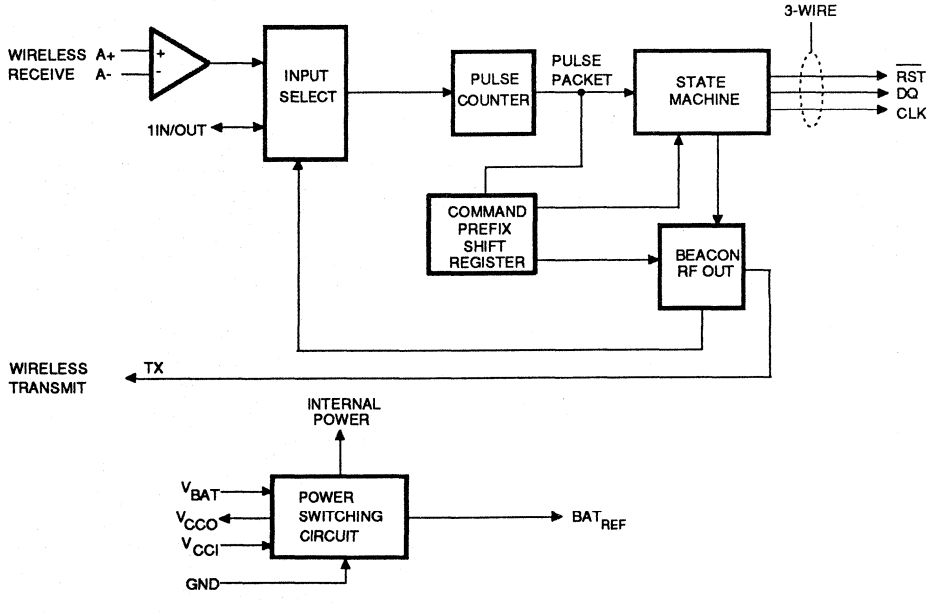
Pulse packets of 50 to 89 pulses are ignored when loading the command prefix shift register. A pulse packet of greater than 90 pulses always initializes the command prefix shift register back to starting with the LSB and aborts any previous transaction. The state machine is also set inactive. After the first 24 bits are received and a valid wake-up is decoded, the command prefix shift register will no longer allow data bits to be written into it and the enable output will become

B1 COMMAND CODES Table 1

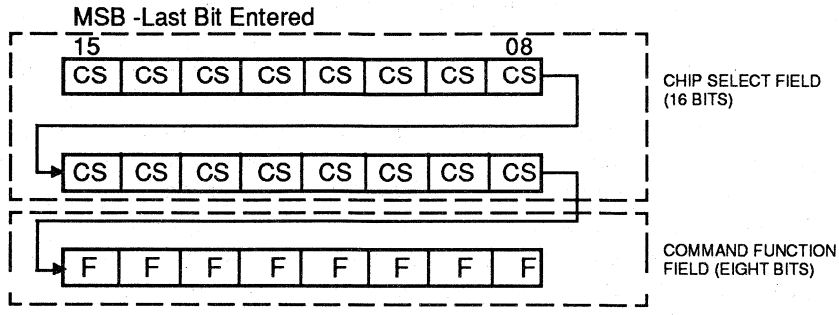
Number of Pulses			Command
Min.	Typ.	Max.	
5	20	29	Write 0 or READ
30	40	49	Write 1
50	60	69	Take $\overline{RST}$ High
70	80	89	Return to Inactive State
90	100	109	Initialize Protocol and Put State Machine Inactive

NOTE: Pulse packets are sent with a minimum of 50 us quiet time after each pulse packet and a maximum quiet time of approximately 1.5 ms.

DS1209S-B1 BLOCK DIAGRAM Figure 1



24-BIT COMMAND PREFIX SHIFT REGISTER BIT PATTERN Figure 2



B1 FUNCTION CODES Table 2

FUNCTION	MSB			FUNCTION CODE				LSB	RESULTS
Wakeup	0	0	0	1	1	0	0	0	Mask All Bits
Wakeup	0	0	0	1	0	0	0	1	Mask All CS Bits 2-15
Wakeup	0	0	0	1	0	0	1	0	Mask CS Bits 4-15
Wakeup	0	0	0	1	1	0	1	1	Mask CS Bits 6-15
Wakeup	0	0	0	1	0	1	0	0	Mask CS Bits 8-15
Wakeup	0	0	0	1	1	1	0	1	Mask CS Bits 10-15
Wakeup	0	0	0	1	1	1	1	0	Mask CS Bits 12-15
Wakeup	0	0	0	1	0	1	1	1	Mask CS Bits 14-15
Wakeup	0	0	1	0	1	0	0	0	Use all CS Bits
Read CS Bits	0	0	1	0	1	0	1	1	Ignore CS Bits
Store CS Bits	0	0	1	0	1	1	0	1	Write all CS Bits
Lock CS Bits	0	0	1	0	1	1	1	0	Use all CS Bits
Reset AGC	0	0	1	0	0	1	1	1	All CS Bits

active and remain active until another 100-pulse packet is received to reinitialize. Subsequent pulse packets which are received will be directed to the state machine with action taken corresponding to the number of pulses received as shown in Table 1.

A pulse packet of 80 pulses, followed by a 20-pulse packet, followed by a 40-pulse packet, enables the beacon mode of the state machine. Beacon mode turns on and off the TX pin at a 5 KHz rate for 1.2 seconds. In a typical application utilizing the DS6065A, this signal can be used to key a transmitter (the DS6065A operates at 303.875 MHz), which allows a base unit to lock onto the transmitted beacon.

4. The DS1209S-B1 is now placed in the active state by issuing a 60-pulse packet which takes RST\ high on the 3-wire serial port. This same 60-pulse packet also turns off the beacon if it has not already timed out. With RST\ high a conversation can now take place between devices placed on the 3-wire port (DS1201, DS1204, DS1207, or DS1280) from the comparator inputs, and data is returned to the sending unit via the TX pin. As pulse packets continue to be received, the device attached to the 3-wire port will be written and read using 20- and 40-pulse packets and reset with a 60-pulse packet. The reset pulse packet will take RST\ low until the next pulse packet is detected after the 50 us dead time. When data is read from the 3-wire port, it is always sent to the TX pin for transmission back to the sending unit.

5. If an 80-pulse packet is received, the state machine will go to an inactive state but still remains alert for new pulse packets.

6. If no pulse packets are received for more than 1.5 ms, the DS1209S-B1 will time out, initialize the command prefix shift register, and set the state machine back to the inactive state. The DS1209S-B1 now waits for new inputs to the protocol serial shift register which begin with a 100-pulse packet.

READING THE CHIP SELECT BITS

The 16-bit chip select (CS) value stored in the command prefix shift register can be determined in several ways. In fact, an exhaustive search could be implemented with a trial and error method which would eventually eliminate all but the correct bit pattern. Obviously, this method is painfully slow as 2^{16} possible combinations may need to be tried. In a similar but much more expedient manner, mask bits can be used in a successive approximation manner to determine the value of the CS bits. This procedure is accomplished by gradually increasing the size of the unmasked chip select fields as each set of bits is identified. However, the simplest method of determining the 16-bit CS value is to read the 16-bit value directly. The following step-by-step procedure will illustrate how to read the chip select bits.

1. Wake up the DS1209S-B1 by using the mask all function code. This is accomplished by sending a 100-pulse packet followed by 24 20-pulse and 40-pulse packets. The first eight pulse packets must match the mask all function code. The last 16 pulse packets can be any combination of 10- and 20-pulse packets as the 16 CS bits are masked. Next the beacon mode of the state machine is enabled by sending an 80-pulse packet followed by a 40- and then a 20-pulse packet. If the beacon mode has been enabled, it should be disabled after receiver lock-on by sending a 30-pulse packet to the comparator inputs.

2. Now load the DS1209S-B1 command prefix shift register with the read CS bits function code. This is accomplished by sending a 100-pulse packet followed by 24 20- or 40-pulse packets. As before, the first eight pulse packets must match the read CS bits function code. However, the last 16 pulse packets can be any combina-

tion of 20- and 40-pulse packets, as the 16 CS bits are ignored. During the 24-bit command prefix shift register load, pulse packets of 60 and 40 are ignored. As usual, pulse packets of 100 will initialize the command prefix shift register and set the state machine inactive.

3. If the 8-bit function code in the command prefix shift register is correctly matched, then for each 20-pulse packet (read command) received at the comparator input pins, one bit of the 16-bit CS field will be read at the TX pin, the LSB of the field appearing first. Thus, it will receive 16 packets of 20 pulses each to read the entire CS field. If more than 16 read pulse packets are sent to the comparator input pins in this mode, the DS1209S-B1 will start over again reading the CS bits, beginning with the first bit. Pulse packets of 40, 60, or 80 pulses are ignored and 100-pulse packets will initialize the command prefix shift register and set the state machine inactive. This is a non-destructive read and can be aborted at any time during the read process.

4. During the entire CS bit read operation, the state machine is disabled. All pulse packets except the 100-pulse packet are ignored by the state machine. As usual, the 100-pulse packet or a time-out of 1.5 ms will initialize the command prefix shift register and return the state machine to inactive.

STORING THE CHIP SELECT BITS

In order to store a new value into the chip select bits of the protocol shift register, it is necessary to know the existing stored value. In addition, if the lock bit is set, a new value for the chip select bits cannot be stored unless power is removed and reapplied. The lock function is only useful in applications where power is permanently applied or removed by exception. The existing value of the CS bits should be obtained using the procedure described in the "Reading Chip Select Bits" section. After obtaining the existing chip select values, a new value can be entered by using the step-by-step procedure which follows:

1. Load the proper 24-bit pattern into the command prefix shift register for storing the chip select bits. This pattern consists of 24 20-pulse and 40-pulse packets. The first eight packets must match the stored CS bits function code. The last 16 pulse packets must match the existing CS bits. During the 24-bit shift register load, only 20- and 40-pulse packets are accepted while 40-, 60-, and 80-pulse packets are ignored. As always, 100-pulse packets will initialize the command prefix shift register and set the state machine inactive.

2. If the 8-bit function code and the 16 CS bits are correct, the next 16 pulse packets will store a new CS value, overriding the old CS bits. Only 20-pulse and 40-pulse packets are accepted. Pulse packets of 60 and 80 are ignored and 100-pulse packets cause the stored CS bit command to abort, initializing the command prefix shift register and returning the state machine to inactive. The DS1209S-B1 does not lock up after 16 pulse packets are sent in this mode. If more packets are sent, the new packets will continue to shift in, storing the last 16 packets that are received.

3. During the entire store CS bits operation, the main state machine is disabled. All pulse packets received will have no effect on the state machine except the 100-pulse packet, which will initialize the command prefix shift register and return the state machine to an inactive state. A time-out of 1.5 ms will have the same effect as a 100-pulse packet.

LOCKING THE CHIP SELECT BITS

The design of the DS1209S-B1 allows for both battery backup and battery operation. The device consumes only modest amounts of power. As a result, most applications for this device are permanently powered and memory elements within the device, like the command

prefix shift register CS bits, are nonvolatile. A special latch is provided so that upon initial power- up (when battery is first connected) the nonvolatile chip select bits can be written with a store CS function code.

The CS bits can be changed as often as desired, using the store function until a lock CS function code is issued. Once sent, the value of the chip select bits cannot be changed until power is removed (battery disconnected) from the DS1209S-B1. The lock CS bit can be accomplished by the following step-by-step procedure.

1. If the CS value is unknown, the procedure for reading the CS bits should be followed so that the value is known.

2. The 8-bit function code for locking the CS bits is transmitted, followed by the 16-bit chip select value. Only 20- and 40-pulse packets are accepted; 60- and 80-pulse packets are ignored. A 100-pulse packet will cause the lock CS bits to abort, initializing the command prefix shift register and returning the state machine to the inactive state.

3. Once the 24-bit command prefix shift register is loaded with an exact match for the CS bits and the lock CS function code, the latch is set automatically and no further action is required.

4. The only way the latch can be reset is to remove power (the battery) from the device. During the lock CS operation the main state machine is disabled so that all pulse packets have no effect. As usual, a 100-pulse packet or a time-out of 1.5 ms will initialize the command prefix shift register and return the state machine to inactive.

POWER SWITCHING CIRCUIT

As shown in the block diagram of Figure 1, the DS1209S-B1 can receive its power from two different sources: the V_{CCI} input or the V_{BAT} input. The DS1209S-B1 is designed to work off of a battery supply as low as 2.5 volts. However, if an alternate supply is available, it can be connected to the V_{CCI} pin. A voltage level of 3 volts minimum is required on the V_{BAT} pin for proper operation. With both the V_{CCI} pin and the V_{BAT} pin attached to appropriate power sources, the DS1209S-B1 will automatically select the supply input which is the higher level. If only one power source is connected, it **MUST** be connnected to the V_{BAT} input. The V_{REF} output is designed specifically to supply power to a connected 3-wire device such as a DS1204, DS1201, DS1207, or DS1280. The V_{REF} output is equal to the V_{BAT} input less a voltage drop of about 0.5 volts. This pin is capable of sourcing a current of 2 mA.

PULSE PACKETS

The minimum time between pulse packets is 50 *us* and the idle time of 1.5 ms will always cause the protocol shift register to initialize and the state machine to go inactive.

Pulse packets range from 20 pulses to 100 pulses, depending on the action to be taken (see command codes in Table 1). If a read pulse packet is detected, data is to be read from a device connected on the 3-wire serial port and the TX pin will become active high for a logic one or remain low for a zero. Time is allotted beyond the 50 *us* between pulse packets for the DS1209S-B1 to send out a one or a zero. This time is specified as a 375 *us* window. If a logic zero is being sent, the TX pin will remain low for the entire window. If a logic one is being sent, the TX pin will be driven to high level within a maximum of 75 *us* and will remain high for a minimum of an additional 150 *us*.

However, if a minimum of four pulses is received at the comparator inputs, the TX pin activity is terminated on the assumption that a logic one has been received and the sending unit has started the next pulse packet. The timing diagram of Figure 3 illustrates the comparator out-

put and the TX pin timing relationship.

COMPARATOR AND AGC OPERATION

The low-power comparator inputs are brought out to the user on the A+ and A- pins. The low-power input comparator is designed to listen for signals with amplitudes as small as 25 millivolts peak-to-peak and frequencies of up to 250 KHz. To address the problem of a noisy environment where extraneous pulses are being generated and disrupting the dead time required for the pulse packets to be counted as groups of 20, 40, 60, 80, or 100 pulses, an automatic gain control (AGC) has been included.

The AGC decreases the sensitivity of the input in steps of 1/1.5. The pulse counter that normally would be looking for 20-100 pulse packets will count up to 255 (or some other number that is laser-programmable between zero and 255) and then clock a second 4-bit AGC counter that initially is reset to 0000. Upon receipt of 255 pulses at comparator inputs the AGC counter is incremented to 0001.

The 16 binary states of this 4-bit AGC counter are used to adjust the sensitivity of the RF input. The counter value 0000 is the maximum sensitivity and 1111 is the minimum. The final input sensitivity is a factor of 2.28×10^{-3} times the initial input sensitivity value (15 steps, each of which is 1/1.5 the sensitivity of the previous value).

Once an input sensitivity has been reached that allows for an adequate dead time to evaluate 20-100 pulse packets, the AGC counter is automatically incremented once more to move slightly further above the noise floor. At this point the 4-bit AGC counter stops incrementing and the transaction can proceed normally.

At the conclusion of the transaction a command can be issued to return the AGC counter to the 0000 state. All CS bits must match for this command and the 8-bit function code required is 00100111. Alternatively, after approximately one second of no pulses, the AGC counter will automatically reset itself to 0000.

1IN/OUT

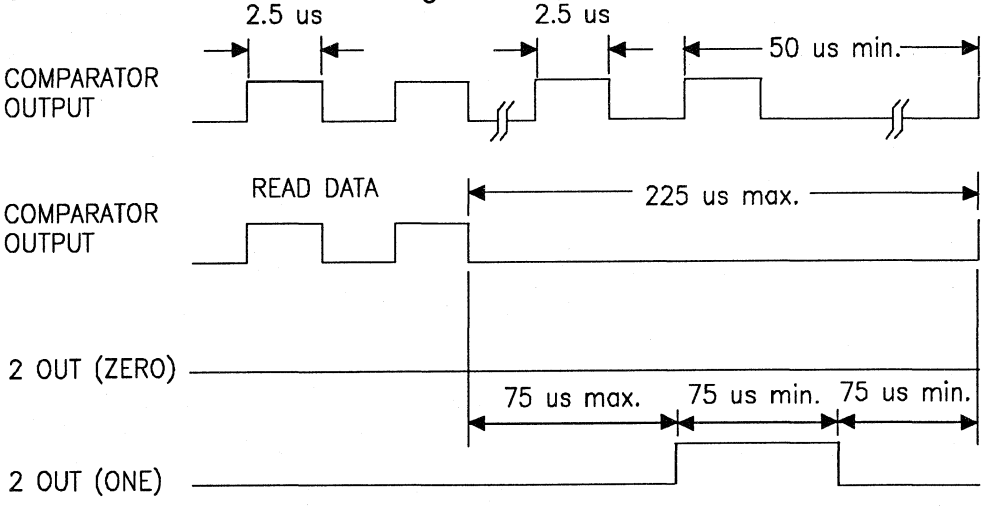
This pin is an input/output one-wire signal port designed to override the comparator input pins and multiplex the TX pin on a single connection. Data is input on the port pin using a frequency of one-half the comparator input frequency with a symmetrical high and low time of 5 *us* +/- 20%. Therefore, the time between pulse packets is 2X the time allotted between pulse packets when 250 KHz is used. If a read pulse packet is detected, time is allotted beyond the 100 *us* between pulse packets for the DS1209S-B1 to send out a one or a zero. This time is specified as a 450 *us* window. If a logic one is being sent, the 1IN/OUT pin will remain low for the entire window. If a logic zero is being sent, the 1IN/OUT pin will be tristated to a high impedance state by the DS1209B and should be pulled high using a pullup resistor. This high impedance state will occur within a maximum of 150 *us* and remain for a maximum of 150 *us*. The 1IN/OUT pin is guaranteed to be inactive after a third 150 *us* time period. The timing diagram of Figure 4 illustrates the 1IN/OUT timing.

RST\, CLK, AND DQ

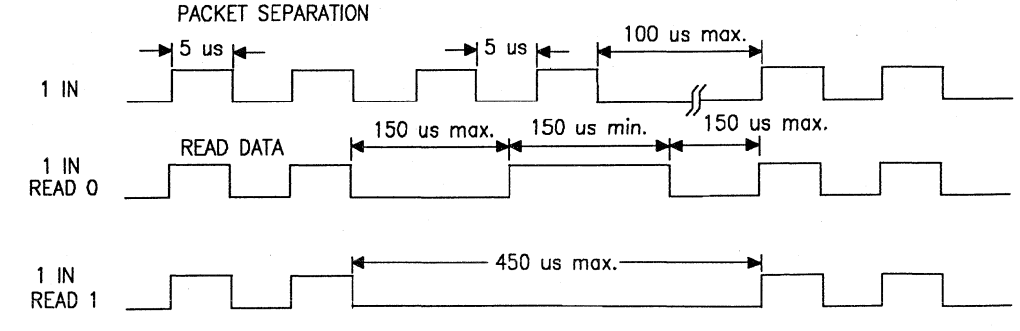
The 3-wire serial port on the DS1209S-B1 consists of the RST\, CLK, and DQ signals. These signals are designed to connect directly to the CLK, RST\, and DQ lines of various 3-wire devices, such as the DS1204, DS1207, DS1201, or DS1280. The RST\ pin on the DS1209S-B1 is driven to a high level whenever a 60-pulse packet is received by the state machine. The RST\ signal remains high until a 80- or 100-pulse packet is received or until 1.5 ms has elapsed without activity at the comparator inputs. The CLK pin on the DS1209S-B1 is normally high until the RST\ signal is high. When RST\ is high and a 20- or 40-pulse packet is received by the state machine (indicating a "read from" or "write

to" the 3-wire port), the CLK pin is driven low for a period of 500 ns minimum to 1.0*us* maximum. If data is being read from a device on the 3-wire serial port, it will become valid within 200 ns of the falling edge of the clock returned to the sending unit. The output will be a high level for a logic one or remain at low level for a logic zero. If data is being written to a device on the 3-wire serial port, then data will be sent from the state machine to the DQ line prior to the falling edge of the clock. This data will remain valid until the clock transitions back to a high level. The TX pin remains low while data is being written to the 3-wire serial port. A timing diagram for the 3-wire serial port is shown in Figure 5. For more detailed information on the 3-wire serial port, see the data sheets on the DS1201, DS1207, or DS1280.

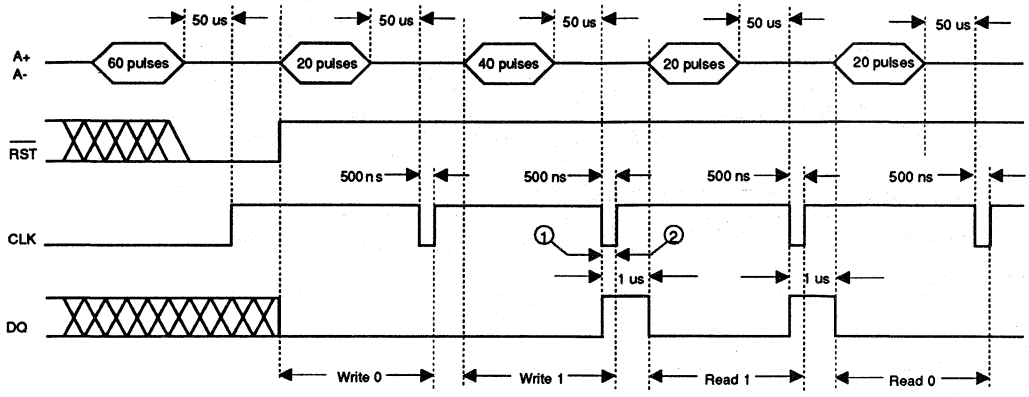
COMPARATOR INPUT TIMING Figure 3



1IN/OUT TIMING Figure 4

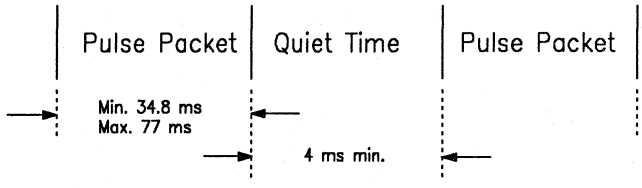


RST\, CLK, AND DQ TIMING Figure 5

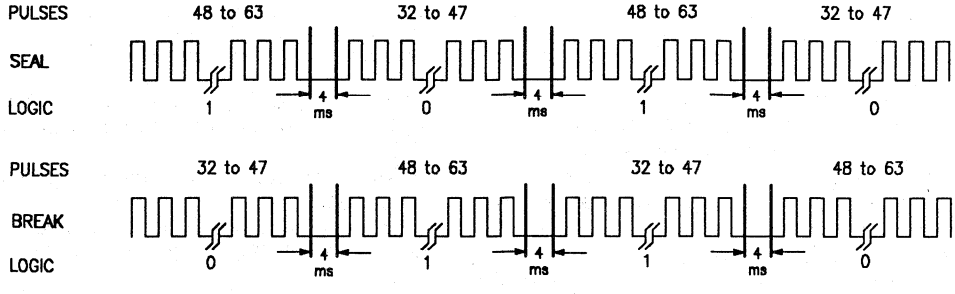


(1) Data setup time: 100 us min.
(2) Data hold time: 100 us max.

FRESHNESS SEAL Figure 6



SEAL AND BREAK COMMAND



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative to Ground	0.5V to +7V
Storage Temperature	-55° to +125°C
Operating Temperature	0° to 70° C
Soldering Temperature	260° for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply Input	V_{CCI}	3.0	5.0	5.5	Volts	1,2
Battery input	V_{BAT}	2.5		4.0	Volts	1,2
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	Volts	1,3
Input Logic 0	V_{IL}	-0.3		0.8	Volts	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, V_{BAT} =3 V, 0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Battery Reference	V_{REF}	V_{BAT} -0.7		V_{BAT}	Volts	1
Switched Voltage Out	V_{CCO}	V_{CCI} -0.3			Volts	1,4
Switched Current Out	I_{CCO}	3	4		mA	5
Operating Current	I_{CC}		2	75	uA	6
Standby Current	I_{cc1}			2	uA	7
Output Logic 1	V_{OH}	V_{CC} -10%			Volts	1,3
Output Logic 0	V_{OL}			0.4	Volts	1
Output Current Logic 1	I_{OH}			250	uA	
Output Current Logic 0	I_{OL}			500	uA	
Comparator Leakage Current	I_L	-1.0		1.0	uA	8
Comparator Sensivity	V_{SINE}	25	20		mV	9
Comparator Frequency	C_{FREQ}	40		250	KHz	
Comparator Input Resistance	R_{IMP}	1			M ohm	
Input Capacitance	C_{IO}			5	pF	

NOTES:

1. All voltages are referenced to ground.
2. When both the battery and supply pins are being used, V_{CCI} should be at least 500 mV higher than V_{BAT} when V_{CCI} is supplying power.
3. V_{CC} applies to the greater of V_{CCI} or V_{BAT} depending on which input is supplying power.
4. V_{CCO} is either V_{CCI} -0.3 V or V_{BAT} -0.3 V.
5. I_{CCO} is current coming from V_{BAT} or V_{CCI} depending on which input is supplying power.
6. Operating current comes from V_{CCI} or V_{BAT} depending on which is supplying power and if power is consumed by the DS1209S-B1 when comparator or 1-wire is active.
7. With freshness seal not broken, receiver standby current is 50 nA.
8. Leakage current applies to all inputs except V_{CCI} and V_{BAT}. 1 IN/OUT, TRI, and DQTRI have 150 uA max. leakage to ground.
9. Input signal is a sine wave, measured in peak-to-peak millivolts at a frequency of 133.3 KHz.

DALLAS SEMICONDUCTOR

DS1280
3-Wire to Bytewide Converter Chip

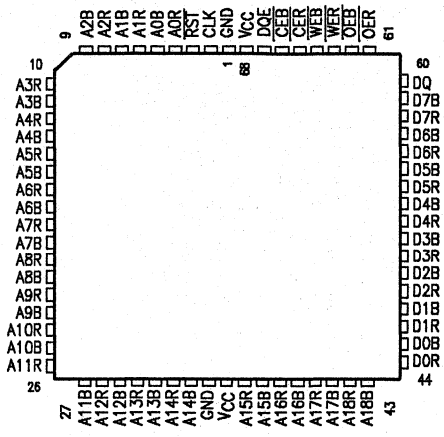
FEATURES

- Adapts JEDEC bytewide memory to a 3-wire serial port
- Supports 512K bytes of memory
- 68-pin version provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery backup and battery operate applications
- Cyclic redundancy check monitors serial data transmission for error
- Available in 68- PLCC surface mount package; 44- or 80-pin quad flat pack for high density requirements

ORDERING INFORMATION

DS1280Q-XX	-68	68-pin PLCC
DS1280FP-XX	-80	80-pin Flat Pack
	-44	44-pin Flat Pack

PIN CONNECTIONS



DS1280Q-68
68-PIN PLCC

PIN NAMES (\ Indicates Condition Low)

RST\	Reset For Serial Port
DQ	Data Input/Output For Serial Port
CLK	Clock Input For Serial Port
DQE	Serial Port Active Output
CEB\	System Bus Enable
OEB\	System Bus Read Enable
WEB\	System Bus Write Enable
A0B-A18B	System Address Bus
D0B-D7B	System Data Bus
CER\	RAM Chip Enable
WER\	RAM Write Enable
OER\	RAM Output Enable
A0R-A18R	RAM Address Bus
D0R-D7R	RAM Data Bus
GND	Ground
V_{CC}	+5 Volts

DESCRIPTION

The DS1280 adds a 3-wire serial port to a bytewide static RAM yet maintains the existing bytewide port. Memory capacity of up to 512K bytes can be addressed directly. Arbitration between the serial and bytewide port is accomplished by handshaking or using predictable idle time as an access window. The serial port requires a six-byte protocol to set up memory transfers. Cyclic redundancy check circuitry is included to monitor serial data transmission for error.

PIN DESCRIPTION

RST - The 3-wire serial port selection signal input. When RST is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK - The clock input signal is used to input or extract data from the 3-wire serial port. A clock cycle is defined as a falling edge followed by a rising edge. Data is driven out onto the 3-wire bus after a falling edge during read cycles and latched into the port on the rising edge during write cycles.

DQ - The DQ signal is the bidirectional data signal for the 3-wire serial port.

DQE - The DQE output signal is active (high level) whenever the 3-wire serial port is driving the DQ line. Therefore, this pin will be high whenever data is being read. Otherwise it will be low and the DQ line will be an input. This signal can be used as a means of tri-stating the DQ driver on the other end.

CER - Chip enable output to RAM. This signal is asserted active (low) during RAM read or write cycles. This signal is either derived from the system bus chip enable (CEB\) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

WER - Write enable output to RAM. This signal is asserted active (low) during RAM write cycles. This signal is either derived from the system bus write enable (WEB\) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

OER - Output enable to RAM. This signal is asserted active (low) during RAM read cycles. This signal is either derived from the system bus read enable (OEB\) or from a 56-bit protocol provided by the 3-wire serial port and associated timing circuits.

A0R-A18R - Addresses supplied to RAM. These signals allow access to up to 512K bytes of RAM controlled by the DS1280. The addresses are either derived from the system address bus (A0B-A18B) or from the protocol and internal binary counter provided by the 3-wire serial port and associated timing circuits.

D0R-D7R - Data bus supplied to RAM. These eight signals comprise the bidirectional data bus between external bytewide RAM and the DS1280. This data bus is either derived from the system data bus (D0B-D7B) or from the protocol and data stream provided by the 3-wire serial port and associated timing circuits.

CEB - System bus chip enable to the DS1280. This signal is used to generate the RAM chip enable for transfer of data to and from the parallel system bus to RAM (68-pin package only).

OEB - System bus output enable (read) for transfer of data from RAM to the parallel system bus (68-pin package only).

WEB - System bus write enable to the DS1280. This signal is used to generate the RAM write enable for transfer of data from the parallel system bus to the RAM (68-pin package only).

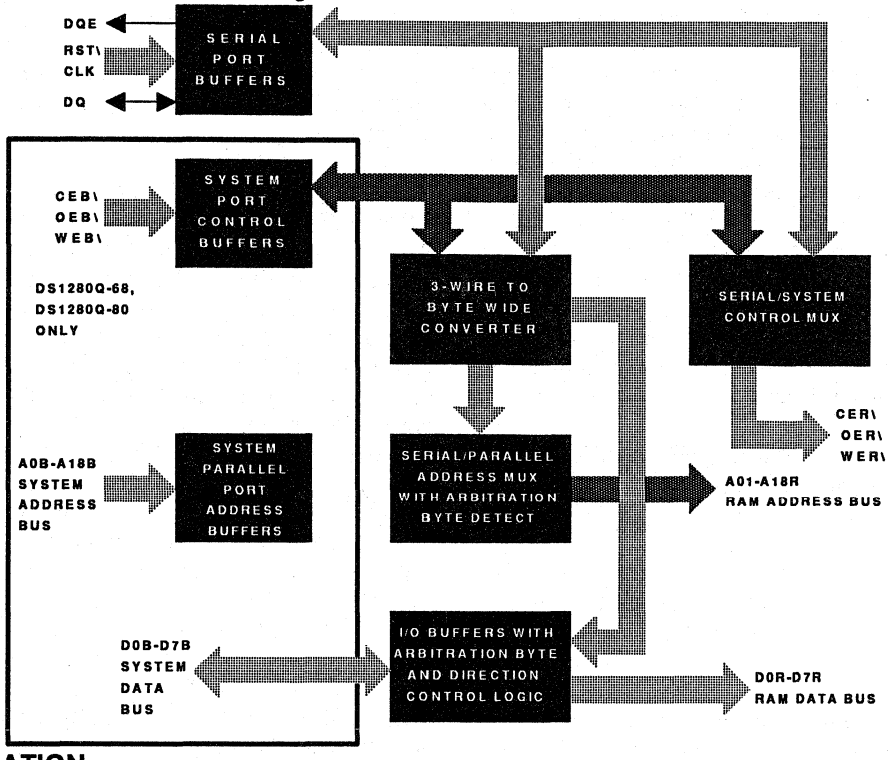
A0B-A18B - System bus addresses to the DS1280. These signals are used to specify the address location for data transfer to and from RAM (68-pin package only).

D0B-D7B - System data bus to and from the DS1280. This bidirectional bus is used to carry data to and from the parallel system bus and RAM (68-pin package only).

Vcc - +5volt power from the DS1280 (2 pins).

GND - Ground for the DS1280 (2 pins).

DS1280 BLOCK DIAGRAM Figure 1



OPERATION

Figure 1 illustrates the main elements of the DS1280. As shown, the DS1280 has two major sections; a 3-wire to bytewide converter and a serial/parallel multiplexer. The source of the serial/parallel multiplexer is either a 3-wire serial port or a bytewide system bus. Arbitration of the serial/parallel multiplexer is controlled by signals from the 3-wire to bytewide converter. The 3-wire serial port, therefore, has priority in accessing the RAM and the methods used to avoid collisions are primarily directed by the 3-wire to bytewide converter.

SYSTEM BYTEWIDE PARALLEL BUS

If the RST\ signal for the 3-wire serial port is low (inactive), the bytewide parallel port can access associated RAM directly. The bytewide parallel bus addresses (A0B-A18B) and control signals (CEB\, OEB\ and WEB\) are buffered by the DS1280 and become outputs A0R-A18R, CER\, OER\, and WER\ respectively, which are connected directly to RAM. The data input/output signals (D0B-D7B) are internally buffered and sent to RAM on the data input/output signals D0R-D7R. The buffering is designed to handle bidirectional data transfer. Data will be written from the bytewide parallel bus to RAM when CEB\ and WEB\ inputs are both active (low). The OEB\ signal is a "don't care" signal during a write cycle. Data is read from RAM via the bytewide parallel port when CEB\ and OEB\ signals are both low and WEB\ is high.

3-WIRE SERIAL BUS

If the RST signal for the 3-wire serial port is active (high), the 3-wire to bytewide converter controls the RAM through the control/address/data multiplexers. The 3-wire to bytewide converter uses a 56-bit protocol written serially using RST\, DQ, and CLK to determine the action required and also the starting address location in the RAM to be used. Data is entered

into the 3-wire while RST\ is high on the low-to-high transition of the CLK signal provided the data is stable on the DQ line with the proper setup and hold times. The last 8 bits of the 56-bit protocol are a cyclic redundancy check byte (CRC) that ensures that all bits of the protocol have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can catch up to three single bit errors within the 56-bit protocol and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written. More discussion on CRC use and CRC generation will follow later in this text.

PROTOCOL: 3-WIRE SERIAL BUS

The 3-wire serial bus protocol can cause eight different actions to occur as shown in Table 1.

The organization of the 56-bit protocol is shown in Figure 2. As defined, the first byte of the protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7, and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the command field. The control field bits are defined in Table 2.

A burst read uses a 19-bit address field which consists of the second, third, and bits 0, 1, and 2 of the fourth byte of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into an 8-bit shift register within the DS1280. The byte of data is then transferred from the shift register to the 3-wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first. A burst write uses the same 19-bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3-wire bus into an 8-bit shift register within the DS1280 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock. Burst reads and writes will continue on a byte-by-byte basis, automatically incrementing the selected address by one location for each successive byte.

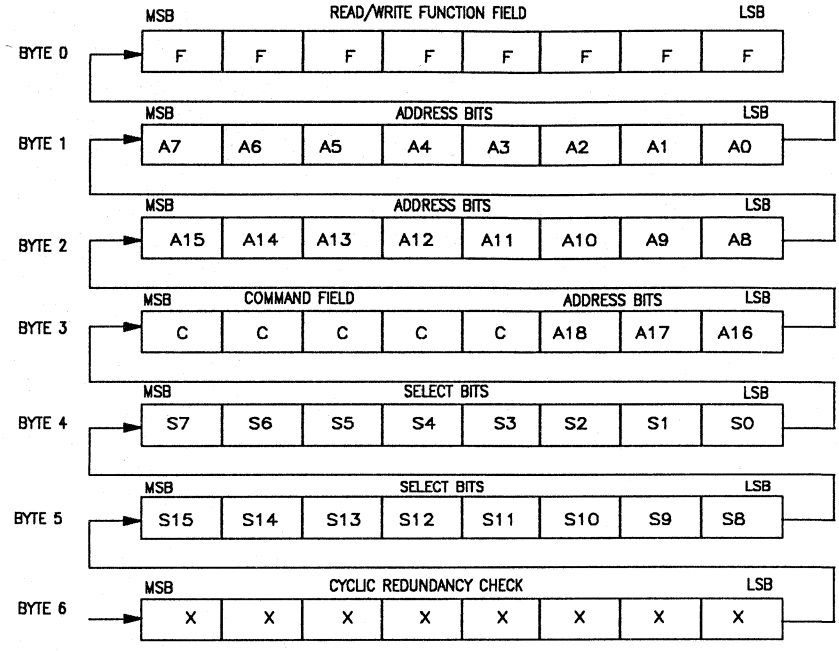
PROTOCOL COMMANDS Table 1

1. Burst read
2. Burst write
3. Read protocol select bits
4. Write protocol select bits
5. Burst read masking portions of the protocol select bits
6. Read CRC register
7. Set the address arbitration byte location
8. Poll arbitration byte for status and control

CONTROL FIELD Table 2

00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 7FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits

PROTOCOL Figure 2



Termination of a current operation will occur at any time when RST\ is taken low. If a byte of data has been loaded into the shift register, a write cycle is allowed to finish, so corrupted data is not written into the RAM. If a full byte of data has not been loaded into the shift register when RST\ goes low, no writing occurs. Reads can be terminated at any point since there is no potential for corruption of data. The read CRC command provides a method for checking the integrity of data sent over the 3-wire bus. The CRC byte resides in the last byte (byte 6) of the protocol. The 8-bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM.

After a burst read or write has finished and RST\ has gone low, the final value of the CRC is stored in the DS1280. If a read CRC register command is issued, the stored CRC value is driven onto the DQ line by the first eight clock cycles after the protocol is received. The CRC value generated by the DS1280 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3-wire bus. If it does not, data has been corrupted and a retransmission should occur. It should be noted that the CRC for the previous transaction can only be obtained if a read CRC command is issued immediately after RST\ goes low to reset the DS1280, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever RST\ goes low again, destroying the CRC value of interest. Generation of the CRC byte by the external unit on the 3-wire bus will be covered later in this data sheet.

In any 2-port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the DS1280 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports.

Two commands are used by the 3-wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel bytewide port, a command is added to move the arbitration byte to either address location "00000" or address location "7FFFF." When setting the arbitration byte address location, the correct read/write field and command field must be entered along with all zeroes or all ones in the address field. It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the DS1280. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some read/write restriction. However, the serial port can still address the actual RAM location at either 00000 or 7FFFF in addition to accessing the arbitration byte.

The second command used by the 3-wire serial port provides for polling of the arbitration byte to determine the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port that the serial port is taking over the RAM. The second command protocol allows the serial port to do a compressed read-write-read operation that causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. The 24 cycles occur by entering the 56-bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111) and the correct command field.

Three other commands are used to set the select bits in the protocol. Once the select bits are set to a binary value they must be matched exactly when protocol is sent or further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore,multiple DS1280s can be connected on the same serial bus and only the appropriate device will respond. To write the select bits, a write function in the read/write field is required along with the appropriate command in the command field.

To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user to have multiple DS1280s in use and uniquely identify each. A read can occur successfully without knowing the select bits but a write cannot occur without matching the current select field.

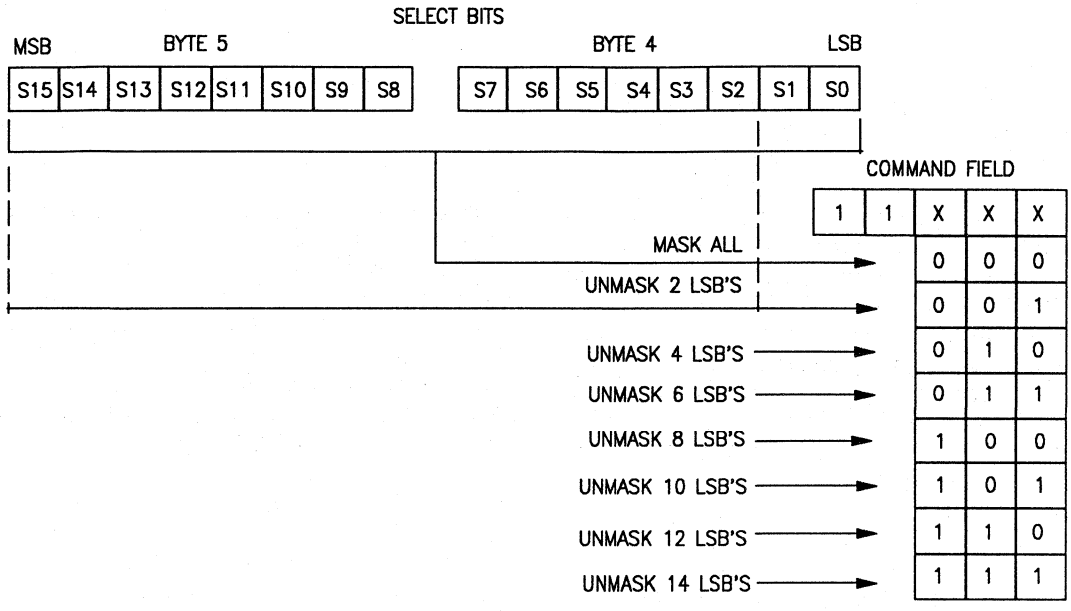
A third command masking specific select bits provides a means for determining the identity of a specific DS1280 when more than one is used. A read in the read/write field and a "11000" in the command field will execute a mask read that ignores all select bits to determine the presence of one or more DS1280s. With the detection of at least one device, a search can begin by masking all but a single pair of DS1280 select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSBs of byte 4 of the select bits (see Figure 3). With these two select bits unmasked, only an exact match of four possible combinations of these two select bits will allow access through the 3-wire port to RAM. The combinations are 00, 01, 10, and 11. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits.

Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. Repetition of unmasking select bit pairs will yield an exact match of 65,536 possible DS1280s in no more than 32 attempts.

ARBITRATION

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3- wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 7FFFF as determined by the protocol input from the 3-wire serial

SELECT BITS MASK Figure 3



port. The arbitration byte has special restrictions and disciplines so that the 3-wire serial bus and the bytewide parallel bus are never in contention for RAM access. This byte is shown in Figure 4.

As defined, the 3-wire serial port can read the whole byte but can only write bits S2-S0. The byte wide parallel port can read the whole byte but can only write bits B1-B0. An internal counter controls bits C2-C0 that cannot be written by either port. Arbitration is accomplished when the status bits are read and written by the respective ports. If the 3-wire serial port wants to access RAM, the arbitration byte should be polled by the serial port until bit B1 equals zero. If B1 equals zero, the 3-wire serial port should then write a one into bit S2. After the write of bit S2, the 3-wire serial port should then read the arbitration byte to confirm that B1=0 and S2=1. This operation must be executed with the protocol for the compressed read/write/read sequence which minimizes overhead.

The 3-wire serial port should always abort any attempt to access RAM if B1 equals one. When the 3-wire serial port completes any transfer of data to or from RAM, bit S2 should be written back to zero so that the bytewide parallel port will know that the 3-wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit B1. A read cycle verifying that S2 equals zero and B1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the B1 bit to zero, signaling the 3-wire serial port that the RAM is not in use.

The bits B0, S1, and S0 can be defined by the user to pass additional arbitration information, making possible more elaborate handshaking schemes between the two ports. Some typical uses for these bits could be an indication that a

ARBITRATION BYTE Figure 4

MSB LSB

P1	P0	S2	S1	S0	C2	C1	C0
PARALLEL BUS STATUS BITS	NOT USED	SERIAL PORT STATUS BITS	NOT USED	NOT USED	COUNT BIT	COUNT BIT	COUNT BIT

port desires access to RAM or the amount of RAM written. Another method of arbitration between the 3-wire serial port and the bytewide parallel bus is the use of the count bits C0-C2. The 3-wire port reads or writes from RAM only once every eight clock cycles. This action occurs when the internal byte counter transitions from a "111" state to a "000" state. The access occurs regardless of the arbitration byte status bits. C0-C2 are updated as the internal serial bit counter is incremented. The bytewide port can execute reads or writes depending on the status of C0-C2. These bits indicate the number of bits the 3-wire serial port has loaded and, therefore, indicate when a read or write will occur from the 3-wire port.

Since the 3-wire port always reads or writes at the ends of a byte (C0-C2 = 1) the bytewide parallel bus should never access RAM if the count bits read all ones. The bytewide parallel port can determine the minimum time left before the 3-wire serial port will access the memory from the count bits and the minimum clock cycle applied to the 3-wire clock input. Essentially the 3-wire serial port is given priority on access to RAM and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3-wire serial port.

CRC GENERATION

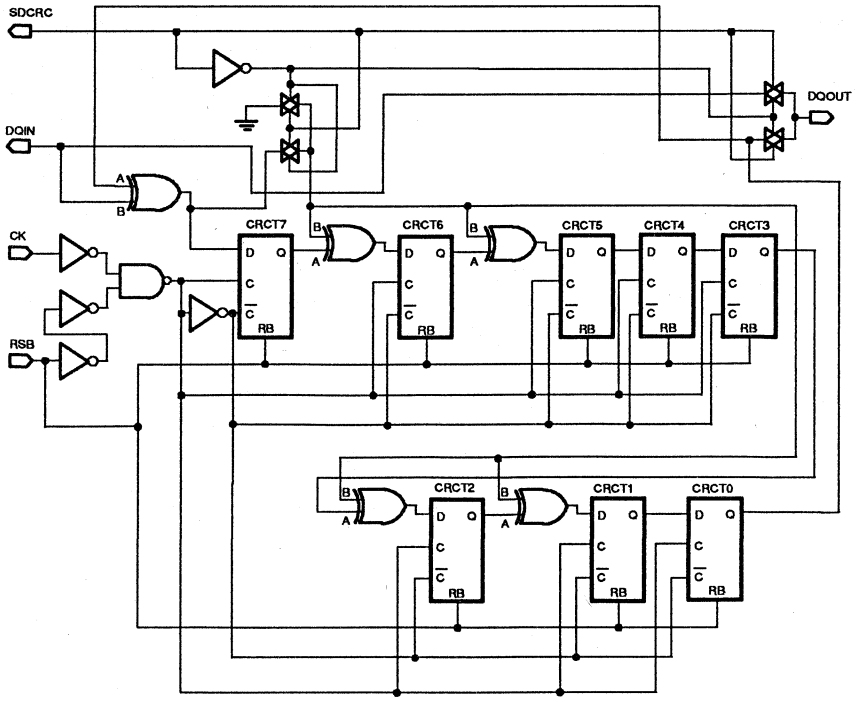
The logic involved in CRC generation is shown in Figure 5. It is comprised of an 8-bit shift register, four exclusive OR gates, and two sets of transmission gates. The transmission gates serve to divert data from DQIN to the CRC generator while each byte is being assembled and, at the same time, output data to the output (DQ OUT). When input select CRC (SDCRC) is driven to an active level (high), data is output at DQOUT from the CRC generator using the clock input (CK) in the same manner as described earlier for operation of the 3-wire serial bus.

The reset signal (RSB) must be high while the CRC generator is being used, as an inactive state will disable the 8-bit shift register. This signal is the same as the reset described for the 3-wire serial bus. A CRC generator for serial port communications can be constructed as described above to satisfy the DS1280 CRC requirements. However, another approach is to generate the CRC using software. An example of how this is accomplished using assembly language follows. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure DO CRC given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and DO CRC is called to update the CRC. After all the data has been passed to DO CRC, the variable CRC will contain the result.

CRC GENERATION LOGIC Table 3

```
DO_CRC:
        PUSH    ACC             ; Save the Accumulator
        PUSH    B               ; Save the B register
        PUSH    ACC             ; Save bits to be shifted
        MOV     B,      #8      ; Set to shift eight bits
CRC_LOOP:
        XRL     A,      CRC     ; Calculate DQIN xor CRCTO
        RRC     A               ; Move it to the last
        MOV     A,      CRC     ; Get the last CRC value
        JNC     ZERO            ; Skip if DQIN xor CRCTO = 0
        XRL     A,      0CCH    ; Update the CRC value
ZERO:
        RRC     A               ; Position the new CRC
        MOV     CRC,    A       : Store the new CRC
        POP     ACC             : Get the remaining bits
        RR      A               ; Position next bit in LSB
        PUSH    ACC             ; Save the remaining bits
        DJNZ    B,      CRC_LOOP ; Repeat for eight bits
        POP     ACC             ; Clean up the stack
        POP     B               ; Restore the B register
        POP     ACC             ; Restore the Accumulator
        RET                     ; Return
```

CRC GENERATION Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to+125°C
Soldering Temperature	260°C for 10 sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A=0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Supply	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}+0.3V	V	
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(t_A=0°C to 70°C V_{CC}=+5V+/-10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		+1	uA	9
Output Leakage	I_{LO}			1	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}	+2			mA	
Supply Current	I_{CC1}			15	mA	2
Supply Current	I_{CC2}			50	mA	3

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=5V+/- 10%, 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	4
Data to CLK Hold	t_{CDH}	40			ns	4
Data to CLK Delay	t_{CDD}			125	ns	4,5,6
CLK Low Time	t_{CL}	500			ns	4
CLK High Time	t_{CH}	500			ns	4
CLK Frequency	f_{CLK}	D.C.		1	MHz	4,10
CLK Rise & Fall Time	t_R t_F			100	ns	
RST\ to CLK Setup	t_{CC}	1			us	4
CLK to RST\ Hold	t_{CCH}	40			ns	4
RST\ Inactive Time	t_{CWH}	125			ns	4
RST\ to D/Q High Z	t_{CDZ}			50	ns	4
Serial Port Active	t_{DA}			25	ns	4,6
Serial Port Inactive	t_{DI}			25	ns	4,6
Parallel Port Propagation	t_{PD}		12	20	ns	4,6,8

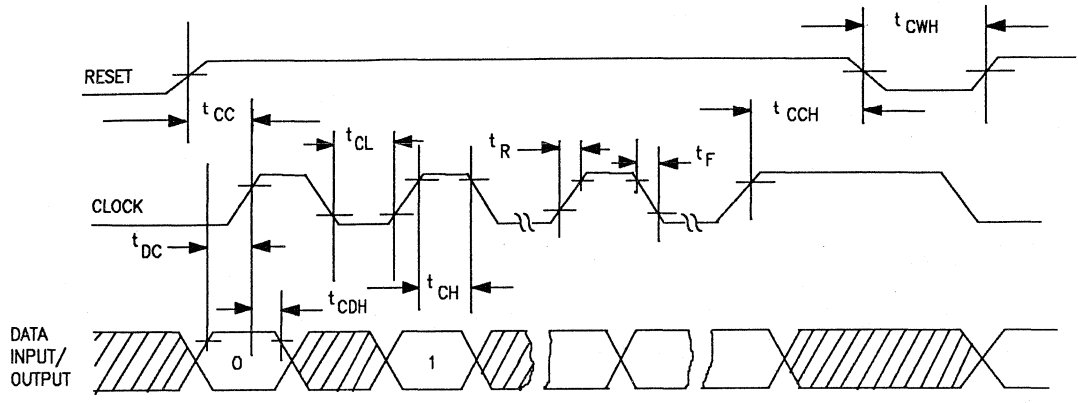
CAPACITANCE

PARAMETER	SYMBOL	COND.	TYP.	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C5		10	pF	
Output Capacitance	C_{OUT}	t_A=25°C7		15	pF	

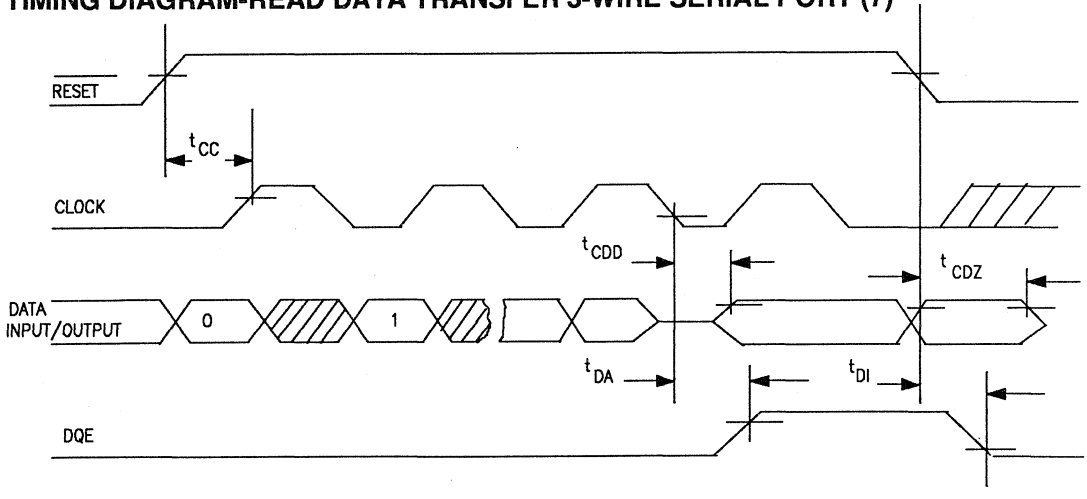
NOTES:

1. All voltages are referenced to ground.
2. I_{CC1} is measured with all outputs open and both the 3-wire serial port or the bytewide parallel port inactive.
3. I_{CC2} is measured with all outputs open.
4. Measured at V_{IH} = 2.0 V or V_{IL} = 0.8 V and 10ns maximum rise and fall time.
5. Measured at V_{OH}= 2.4 V and V_{OL} = 0.4V.
6. Measured with a load capacitance of 50 pF.
7. The 3-wire serial port will correctly read and write any static RAM with an effective access time of 200ns.
8. Propagation delay is the same for data going either way on the bytewide parallel bus.
9. Pins A0B through A18B, RST\, DQ, CEB\ have pulldown resistors which will leak approximately 50 uA.
10. Arbitration byte must be accessed at a maximum clock frequency of 500 KHz with a symmetrical waveform.

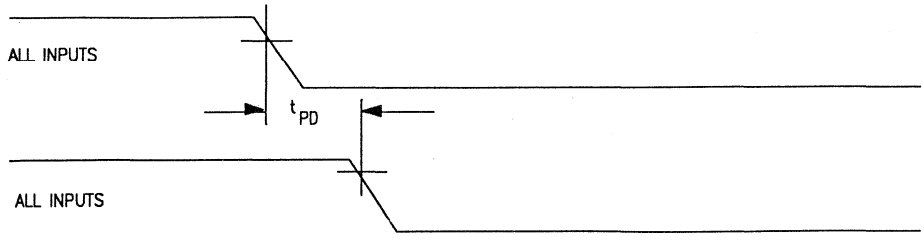
TIMING DIAGRAM-WRITE DATA TRANSFER 3-WIRE SERIAL PORT(7)



TIMING DIAGRAM-READ DATA TRANSFER 3-WIRE SERIAL PORT (7)

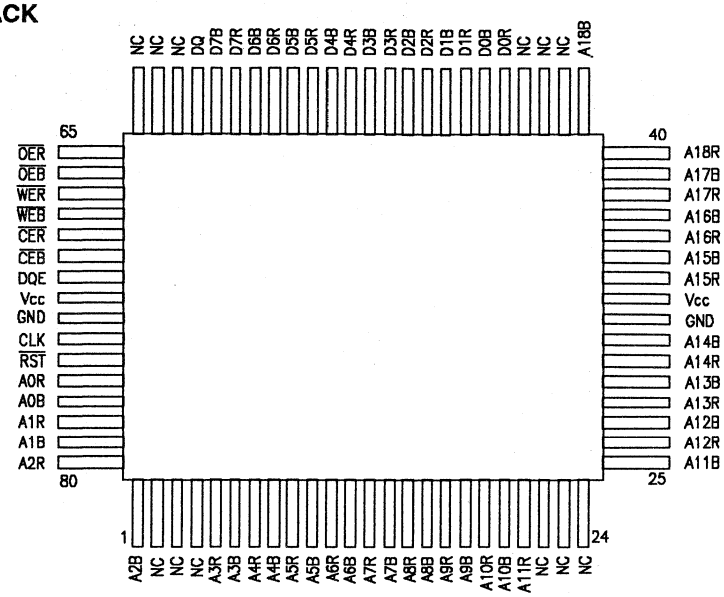


PROPAGATION DELAY-DATA TRANSFER: BYTEWIDE PARALLEL DATA BUS (8)

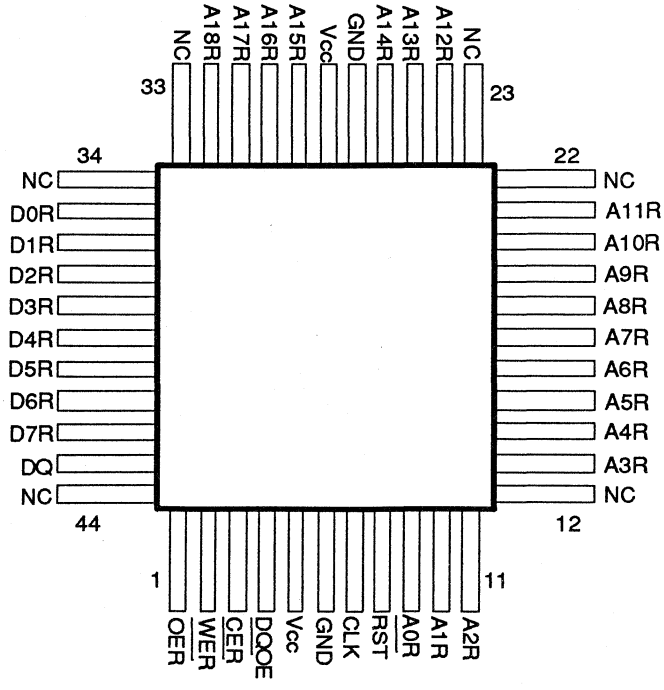


PIN DESCRIPTIONS

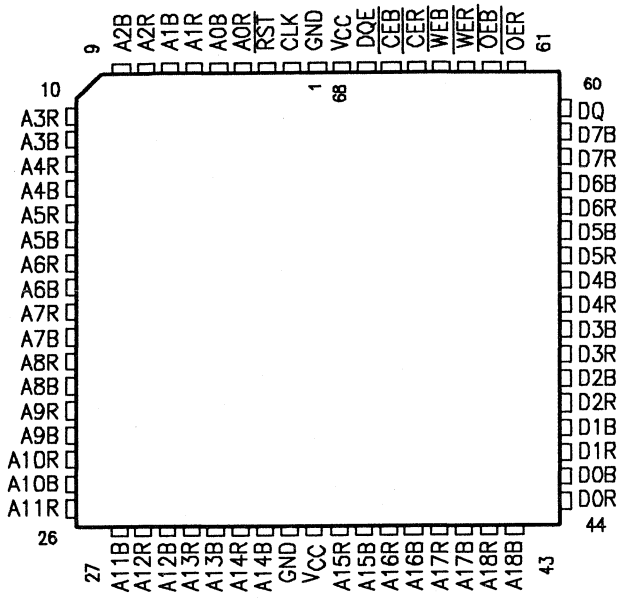
DS1280FP-80
80-PIN FLAT PACK



DS1280FP-44
44-PIN FLAT PACK



DS1280Q-68
68-PIN PLCC



DALLAS SEMICONDUCTOR

DS1281
1- to 3-Wire Converter Chip

FEATURES

- Adapts a 3-wire device to a 1-wire touch interface
- Contains a unique factory lasered 48-bit serial number
- Contains an 8-bit type identifier code to simplify protocol identification
- Provides arbitration mechanisms for dual port operation
- CMOS circuitry design for battery-operated applications
- Space saving 16-pin SOIC package

PIN NAMES (\ Denotes Condition Low)

V_{CC}	+ 5 Supply
RSTI\	RSTI\ Input
DQI	DQ Input
CLKI	CLK Input
GND	Ground
RSTO\	RSTO\Output
DQO	DQ Output
CLKO	CLK Output
1-Wire	Touch Interface
NC	No Connection

DESCRIPTION

The DS1281 1-to 3-Wire Converter Chip is used to connect a 3-wire (data, clock and RST\) serial device to a 1-wire touch interface. Each DS1281 is manufactured with a unique 48-bit serial number which can be read through the 1-wire touch interface. This serial number includes an 8-bit type identifier code which can be read through the 1-wire interface. An internal state machine provides an arbitration mechanism for operation with an existing 3-wire serial port on a first-come, first-served basis. Low-power CMOS circuitry design allows operation of the part in battery backup and battery operate environments.

OPERATION

When the 1-wire touch interface is used, all communications to and from the DS1281 are accomplished via a single interface lead. Data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

WRITE TIME SLOTS

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds and a maximum of 120 microseconds in duration. There is a minimum of a 1 microsecond access recovery high time between time slots.

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot (See Figure 1).

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot (See Figure 2).

READ TIME SLOTS

The host generates read time slots when data is to be read from the 1-wire interface. A read time slot is initiated when the host pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of one microsecond and a maximum of 15 microseconds. This maximum time of 15 microseconds includes the time required for the data line to pull up to a high level after it is released. The state of the 1-wire data line must be read by the host within 15 microseconds after the start of the read time slot. After this time, the state of the data is not guaranteed (See Figure 3). All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond valid access recovery time between individual read time slots.

1-WIRE PROTOCOL

The 1-wire protocol can be viewed as having three distinct layers. These layers are the presence detect layer, the reset layer, and the command layer.

PRESENCE DETECT

The presence detect layer is used to signal to a host device that a new device has been attached to the 1-wire port. The 1-wire port from the host remains at a logic high level during quiescent times between read and write time slots. This high time must be present for a minimum of 15 microseconds before the new device can assert a presence detect signal. The presence detect signal will be a logic low level asserted by the newly attached device which remains low for a maximum of 240 microseconds and then is released (See Figure 4). This low logic level can be detected by the host and used as an interrupt condition for the host processor.

DEVICE RESET

The reset layer is used to reset the attached 1-wire devices. This allows the host to place the 1-wire device or devices into a known state at any time. The reset signal consists of a logic low level asserted by the host for a minimum of 480 microseconds. Afterwards the host must release the 1-wire signal line and allow it to rise to a logic high level. This high logic level must be maintained by the host for a minimum of 480 microseconds before any data can be exchanged. During this logic high time, any device present on the 1-wire signal line will assert its presence detect waveform (See Figure 5).

1-WIRE COMMANDS

There are four commands which can be issued by the host on the 1-wire port (LSB first). These are:

1) [33 hex] read ROM data
2) [55 hex] match ROM data
3) [F0 hex] search ROM data
4) [CC hex] pass through mode

READ ROM DATA

Upon recognition of the command word [33 hex], the DS1281 is ready to respond to the next eight read time slots with the type identifier number. This number is a hexadecimal 03 and is unique to the DS1281 part.

After receipt by the host of the type identifier number, the DS1281 is ready to output the unique 48-bit serial number contained within the device. The host must issue 48 read time slots to retrieve this number. Following the 48-bit serial number is an 8-bit Cyclic Redundancy Check (CRC) value. This CRC value has been calculated over the type identifier and serial number, 56 bits total, using the following polynomial:

$p_x = x^2 + x^3$, assuming x^0 => LSB

This calculated value is lasered into the part at the time of manufacture. To read the CRC value, the host must issue eight additional read time slots.

MATCH ROM DATA

The match ROM data command is used as a device select when multiple 1-wire devices are connected to a single bus. This command allows the host to address any one of the multiple 1-wire devices on an individual basis. To do a match ROM data command, the host must issue the command (55 hexadecimal) to the device with eight write time slots. Following the command byte, the host must write the desired device's type identifier, serial number, and CRC byte. If all of these values match the data stored internally in the ROM, the DS1281 will generate output three wire signals to access a three wire part. If any of the bit values transmitted by the host fail to match the ROM data pattern, the access will be terminated. To return from a pattern fail condition, the host must issue a reset command.

| Type ID | 48-bit Serial Number | CRC |

transmit ---------->

SEARCH ROM DATA

The search ROM data command (F0 hexadecimal) allows the host 1-wire device to poll efficiently to determine the unique ROM address of all devices on the 1-wire bus. In this mode, each of the bits of the ROM data requires three time slots on the 1-wire bus. The first two time slots are read time slots in which the DS1281 transmits back to the host the value of the ROM bit followed by its complement. The third time slot is a write time slot in which the host supplies its desired value for the ROM bit. The DS1281 then compares the desired value with the actual ROM bit. If the bits agree, the DS1281 increments its internal counter to point to the next bit in the ROM data and then repeats the same set of three time slots for the next bit. If all bits of the ROM are matched correctly, the host can access the external 3-wire part with the standard command structure for the part.

EXAMPLE OF A ROM SEARCH

The following example of the ROM search process assumes four different DS1281's are connected to the same 1-wire bus. The ROM data of the four DS1281's begins as shown:

ROM0- 00110101...
ROM1- 10101010...

ROM4- 00010001...

The search processes are as follows:

1) The host begins by resetting all devices present on the 1-wire bus. After this, the host will attempt to read the type identifier, serial number, and CRC value for the part.

2) The host will then issue the SEARCH ROM DATA command on the 1-wire bus by writing [F0 hexadecimal].

3) The host executes two read time slots and receives two zero bits. This indicates that both one bits and zero bits exist as the first bit of the devices on the bus.

4) The host supplies a write zero time slot as the third time slot. This deselects ROM1 and ROM2 for the remainder of this search pass, leaving only ROM0 and ROM3 connected to the 1-wire bus.

5) The host executes two read time slots and receives a zero bit followed by a one bit. This indicates that all devices still coupled to the 1-wire bus have zeros as their second ROM data bit.

6) The host supplies a write zero time slot as the third time slot to keep ROM0 and ROM3 coupled.

7) The host executes two read time slots and receives two zero bits. This indicates that both one bits and zero bits exist as the third bit of the ROM data of the attached devices.

8) The host supplies a write zero time slot as the third time slot. This deselects ROM0 leaving ROM3 as the only device connected.

9) The host reads the remainder of the ROM data bits for ROM3 and continues to access the part if desired. This completes the first ROM search pass and has identified one part uniquely on the 1-wire bus.

At this point, the host repeats the process described above to determine the addresses of the remaining devices on the 1-wire bus by repeating steps 1 through 7.

Note should be made of the following points to the example described previously:

The host learns the unique address (ROM data pattern) of one 1-wire device on each ROM SEARCH operation. The time required to derive the part's unique address is:

960 us + [8+(3*64)] * 60us = 12.96 milliseconds

The host is therefore capable of identifying more than 75 different 1-wire devices per second.

Additionally, the data obtained from the two read time slots of each set of three time slots have the following interpretations:

00 - there are still devices attached which have conflicting bits in this position.

01 - all devices still coupled have a zero bit in this bit position.

10 - all devices still coupled have a one bit in this bit position.

11 - there are no devices attached to the 1-wire bus. (This is an error condition)

PASS-THRU MODE

The pass-thru command is used to allow a host connected to the 1-wire bus to quickly gain access to the 3-wire device connected to the DS1281. It is entered by issuing 8 write time slots of [CC hexadecimal] to the DS1281. This command bypasses the serial number internal to the DS1281 and allows the host to directly

control the attached 3-wire device.

3-WIRE BUS

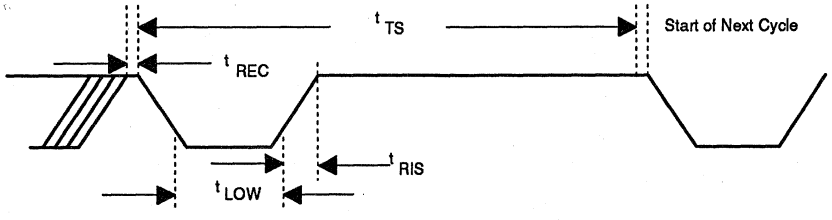
The 3-wire bus is comprised of three signals. These are the RST\ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the RST\ input high. The RST\ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if the RST\ is low and the DQ pin goes to a high impedance state. When data transfers to the DS1281 are terminated by the RST\ signal going low, the transition of the RST\ going low must occur during a high level of the CLK signal. Failure to insure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfer is illustrated in Figures 6 and 7 for normal modes of operation.

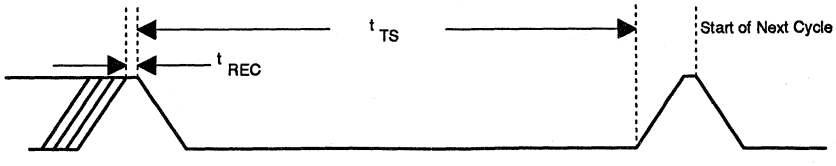
1-WIRE/3-WIRE ARBITRATION

The DS1281 can utilize both the 1-wire and the 3-wire busses simultaneously. Neither input bus has priority over the other. Instead, if both inputs are being used, the signal arriving first will take precedence. More simply, if the 1-wire interface becomes active before the 3-wire interface, all communications will take place on the 1-wire bus. The 3-wire bus will be ignored in this case. The same condition occurs for the 1-wire interface if the 3-wire interface becomes active first.

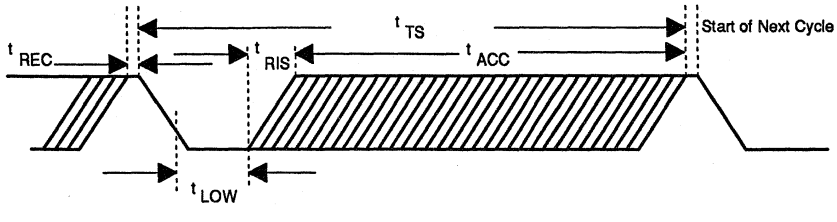
WRITE ONE TIME SLOT Figure 1



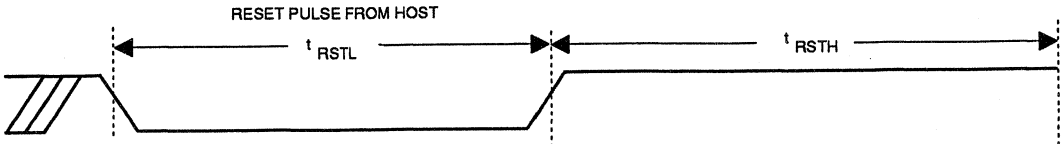
WRITE ZERO TIME SLOT Figure 2



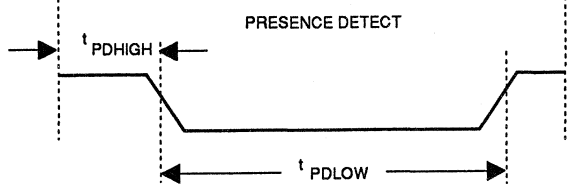
READ TIME SLOTS Figure 3



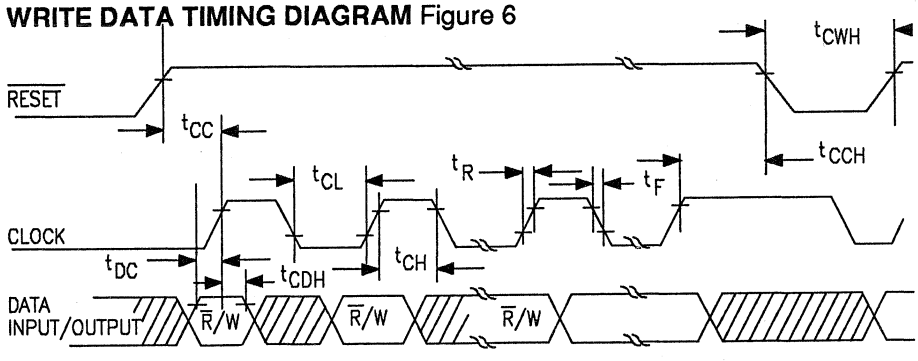
RESET PULSE Figure 4



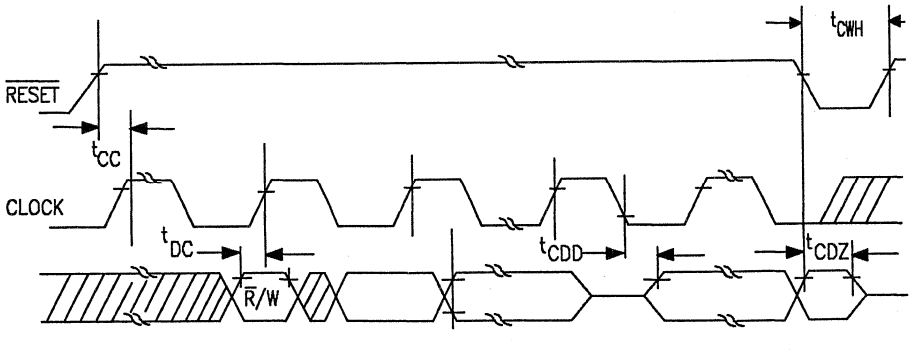
PRESENCE DETECT Figure 5



WRITE DATA TIMING DIAGRAM Figure 6



READ DATA TIMING DIAGRAM Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0			V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
RESET\ Logic 1					V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}			+500	uA	
Output Leakage	I_{LO}			+500	uA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ 0.4V	I_{OL}			+2	mA	
RST\ Input Resistance	Z_{RST}	10		40	K ohm	
D/Q Input Resistance	Z_{DQ}	10		40	K ohm	
CLK Input Resis.	Z_{CLK}	10		40	K ohm	
Active Current	I_{CC1}			1	mA	5
Standby Current	I_{CC2}			200	nA	5

CAPACITANCE

(t_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4,7
CLK Low Time	t_{CL}	125			ns	2
CLK High Time	t_{CH}	125			ns	2
CLK Frequency	t_{CLK}	DC		4.0	MHz	2
CLK Rise & Fall	t_R,t_F			50	ns	2
RST\ to CLK Setup	t_{CC}	1			us	2
CLK to RST\ Hold	t_{CCH}	40			ns	2
RST\ Inactive Time	t_{CWH}	125			ns	2
RST\ to I/O High Z	t_{CDZ}			50	ns	2

AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(0°C to 70°C, V_{CC} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{TS}	60		120	uS	
Recovery Time	t_{REC}	1			uS	
Low Time	t_{LOW}	1		14	uS	
Reset Time High	t_{RSTH}	480			uS	
Reset Time Low	t_{RSTL}	480			uS	
Presence Detect	t_{PDHIGH}	15		60	uS	
Presence Detect	t_{PDLOW}	60		240	uS	
Rise Time	t_{RIS}			1	uS	6

NOTES:

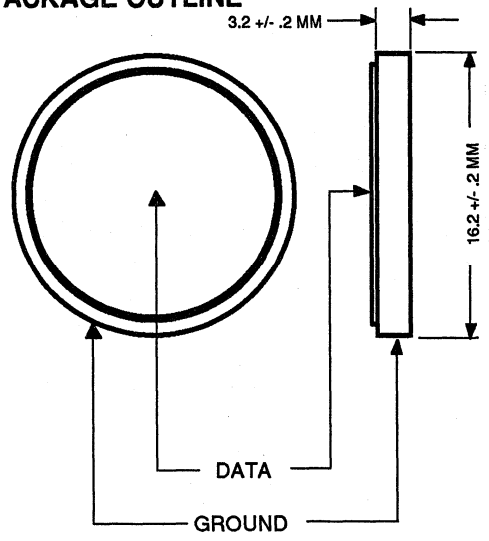
1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10 ns maximum rise and fall time.
3. V_{OH} = 2.4V and V_{OL} = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. Rise time must take into account capacitance and user pullup value.
7. Does not include access time of external 3-wire part.

DALLAS SEMICONDUCTOR

DS199x
Touch Devices

FEATURES
- Identification by touch
- Nonvolatile internal memory chip
- Reads or writes in less than 20 ms while affixed to an object
- Low-cost and reusable
- Chip-based identifier communicates to host reader via One-Wire™ protocol
- Optional adhesive backing for attachment to an object
- Coin-shaped for easy handling and insertion
- Round shape for self-aligning touch contact
- Durable stainless steel case
- Data signal surface and ground rim simplify contact alignment
- Operating temperature range -20° to +50° C
- Applications include identification, workpiece monitoring, manufacturing notations, tool management, inventory control, record keeping, parts tracking, security and access control

PACKAGE OUTLINE



CONTACTS

Rim	Ground
Surface	Data

ORDERING INFORMATION

1990	Touch Serial Number
1991/1991L*	Touch MultiKey
1992/1992L*	Touch Memory™ (1Kx1)

* L denotes 5 year data retention; standard is 2 years.

DESCRIPTION

The DS199x Touch Device is a nonvolatile memory in a coin-shaped package that can be read or written with a simple touch using the One-Wire™ protocol. The equivalent of silicon self-stick notes, Touch Devices can be affixed to an object or carried by a person for identification. They are low-cost and reusable. Signaling necessary for reading or writing is reduced to just one data conductor plus ground and the familiar round coin shape ensures easy handling.

OVERVIEW

All communications to and from Touch Devices are accomplished via a single interface lead. Data contained within a Touch Device is accessed through the use of time slots using the One-Wire™ protocol. No markings are provided on the Touch Device container. Instead, each device family has a specific identification number lasered into the device which is read by the user to identify the part type.

For specific information on the function of each device, refer to Table 1.

TABLE 1

Touch Device	Description	Related Chip
DS1990 Touch Serial Number	Unique 48-bit serial number, lasered-in at the factory.	DS2400 Silicon Serial Number
DS1991 Touch MultiKey	3 password-protected 384-bit partitions, 1 512-bit scratchpad memory.	DS1205 MultiKey
DS1992 Touch Memory	1Kx1 read/write NV SRAM	

PACKAGING OPTIONS

DS199x Touch Devices can be ordered with adhesive backings or mounted on the DS9093 Touch Device Mount. Contact the Marketing Department for availability and minimum order requirements. DS199x Touch Devices are shipped standard without adhesive material.

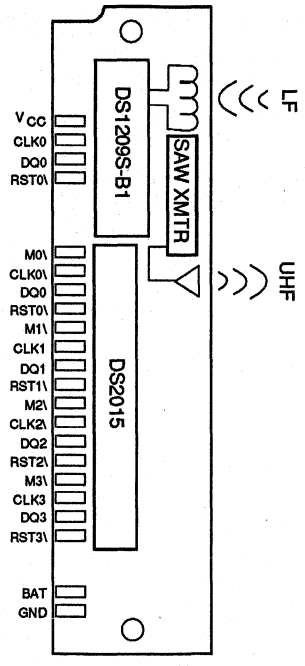
DALLAS SEMICONDUCTOR

DS2267
Wireless Transceiver Stik

FEATURES

- Wireless transmitter/receiver subsystem with 3-wire serial data port
- Two-way, half-duplex RF link has range in excess of 5 feet
- Addressability allows up to 65,536 devices within the same proximity range
- Transmit link uses 303.875 MHz and receive link uses 133.3 KHz
- Onboard DS2015 Quad Port Serial RAM enables asynchronous microprocessor interface
- Greater than 1000 bits per second data transfer rate
- Snaps into a 40-pin parallel or perpendicular mount connector
- Unlimited operation under Federal Communications Commission (FCC) Rules and Regulations, Part 15, Subpart C

PACKAGE DESCRIPTION



40-Pin SIP Stik

This device has not been approved by the Federal Communications Commission. This device is not, and may not be, offered for sale or lease, or sold or leased until the approval of the FCC has been obtained.

DESCRIPTION

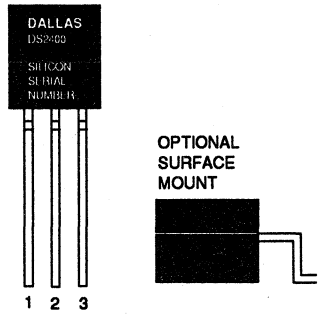
The DS2267 Wireless Transceiver Stik provides an asynchronous interrupt-driven port which couples a host microprocessor to an RF wireless data link. The Wireless Transceiver Stik has a SAW-stablized UHF transmitter and an LF receiver onboard. These provide for wireless data transfers between a host system and a Wireless Transceiver Stik via a DS6068A RF Communicator. Additionally, the Wireless Transceiver Stik has a DS2015 Quad Port Serial RAM memory which can be used as a buffer device to the user-supplied microprocessor. Data transfer rates of greater than 1000 bits per second can be supported between the Wireless Transceiver Stik and a DS6068A RF Communicator. Data is received on a frequency of 133.3 KHz and transmited back to the RF Communicator at 303.875 MHz. Data communication at distances of over 5 feet is achieved through the use of a SAW-stabilized transmitter. Up to 65,536 Wireless Transceiver Stik-equipped devices can be individually addressed within the same wireless field. For more specific information on the functionality of the DS2267 Wireless Transceiver Stik, please see the DS2015 Quad Port Serial RAM and DS1209S-B1 Wireless to 3-Wire Converter Chip data sheets.

DALLAS SEMICONDUCTOR

DS2400
Silicon Serial Number

FEATURES
- Unique 48-bit silicon serial number gives 10^{14} combinations
- Factory lasered and tested, no two parts alike
- 8-bit cyclic redundancy check ensures error-free reading
- 8-bit model number references DS2400 communications requirements to system
- Presence detect indicates to the system when first contact is made
- Low-cost TO-92 package and optional surface mount option
- Reduces control, address, and data to a single pin
- Zero standby power required
- Directly connects to one port pin for microprocessor interface
- Pulse width measurement determines "1s" or "0s"
- Power derived from data line

PIN DESCRIPTION



PIN NAMES
Pin 1 Ground
Pin 2 Data (DQ)
Pin 3 No Connect

DESCRIPTION
The DS2400 Silicon Serial Number is a device which contains an 8-bit model number, a unique 48-bit serial number, and an 8-bit cyclic redundancy check value embedded in silicon. Signaling necessary for reading or writing is reduced to just one interface lead. The familiar TO-92 package provides a small, low-cost enclosure. Power for reading and writing is derived from the data line itself with no need for an external power source.

OPERATION

All communication to and from the DS2400 Silicon Serial Number is accomplished via a single interface lead. Data contained within the DS2400 is accessed through the use of time slots and a 1-wire protocol. Power to the part is derived from the high going pulse at the beginning of a write or read time slot.

WRITE TIME SLOTS

A write time slot is initiated when the system pulls the data line from a high logic level to a low logic level. There are two types of write time slots: write one and write zero. All write slots must be a minimum of 60 microseconds and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond recovery time between individual write cycles.

For the system to generate a write one time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot (see Figure 1).

For the system to generate a write zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot (see Figure 2).

READ TIME SLOTS

The system generates read time slots when data is to be read from the DS2400. A read time slot is initiated when the system pulls the data line from a logic high level to a logic low level. The data line must remain at a low logic level for a minimum of 1 microsecond and a maximum of 15 microseconds. This maximum time of 15 microseconds includes the time required for the data line to pull up to a high level after it is released. The state of the DS2400 data must be read by the system within 15 microseconds after the start of the read time slot. After this time, the state of the data is not guaranteed (see Figure 3). All read time slots must be a minimum of 60 microseconds in duration and a maximum of 120 microseconds in duration with a minimum of a 1 microsecond recovery time between individual read time slots.

1-WIRE PROTOCOL

To communicate with the DS2400 a specific protocol is utilized. The 1-wire protocol consists of four separate states which are used to reset the device, issue a command word, read the type identifier number, and read the unique silicon serial number and CRC byte (see Figure 4).

To initially set the DS2400 into a known state, a reset pulse must be sent to it. The reset pulse is a logic low generated by the system which must remain low for a minimum of 480 microseconds and then be followed by a 480 microsecond logic high level (see Figure 5). During this 480 microsecond high time the DS2400 will assert a presence detect signal. This signal is generated by the DS2400 and consists of a logic low level which is held for a maximum of 240 microseconds and minimum of 60 microseconds. This signal can be used to detect that a DS2400 is attached to the 1-wire interface after the issuance of a reset command.

Once the DS2400 has been set into a known state, the command word is transmitted to the DS2400 with eight write time slots. The command word for the DS2400 is a hexadecimal **0F**.

Upon recognition of the command word the DS2400 is ready to respond to the next eight read time slots with the type identifier number. This number is a hexadecimal **01**.

After receipt by the system of the type identifier number the DS2400 is ready to output the unique 48-bit serial number contained within the device. The system must issue 48 read time slots to retrieve this number. Following the 48-bit serial number is an eight-bit cyclic redundancy check value. This CRC value has been

calculated over the type identifier and serial number (56 bits) and is lasered into the part at the time of manufacture. To read the CRC value the system must issue eight read time slots. To stop reading at any time the system can issue a reset pulse.

CRC GENERATION

To validate that the transmitted data from the DS2400 has been received correctly by the system a comparison of the system-generated CRC and the received DS2400 CRC must be made. If the two CRC values match, the transmission was error-free. An example of how to generate the CRC using software is shown in Table 1. This assembly language code is written for the DS5000 Soft Microcontroller. The assembly language procedure **DO_CRC** given below calculates the cumulative CRC of all the bytes passed to it in the accumulator. Before it is used to calculate the CRC of a data stream, it should be initialized by setting the variable CRC to zero. Each byte of the data is then placed in the accumulator and **DO_CRC** is called to update the CRC variable. After all the data has been passed to **DO_CRC**, the variable CRC will contain the result.

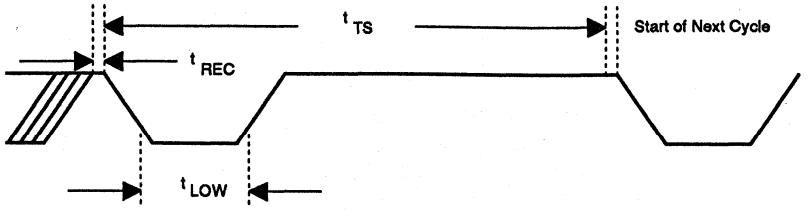
RECOMMENDED SYSTEM INTERFACE

The system must have an open drain driver with a pullup resistor of approximately 5K ohms to Vcc on the data signal line. The DS2400 has an internal open drain driver with a 500K ohm pulldown resistor to ground. The pulldown resistor holds the data input pin at ground potential when the DS2400 is not connected to a 1-wire interface (see Figure 6).

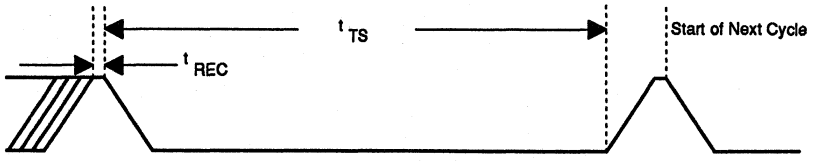
ASSEMBLY LANGUAGE PROCEDURE Table 1

```
DO_CRC:     PUSH    ACC         ; save the accumulator
            PUSH    B           ; save the B register
            PUSH    ACC         ; save bits to be shifted
            MOV     B,#8        ; set shift = 8 bits
                                ;
CRC_LOOP:   XRL     A,CRC       ; calculate CRC
            RRC     A           ; move it to the carry
            MOV     A,CRC       ; get the last CRC value
            JNC     ZERO        ; skip if data = 0
            XRL     A,#18H      ; update the CRC value
                                ;
ZERO:       RRC     A           ; position the new CRC
            MOV     CRC,A       ; store the new CRC
            POP     ACC         ; get the remaining bits
            RR      A           ; position the next bit
            PUSH    ACC         ; save the remaining bits
            DJNZ    B,CRC_LOOP  ; repeat for eight bits
            POP     ACC         ; clean up the stack
            POP     B           ; restore the B register
            POP     ACC         ; restore the accumulator
            RET
```

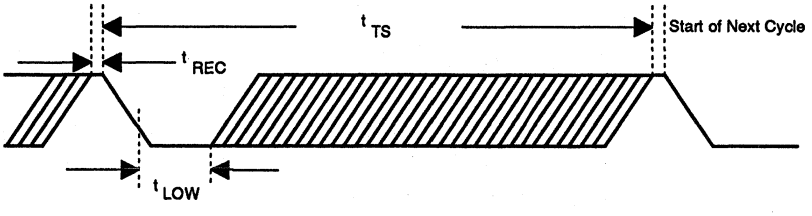
WRITE ONE TIME SLOT Figure 1



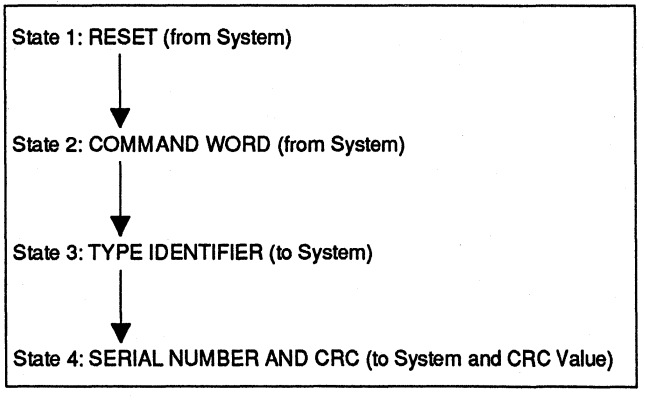
WRITE ZERO TIME SLOT Figure 2



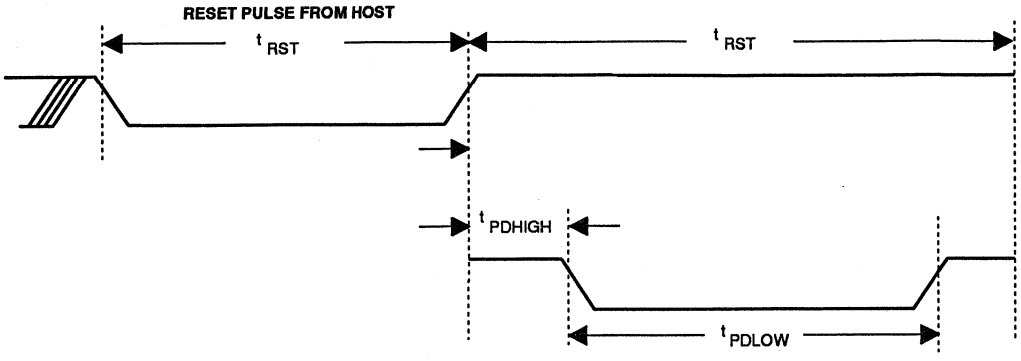
READ DATA TIME SLOTS Figure 3



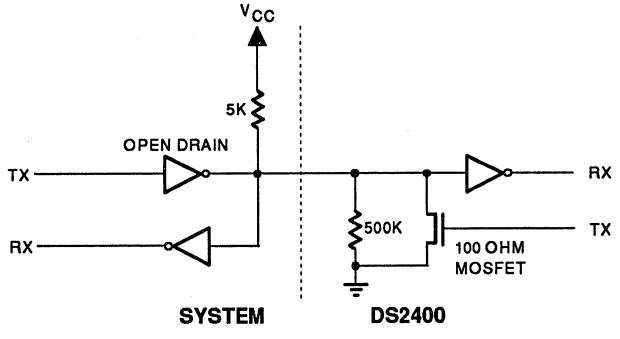
1-WIRE PROTOCOL Figure 4



RESET PULSE/PRESENCE DETECT Figure 5



RECOMMENDED SYSTEM TO DS2400 INTERFACE Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage On Data Pin Relative to Ground	-0.5 to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C To 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Data Pin	DQ	-0.5		5.5	Volts	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V +/- 10%, 0°C To 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Logic Low	V_{IL}	-0.5		0.4	Volts	1,6
Input Logic High	V_{IH}	3.0	5.0	5.5	Volts	1,6,7
Sink Current	I_L	-1.0			mA	4,6
Output Logic Low	V_{OL}			0.4	Volts	3,6
Output Logic High	V_{OH}			5.5	Volts	3,6
Input Resistance	I_R	500K				2
Operating Charge	I_{OP}			30	NC	5,6

NOTES:

1. All voltages are referenced to ground.
2. Input is pulled to ground.
3. @1 mA.
4. @ V_{OUT} = 0.4V.
5. 30 nanocoulombs per 72 time slots @ 5.0V.
6. @V_{CC} = 5.0 volts with a 5K pullup to V_{CC} and a maximum time slot of 120 us.
7. V_{IH} is a function of the external pullup resistor and the V_{CC} supply.

AC ELECTRICAL CHARACTERISTICS

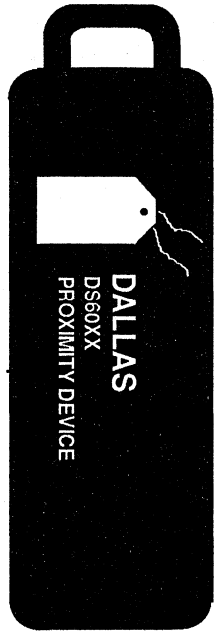
(V_{CC} = 5V +/- 10%, 0°C to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Time Slot	t_{TS}	60		120	uS	
Recovery Time Between Time Slots	t_{REC}	1			uS	
Low Time (generated for write one and read time slots)	t_{LOW}	1		15	uS	
Reset Time	t_{RST}	480			uS	
Presence Detect High Time (generated by DS2400 during presence detect cycle)	t_{PDHIGH}	15		60	uS	
Presence Detect Low Time (Generated by DS2400 during presence detect cycle)	t_{PDLOW}	60		240	uS	

DALLAS SEMICONDUCTOR

DS606xA
Proximity Device

FEATURES
- Wireless read/write nonvolatile memory
- Read and write by proximity
- Up to 65,536 proximity devices can be uniquely addressed within the same wireless proximity
- Two-way half-duplex radio link has range in excess of 5 feet
- Transmit link uses 303.875 MHz and receive link uses 133.3 KHz
- Greater than 1000 bits per second data transfer rate
- SAW-stabilized transmitter improves communications accuracy
- Compact size: can be attached to an object or carried on a key ring
- Contains a lithium energy cell for 10 years of operation
- Unlimited operation under Federal Communications Commission (FCC) Rules and Regulations, Part 15, Subpart C
- Applications include: access control, portable data record, information system security, and physical tracking of objects



ACTUAL SIZE

DESCRIPTION
Proximity devices are miniature electronic memories with a self-contained transmitter, receiver, and power supply. They provide for wireless data transfers between a host system and proximity device via a DS6068A RF Communicator. Depending upon the memory device internal to the proximity device, secure, nonsecure, and combinations of secure and nonsecure memories are available. All data transfers are accomplished via an RF full-duplex link with a transfer rate of greater than 1000 bits per second. The proximity devices receive data on a frequency of 133.3 KHz and transmit data back to the RF Communicator at 303.875 MHz. Data communication at distances of over 5 feet is achieved through the use of a SAW-stabilized transmitter. Up to 65,536 proximity devices can be individually addressed within the same operating wireless proximity. The proximity devices are designed to be rugged and durable enough to withstand normal handling with a life expectancy of over ten years. The small, lightweight construction makes the devices suitable for carrying in a pocket or direct attachment to any mobile object.

OVERVIEW

The proximity devices are designed to communicate over a two-way half-duplex RF link to a DS6068A RF Communicator. The main elements of the proximity devices are shown in the block diagram of Figure 1. As shown, the devices consist primarily of two Dallas Semiconductor chips: the DS1209S-B1 Wireless to 3-Wire Converter and an application-specific memory device. Additional elements include receiver and transmitter circuitry that allows the devices to communicate over an RF path with a remote communicator. A brief discussion of the components is given in the following section of this data sheet. However, in order to understand the operation of the proximity devices, examination of the DS1209S-B1 and data sheets of each specific memory device is recommended. In addition, knowledge of the DS6068A RF Communicator and associated software is helpful.

OPERATION

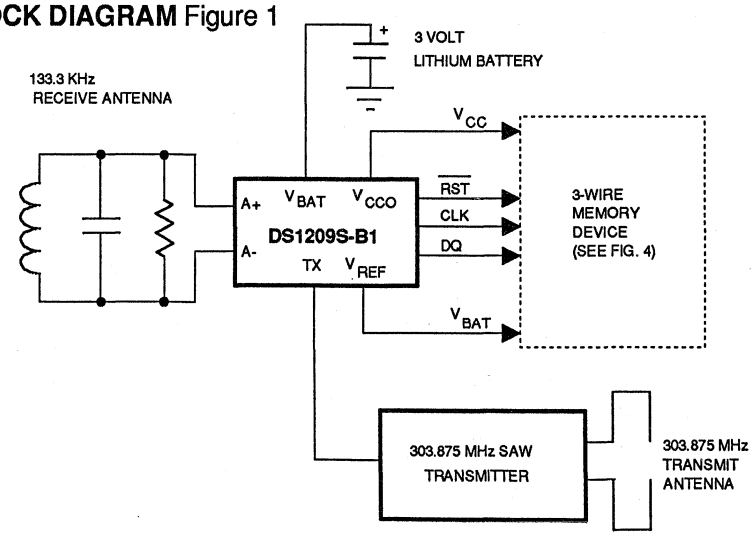
RF pulse packets transmitted by the DS6068A at a frequency of 133.3 KHz are detected by the receive antenna and arrive at the comparator input terminals of the DS1209S-B1. Signals as low as 25 mV peak-to-peak at the inputs are amplified to full level signals. These amplified 133.3 KHz signals are then sent to an internal state machine for processing and interpretation by the DS1209S-B1.

The DS1209S-B1 state machine determines what action is to be taken with the attached 3-wire device. Signals from the DS1209S-B1 are CLK, RST\, and DQ. These signals are used to either write data into or read data out of the attached memory device. A typical transaction sequence is shown in Figure 2. Figure 4 lists the memory devices utilized in the different Proximity Devices. For further information please see the referenced data sheets.

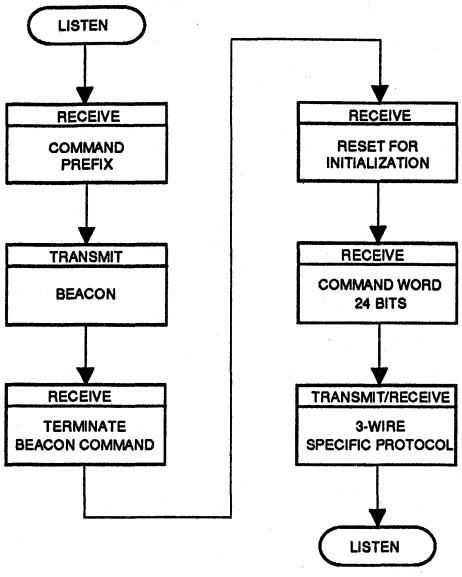
When the DS606xA is receiving data to store in a 3-wire device, the DS1209S-B1 generates the CLK, RST\, and data signals from the signals received at the comparator inputs. However, when the DS606xA is being read, data is transmitted back to the DS606xA RF Communicator via a 303.875 MHz transmitter that is controlled by the DS1209S-B1. The digital data sequence transmitted is described in the DS1209S-B1 data sheet.

The DS606xA is self-powered by a lithium energy cell designed to last for over ten years. Energy consumption and power distribution within the DS606xA is controlled by the DS1209S-B1.

DS606xA BLOCK DIAGRAM Figure 1

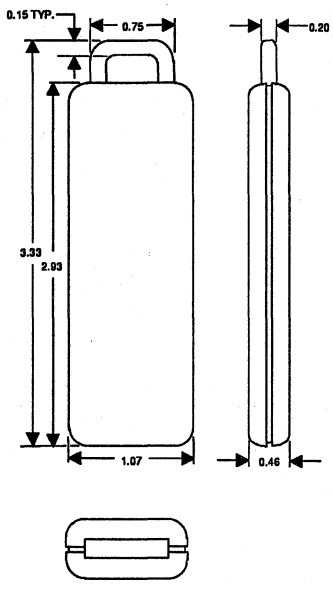


TRANSACTION SEQUENCE Figure 2

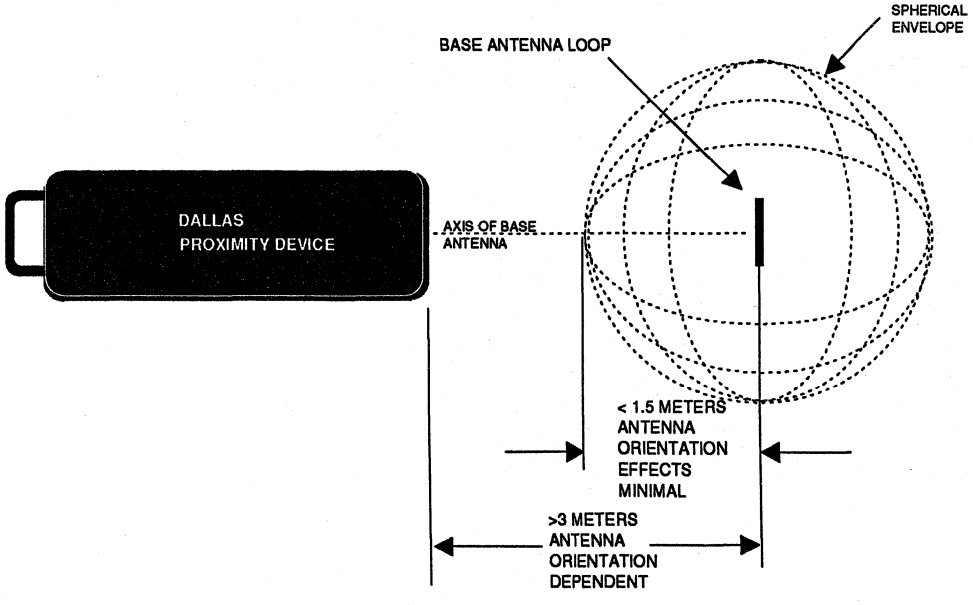


DS606xA DIMENSIONS

All measurements in INCHES



FREE SPACE RANGE Figure 3



DEVICE DEFINITION Figure 4

PROXIMITY DEVICE	DESCRIPTION	RELATED DATA SHEET
DS6065A Proximity Key	128-bit secure read/write memory. 64-bit ID and 64-bit password.	DS1204
DS6066A Proximity Tag	1024-bit read/write non-secure memory.	DS1200
DS6067A Proximity Device	512-bit read/write non-secure memory partition and three secure 384-bit read/write memory partitions.	DS1205

PROXIMITY DEVICE SPECIFICATIONS

Communication	Bidirectional, full duplex
Range (free space)	> 5 feet with DS6068A RF Communicator (see Figure 3)
Memory Capacity	Dependent on device definition
Transaction Response Time	< 200 ms with DS6068A RF Communicator
Operating Time	>10 years after freshness seal is disabled @ 25°C
Endurance	>1 million transactions
Transmit Frequency	303.875 MHz +/- 250 KHz (SAW stabilized)
Transmit Modulation	Binary Amplitude Shift KeyRing
Transmit Output Power	< 200 uV/meter @ 3 meters
Receiver Frequency	133.3 KHz +/- 2 KHz
Receiver Modulation	Binary Amplitude Shift Keying
Storage Temperature	-40°C to +80°C
Operating Temperature	-20°C to +50°C
Bit Transfer Rate	>1000 bits per second
Humidity	95%, noncondensing @ 50°C
Weight	22.7 grams

FCC CERTIFICATION ID

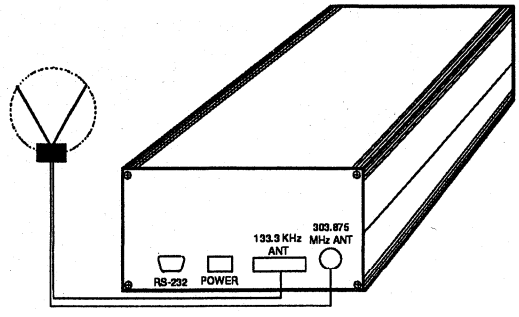
PART	CERTIFICATION ID
DS6065A	GIDDS6065A
DS6066A*	PENDING
DS6067A*	PLANNED

*THIS DEVICE HAS NOT BEEN APPROVED BY THE FEDERAL COMMUNICATIONS COMMISSION. THIS DEVICE IS NOT, AND MAY NOT BE, OFFERED FOR SALE OR LEASE, OR SOLD OR LEASED UNTIL THE APPROVAL OF THE FCC HAS BEEN OBTAINED

DALLAS SEMICONDUCTOR

DS6068A
RF Communicator

FEATURES
- Provides a wireless data link to Dallas proximity devices
- Two-way half-duplex radio link has range in excess of five feet
- Compatible with DS606xA series RF proximity devices
- Host communications occur over a standard asynchronous RS-232C port
- Communicates via a 133.3 KHz magnetic field transmitter and a 303.875 MHz UHF receiver
- Greater than 1000 bits per second RF data transfer rate
- Unlimited operation under Federal Communications Commission rules and regulations, Part 15, Subpart C
- Supplied with wall-mounted UL-approved power supply
- Includes antennas for transmitter and receiver



CONNECTIONS
RS-232 (DCE)
Power
Transmit Antenna: 133.3 KHz LF
Receive Antenna: 303.875 MHz UHF

RS-232 Port	DB-9 Female
Pin 1	No Connection
Pin 2	Receive Data In
Pin 3	Transmit Data Out
Pin 4	Data Terminal Ready
Pin 5	Ground
Pin 6-9	No Connection

POWER CONNECTOR	
Pin 1,3	14 VAC 50/60 Hz
Pin 2	Ground

DESCRIPTION
The DS6068A RF Communicator is a magnetic field transmitter and an RF receiver which will directly interface to a personal computer or terminal via a standard asynchronous RS-232 port. The RF Communicator is designed to work with DS606XA proximity devices forming a wireless RF link with a range greater than five feet. Its built-in microcontroller sends data to the proximity devices via a 133.3 KHz magnetic field transmitter and receives data from the 303.875 MHz RF SAW stabilized super-regenerative receiver. This two-way link allows communications to take place between the portable proximity devices and the fixed RF Communicator as people or objects pass within range. Because of the intelligence built into the RF Communicator in the form of the DS2250 Soft Microcontroller, the DS6068A can pick out a single proximity device present out of many while managing the digital-to-RF and RF-to-digital conversion required by the host system.

RF COMMUNICATOR OVERVIEW

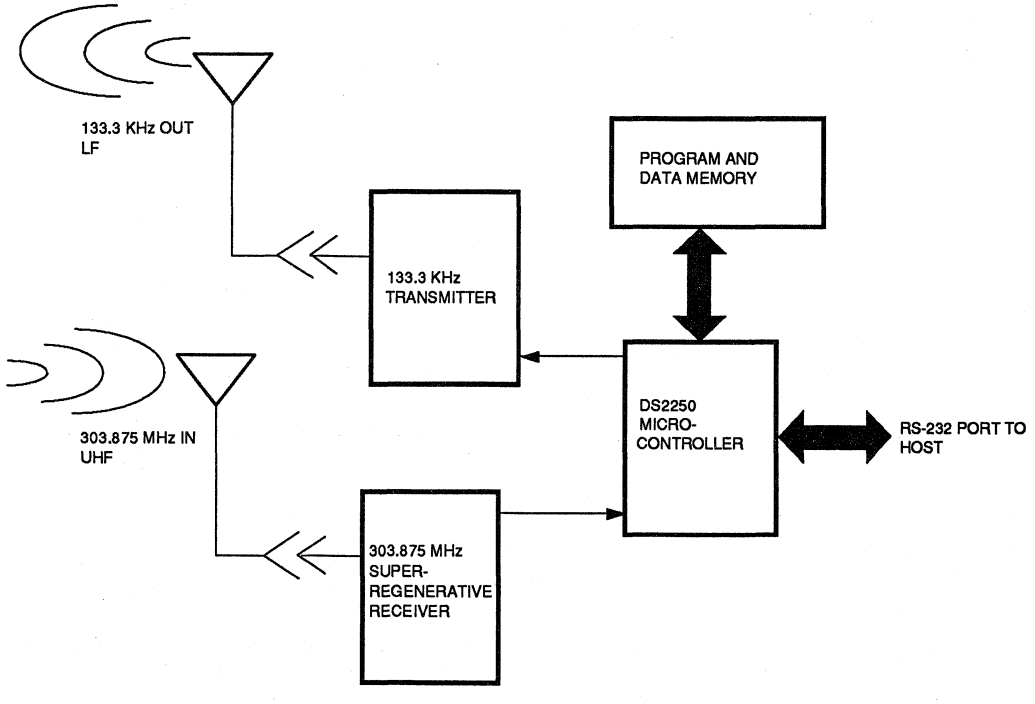
In order to understand the protocol and format of the RF/magnetic link, detailed knowledge of the DS606XA proximity device data sheet is recommended. Software for controlling the unit is available only in the DS6068AK Wireless Starter Kit. This software is written in Pascal and includes both source code and executables. For further information please refer to the DS6068AK data sheet.

RF COMMUNICATOR OPERATION

The block diagram shown in Figure 1 illustrates the main components within the DS6068A. As shown, RF information received by the 303.875 MHz super-regenerative receiver is processed by the DS2250 Soft Microcontroller and then output to the host via the RS-232 serial port. Digital information received by the DS2250 is converted into signals that excite the 133.3 KHz magnetic field transmitter which in turn produces pulse packets of varying sizes. These pulse packets contain both command and data information which is interpreted by the DS1209S-B1 device internal to the proximity devices.

Pulse packets are 20, 40, 60, 80, and 100 pulses in size (the definition and use of each type of pulse packet is described in the literature on the

RF COMMUNICATOR BLOCK DIAGRAM Figure 1



proximity devices and is not covered here). When data is being sent to the proximity device, only the 133.3 KHz transmitter is active. However, when data is to be retrieved from a proximity device, both the 133.3 KHz transmitter and the 303.875 MHz receiver are used. The RF Communicator sends out commands on the 133.3 KHz link and then listens for data being returned on the 303.875 MHz link. The data received is sent to the DS2250 where it is processed and stored in memory. The target system can then retrieve the data at its convenience over the RS-232 port.

TRANSMIT/RECEIVE ANTENNA

Both the transmit and receive antennae reside in a single package (Figure 3). The 133.3 KHz antenna is a wound resonant coil and the 303.875 MHz antenna is similar to a half-wave resonant dipole. The 133.3 KHz antenna is attached to the RF Communicator via line cord which is connected to the terminal block on the DS6068A. The 303.875 MHz antenna is attached to the RF Communicator via a 75-ohm coaxial cable and jack. The lengths of both cables allow the antenna to be mounted up to 1.85 meters away from the RF Communicator.

POWER SUPPLY

A wall-mounted, 120 VAC, 50/60 Hz , UL-approved power supply is included with each RF Communicator. For battery operation connect +12.5 to 15VDC to Pin 1 and Ground to Pin 2 of the Power Connector.

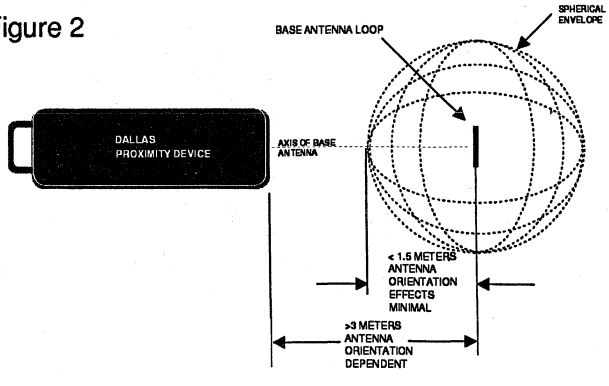
ENCLOSURE

Extruded aluminum: 2 1/2"(H) x 4 1/2"(W) x 7 1/2" (D). See Figure 4 for suggested mounting.

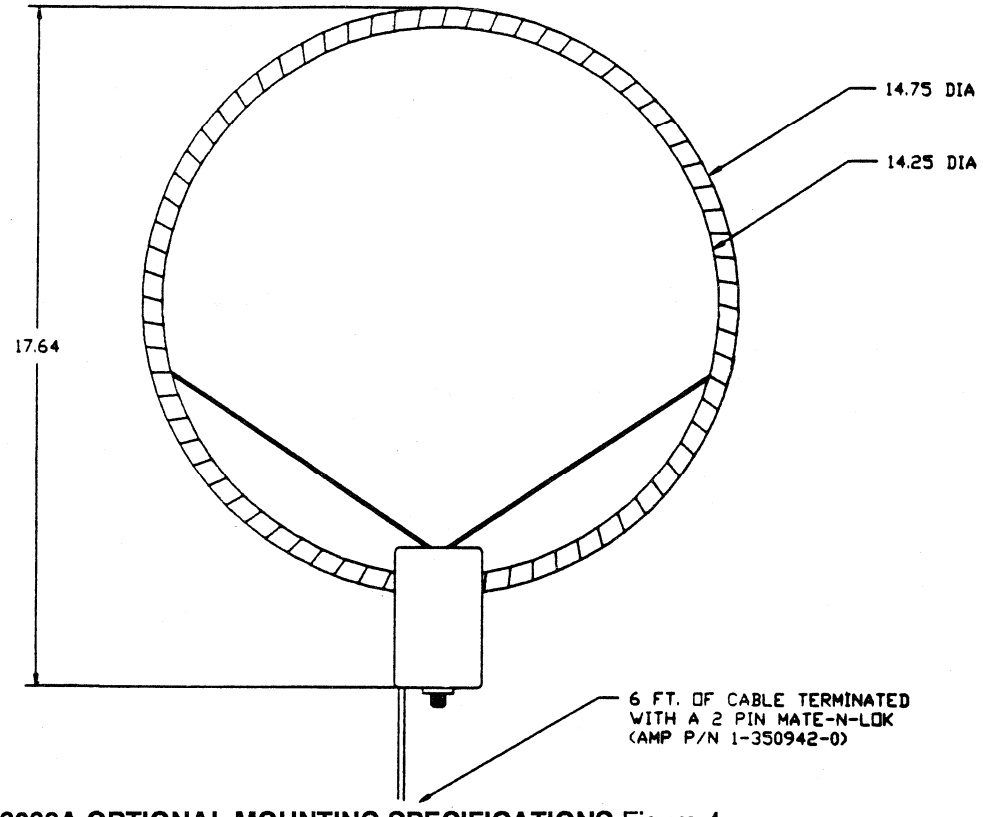
DS6068A RF COMMUNICATOR SPECIFICATIONS

Communication	Two-way Half-duplex
Range (Free Space)	> 5 feet with DS606XA proximity devices (see Figure 2)
Memory Capacity	8K bytes
Receiver Frequency	303.875 MHz SAW-stabilized
Transmitter Frequency	133.3 KHz magnetic
Transmitter Modulation	Binary Amplitude Shift Keying
Transmitter Radiated Power	< 18 uV/M @ 300 M
Storage Temperature	-40°C to +80°C
Operating Temperature	-20°C to +50°C
Operating Power	14 VAC +/- 10% 50/60 Hz @ 3 amp. max.
Antenna Feed Length	1.85 Meters
Weight	2.1 Kilograms (base unit, antennas, and power supply)
Humidity	95%, noncondensing @ 50°C
FCC ID	GIDDS6068A

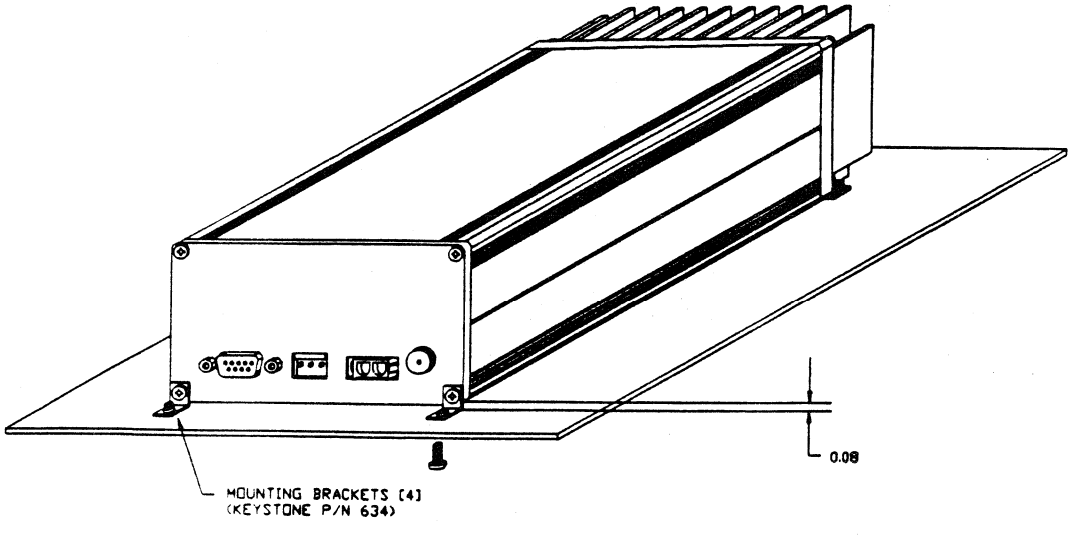
FREE SPACE RANGE Figure 2



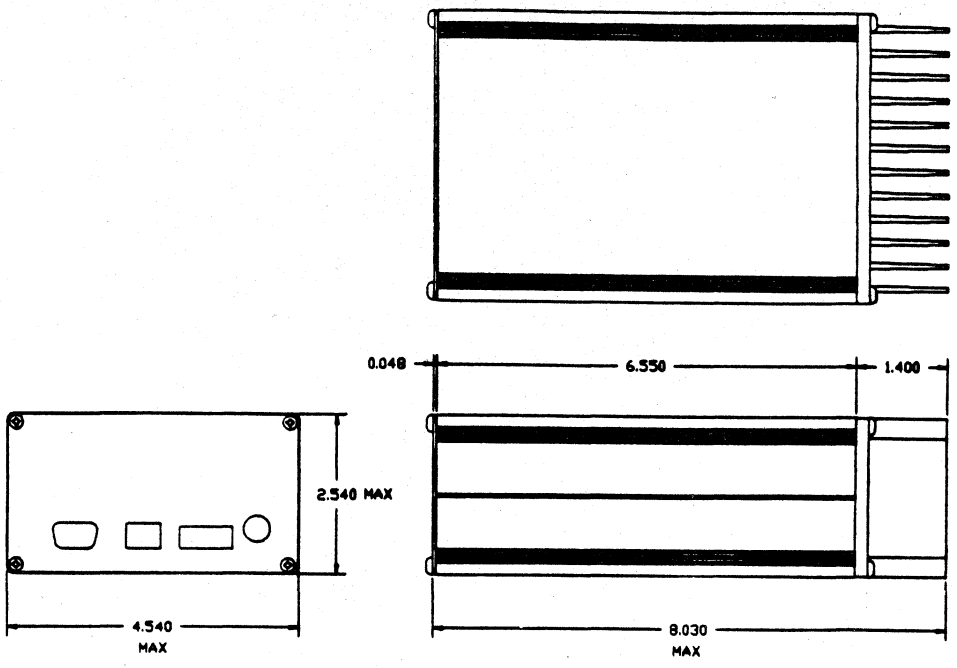
ANTENNA MECHANICAL DESCRIPTION Figure 3
(All dimensions in INCHES)



DS6068A OPTIONAL MOUNTING SPECIFICATIONS Figure 4
(All dimensions in INCHES)



DS6068A
RF COMMUNICATOR
(Dimensions in INCHES)

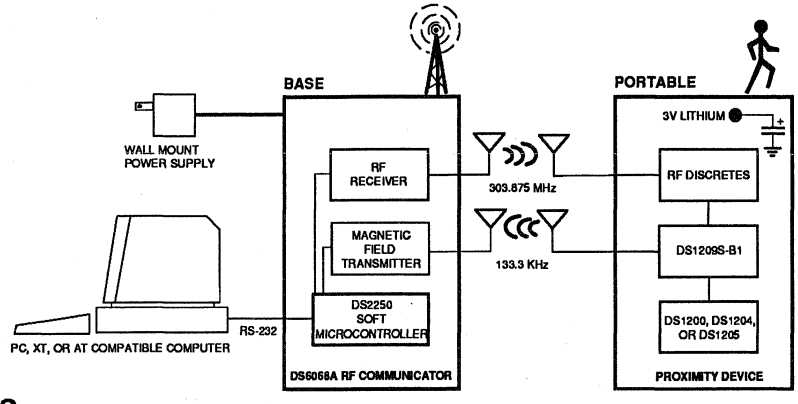


MATING CONNECTORS

133.3 KHz Antenna	AMP Mate-N-Loc 350-777-1 or equivalent
303.875 MHz Antenna	F-Style connector or equivalent
Power Supply	Molex 6442 or equivalent
DB-9S (RS-232)	AMP 745203-1 or equivalent

DALLAS SEMICONDUCTOR

DS6068AK
Wireless Starter Kit



INCLUDES:

- Two DS6065A Proximity Keys and one DS6066A Proximity Tag
- DS6068A RF Communicator for two-way information exchange with a range greater than five feet
- RS-232 DCE DB9 connector for easy interfacing to a personal computer serial communications port
- A U.S. type wall-mounted 120 VAC 50/60 Hz UL-approved power supply
- Software for IBM PC-compatible computers on 5 1/4" disks; source included
- Data sheets and documentation
- Unlimited operation under Federal Communications Commission (FCC) Rules and Regulations, Part 15, Subpart C

DESCRIPTION

The DS6068AK Wireless Starter Kit provides the basic components needed for rapid evaluation of proximity device performance: two DS6065A Proximity Keys, one DS6066A Proximity Tag, a DS6068A RF Communicator, antennas, cables, power-supply application software for IBM PC-compatible computers, documentation, and data sheets. The Starter Kit displays the contents of the proximity devices on a personal computer screen. The computer can exchange information with the proximity device over an RF link at a distance greater than five feet.

INSTRUCTIONS

Connect one end of a DB-9 to DB-9 cable to the DS6068AK Communicator and the other end to a personal computer. If not using an AT style port, use a DB-9 to DB-25 cable. Turn on the PC and then the DS6068A Communicator. Insert the software disk and print or type the "READ.ME" file. This file contains instructions for running the supplied applications software.

RF units are pre-licensed for unlimited operation under Federal Communications Commission (FCC) Rules and Regulations, Part 15, Subpart C.

Please see the DS6068A RF Communicator and DS606XA Proximity Device data sheets for technical information and performance specifications.

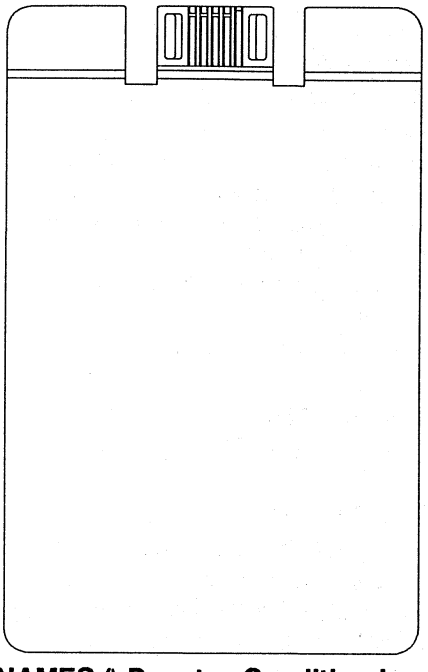
DALLAS SEMICONDUCTOR

DS6460
Proximity MegaTag

FEATURES

- Wireless read/write nonvolatile memory
- Read/write by both proximity and 3-wire (DQ, CLK, and RST\)
- Contains a 1 million-bit nonvolatile static RAM
- Up to 65,536 proximity devices can be uniquely addressed within the same wireless proximity
- Full-duplex radio link has range in excess of 3 meters
- Transmit link uses 303.875 MHz and receive link uses 133.3 KHz
- Greater than 1200 bits per second data transfer rate using 3-wire serial port
- Contains a lithium energy cell for 10 years of operation
- Applications include: access control, portable data record, and information system security

PIN DESCRIPTION



PIN NAMES (\ Denotes Condition Low)

1	Ground
2	Clock
3	Data
4	RST\
5	V_{CC}

DESCRIPTION

The DS6460 Proximity MegaTag is a one million- bit memory device with both a 3-wire serial interface and a wireless transceiver internal to the device. Wireless data transfers take place between a DS6460 Proximity MegaTag and a DS6068A RF Communicator at greater than 1200 bits per second. Distances of over 3 meters are achieved through the use of a SAW-stabilized transmitter. Up to 65,536 proximity devices can be individually addressed within the same operating proximity. When using a 3-wire serial interface, data can be transferred at up to 1 million bits per second. The DS6460 Proximity MegaTag is designed to be rugged and durable enough to withstand normal handling with a life expectancy of over ten years.

DALLAS SEMICONDUCTOR

DS9092
Touch Device Probe

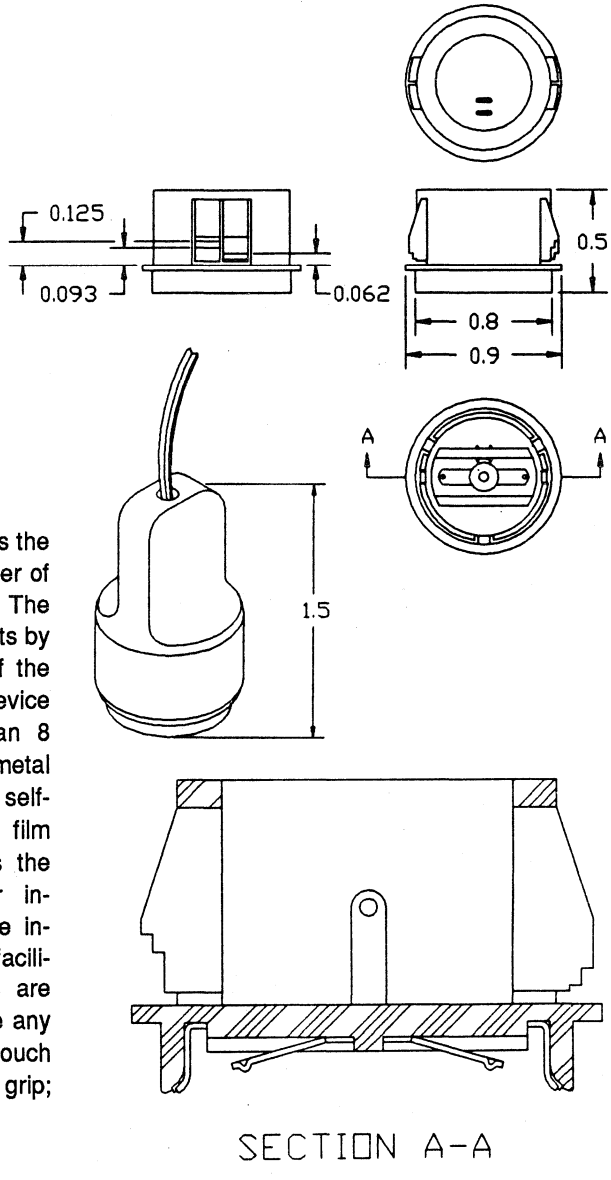
FEATURES

- Low-cost read/write probe for DS199x Touch Devices
- Self-centering cup shape guides alignment
- Durable metallic alloy wipes clean with each soft touch
- Dual rim and surface contact areas increase reliability
- Locking retainer facilitates panel mounting
- Solder terminals allow user-defined cable length
- Optional finger grip for ease of handling (DS9092G)

DESCRIPTION

The DS9092 Touch Device Probe provides the electrical contact necessary for the transfer of data to and from a DS199X Touch Device. The rounded cup shape tolerates misalignments by sliding over the matching circular rim of the Touch Device. In this way, a Touch Device can be captured when struck within an 8 millimeter radius of its center line. Solid metal contact surfaces resist wear and have a self-cleaning wiping action for eliminating film build-ups. The rim contact as well as the surface contact have redundancy for increased reliability. Locking retainers are incorporated into the DS9092 housing to facilitate panel mounting. Solder terminals are provided which allow the customer to use any desired length of cable. The DS9092 Touch Device Probe is available with a finger grip; specify the DS9092G when ordering.

PACKAGE DESCRIPTION

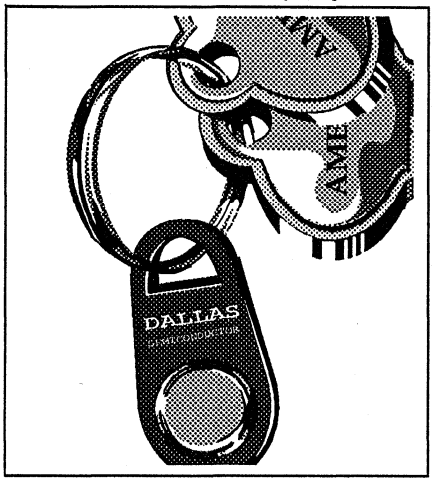


DALLAS SEMICONDUCTOR

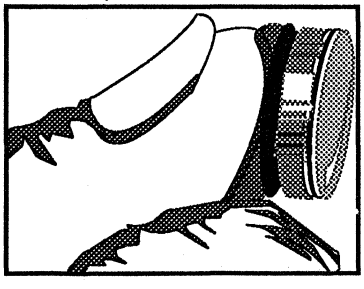
DS9093
Touch Device Mount

FEATURES

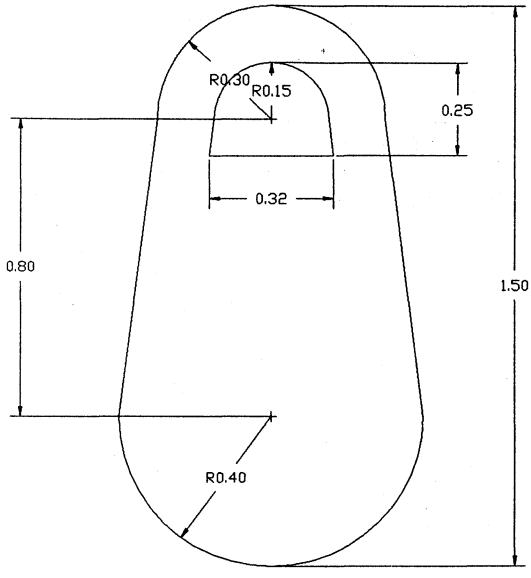
- Attaches Touch Device to key ring



- Holder for using Touch Device as a thumb pad



DIMENSIONS



DESCRIPTION

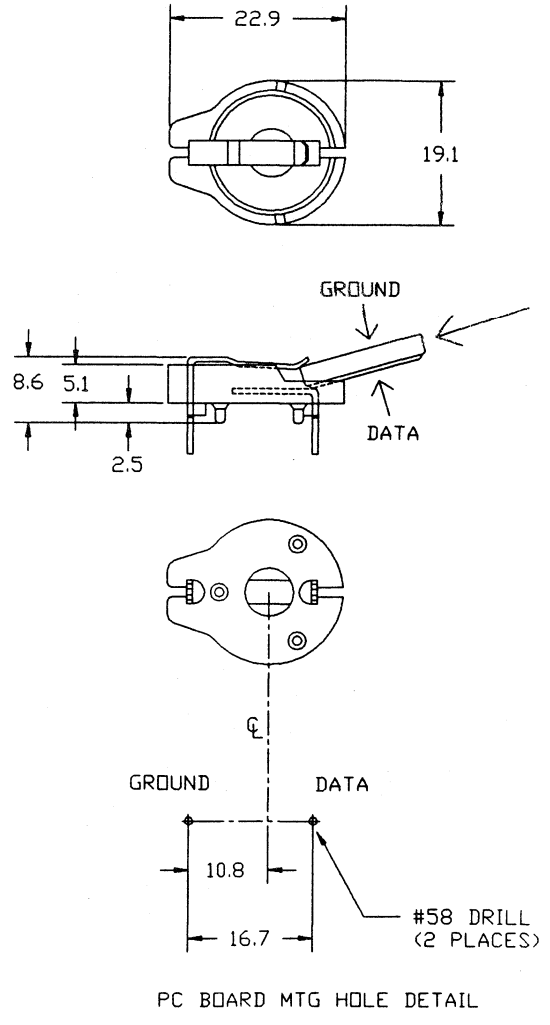
The DS9093 Touch Device Mount is a low-cost plastic fob that holds a Touch Device. It provides stability and ease of handling for a Touch Device when used in thumb pad applications. It can be attached to a key ring for carrying.

DALLAS SEMICONDUCTOR

DS9094
Touch Device Clip

FEATURES

- Low-cost holder for DS199x Touch Devices
- Printed circuit board mount
- Contacts are 302 spring stainless steel, nickel-plated
- Flammability rating: UL94V-O



PC BOARD MTG HOLE DETAIL

DESCRIPTION

The DS9094 Touch Device Clip holds a DS199x Touch Device and connects to a printed circuit board. With the molded design, Touch Devices can be inserted and extracted without special tools. If the Touch Device is improperly installed, a beveled edge on the DS9094 prevents contact. The DS9094's low profile minimizes the clearance height above the printed circuit board.

Telecommunications

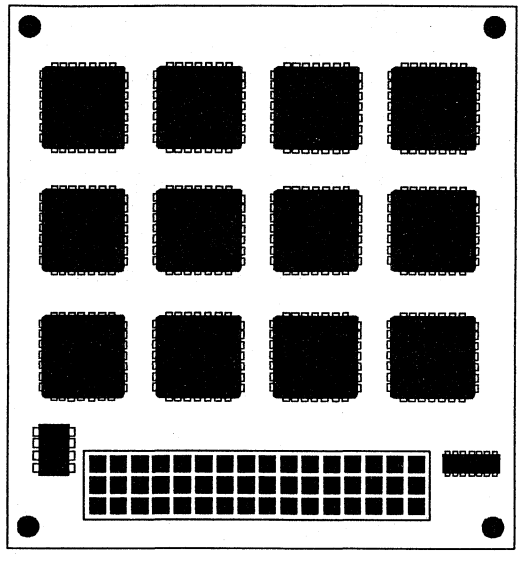
The following Telecom datasheets are one-page overviews. For complete datasheets, please refer to the Dallas Semiconductor Telecom Data Book.

DALLAS SEMICONDUCTOR

DS2157/8
ADPCM Array Chip

FEATURES

- High-density, multi-channel speech compression system provides full-duplex channels on a 3 x 3 inch board.
- Based on high-performance DS2167/68 ADPCM processors. DS2157 uses the DS2167 ADPCM Processor Chip and supports the July 1986 T1Y1 recommended algorithm. DS2158 supports the "old" CCITT G.721 algorithm.
- Flexible data bussing scheme accommodates user's backplane data format and rate.
- Microcontroller-compatible port for system configuration. Onboard power monitor provides system reset.



DESCRIPTION

The DS2157 and DS2158 ADPCM Array Chips use surface-mount technology and the DS2167/68 ADPCM Processor Chips to yield 12 or 24 full-duplex channels in nine square inches. The DS2157 Array features the DS2167Q Processor, which implements the July 1986 T1Y1 recommended ADPCM algorithm. The DS2158 array features the DS2168Q Processor, which implements the "old" CCITT G.721 algorithm. The PCM data interfaces are organized into four independent busses which can be configured to best suit the data format on the user's system backplane. The array also includes input signal buffering and a power-monitor reset circuit.

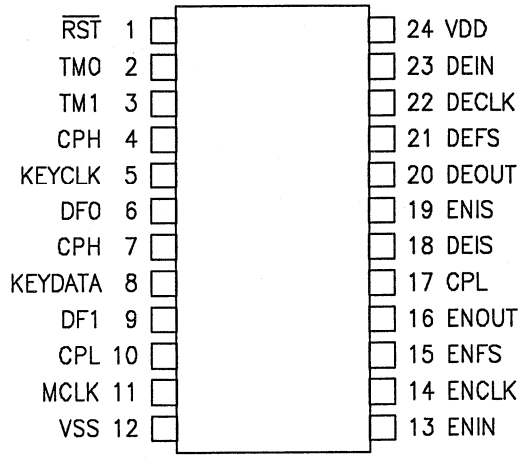
DALLAS SEMICONDUCTOR

DS2160
DES Processor Chip

FEATURES

- Performs voice/data encryption and decryption according to the Data Encryption Standard (DES)
- Full-duplex operation; one encrypt channel, one decrypt channel
- Each channel can process up to 64K bits per second
- Connects directly to combo-codec devices
- Simple key entry
- Uses Cipher Feedback Mode (CFB) of the DES standard
- Can encrypt/decrypt either 8 bits, 7 bits, 6 bits, or 4 bits
- Single +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

PIN CONNECTIONS



DS2160 24-Pin DIP

DESCRIPTION

The DS2160 DES Processor Chip is a dedicated Digital Signal Processing (DSP) CMOS chip optimized for the National Bureau of Standard's Data Encryption Standard (DES) algorithm. The DS2160 has two channels: one for encryption and one for decryption. The chip performs encipher/decipher operations on 64-bit words at a rate of up to 64K bits per second per channel.

To provide security as specified in DES, a 64-bit key is necessary. The key is entered into the DS2160 through a simple serial port and cannot be accessed externally. The DES algorithm is used in both governmental and commercial applications where sensitive information is passed though unsecured media.

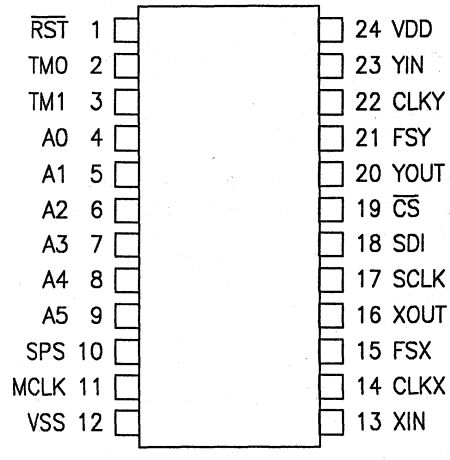
DALLAS SEMICONDUCTOR

DS2165
16/24/32Kbps ADPCM Processor Chip

FEATURES

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps
- Dual fully independent channel architecture; device can be programmed to perform either:
  - two expansions
  - two compressions
  - one expansion and one compression
- Interconnects directly to combo-codec devices
- Input to output delay is less than 375 us
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports channel associated signaling
- Each channel can be independently idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2167 ADPCM Processor Chip
- Single +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

PIN DESCRIPTION



DS2165 24-Pin DIP

DESCRIPTION

The DS2165 ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression to 32Kbps follows the algorithm specified by CCITT Recommendation G.721 (July 1986) and ANSI document T1.301 (April 1987). The compression to 24Kbps follows ANSI document T1.303. The compression to 16Kbps follows a proprietary algorithm developed by Dallas Semiconductor. The DS2165 can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

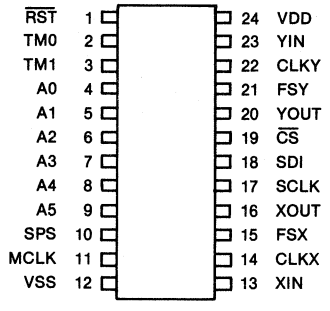
DALLAS SEMICONDUCTOR

DS2167/8
ADPCM Processor Chip

FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations
  - DS2168 supports "old" CCITT G.721 recommendations
- Dual independent channel architecture—device may be programmed to perform full duplex , 2-channel expansions, or 2-channel compressions
- Interconnects directly with *u*-law or A-law combo-codec devices
- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications
  - On-chip channel counters identify input and output timeslots in TDM-based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- Hardware mode intended for stand-alone use
  - No host processor required
  - Ideal for voice mail applications
- 28-pin surface-mount package available, designated DS2167Q/ DS2168Q

PIN CONNECTIONS



DESCRIPTION

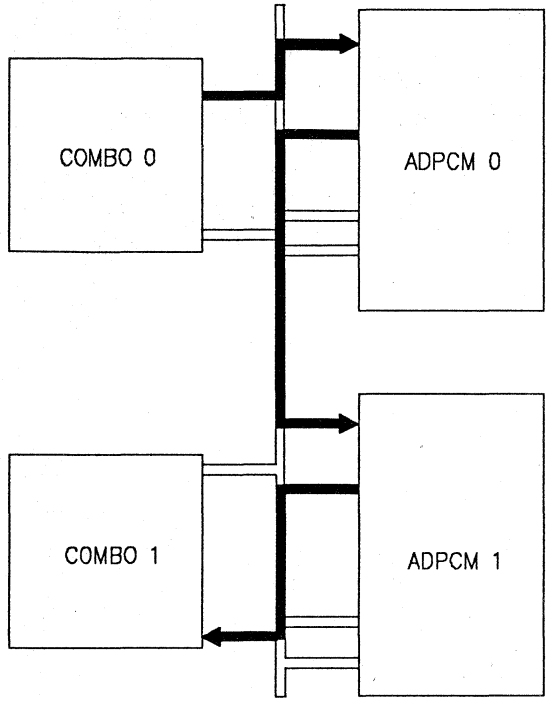
The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

DALLAS SEMICONDUCTOR

DS2167K
ADPCM Design Kit

FEATURES

- Emulates multi-channel applications such as T1 transcoders
- Expedites new designs by eliminating first-pass device prototyping
- Interfaces directly to IBM PC, XT, AT and compatibles
- High-level, graphic software demonstrates chip flexibility and feature set
- Kit components include:
  - DS2167 ADPCM processors (2)
  - Codec-combo devices (2)
  - Timeslot assigner circuit (TSAC) for combos
  - Support logic and clock generation circuitry
  - Printed circuit board
  - Interface cable for PC
  - Documentation and control software diskette



DESCRIPTION

The ADPCM design kit provides everything a user needs to evaluate the DS2167 ADPCM processors in an actual system environment. The evaluation board connects directly to transmission tests for performance monitoring of compressed or expanded channels. The board requires +/-5 volts. A system control interface connects directly to the PC parallel printer port.

The kit's control software turns the PC into a powerful system controller. The program gives the user full control of system configuration, including timeslot placement, operating modes (compression, expansion, bypass or idle), data formats and algorithm reset. The controller program runs under MS DOS or IBM DOS version 2.0 or later. Color monitors are supported but not required.

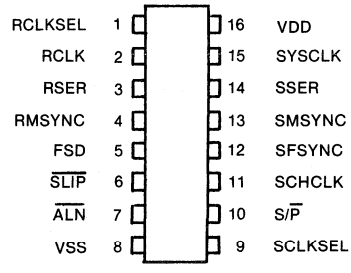
DALLAS SEMICONDUCTOR

DS2175
T1/CEPT Elastic Store Chip

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
  - Slips occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A DS2181 CEPT Transceivers
- Industrial temperature range of −40° to +85°C available, designated DS2175N

PIN CONNECTIONS



DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

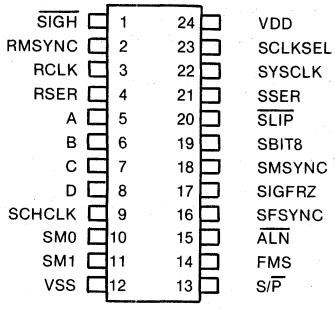
DALLAS SEMICONDUCTOR

DS2176
Elastic Store with Signaling Buffer Chip

FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of −40°C to +85°C available, designated **DS2176N**

PIN CONNECTIONS



DESCRIPTION

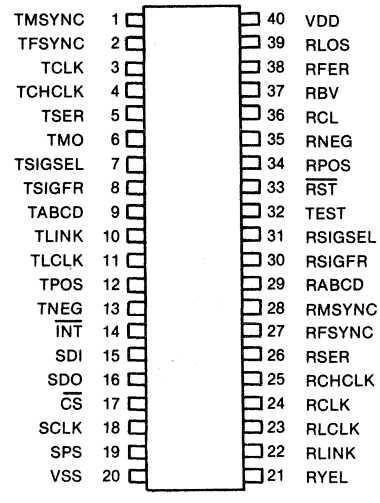
The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DALLAS SEMICONDUCTOR

DS2180A
T1/ISDN Primary Rate Transceiver

FEATURES
- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of −40 °C to +85 °C available, designated DS2180AN or DS2180AQN

PIN CONNECTIONS



DESCRIPTION
The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

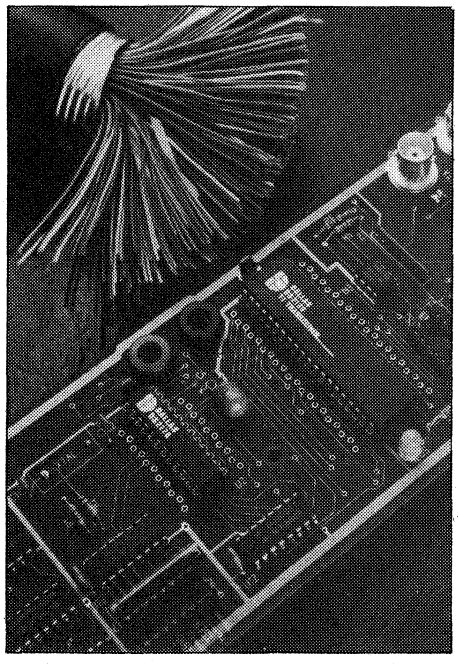
Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

DALLAS SEMICONDUCTOR

DS2180K
T1 DESIGN KIT

FEATURES

- Demonstrates key "hardware mode" attributes of the DS2180/DS2176 pair, such as:
  - Framing/synchronization
  - Link supervision and control
  - Signaling supervision
  - Rate adaption to equipment backplanes
- Expedites new designs by eliminating first-pass device prototyping
- Easily interfaced to user host controller for "software mode" evaluation
- User-supplied line interface allows direct connection to T1 lines
- Kit components include:
  - DS2180 T1 Transceiver
  - DS2176 T1 Receive Buffer
  - Printed circuit board
  - Support logic and clock generation circuitry
  - Applications and assembly information



DESCRIPTION

The DS2180K allows the user to evaluate the performance of the DS2180 T1 Transceiver and DS2176 T1 Receive Buffer in an actual system environment. The evaluation board requires +5 volts; board inputs and outputs are TTL-compatible. Test points and control options on the board simplify selection of device feature sets required by the system designer.

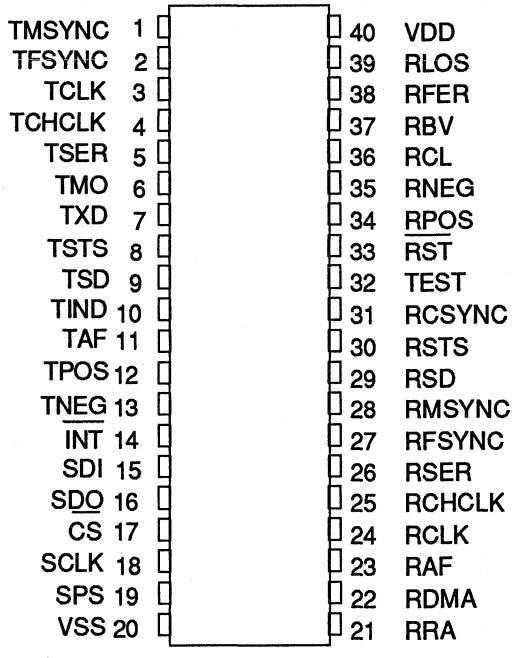
Kit assembly requires approximately 1 hour. Although designed for hardware mode operation, a small wire-wrap area is provided for user-supplied host processor interface.

DALLAS SEMICONDUCTOR

DS2181
CEPT Transceiver Chip

FEATURES
- Single chip primary rate transceiver meets CCITT standards G.704 and G.732
- Supports new CRC4-based framing standards and CAS and CCS signaling standards
- Simple serial interface used for device configuration and control in processor mode
- Hardware mode requires no host processor; intended for standalone applications
- Comprehensive, on-chip alarm generation, alarm detection, and error logging logic
- Shares footprint with DS2180A T1/ISDN Primary Rate Transceiver
- Companion to DS2175 T1/CEPT Elastic Store Chip
- 5V supply; low-power CMOS technology

PIN CONNECTIONS



DS2181 40-Pin DIP

DESCRIPTION
The DS2181 CEPT Transceiver Chip is designed for use in CEPT networks and supports all logical requirements of CCITT Red Book Recommendations G.704 and G.732. The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signaling data, and produces network alarm codes when enabled. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signalling, and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls such features such as error logging, per-channel code manipulation, and alteration of the receive synchronizer algorithm.

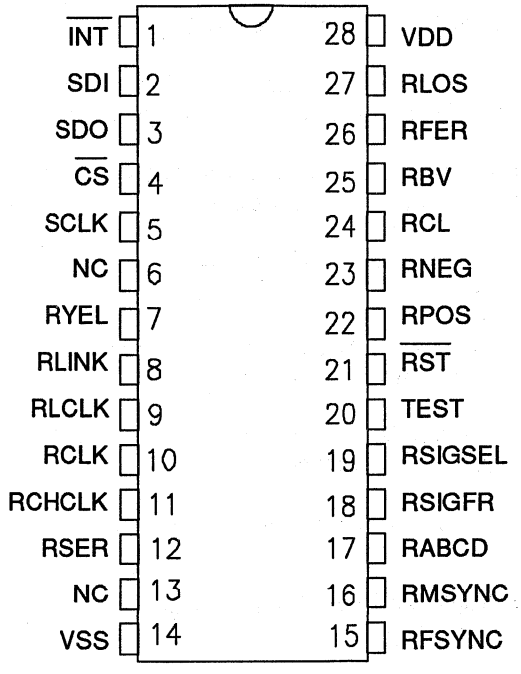
The hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.

DALLAS SEMICONDUCTOR

DS2182
T1 Line Monitor Chip

FEATURES
- Performs framing and monitoring functions
- Supports Superframe and Extended Superframe formats
- Designed to fulfill the requirements outlined in TA-TSY-000147 (DS1 Rate Digital Service Monitoring Unit) and TR-TSY-000194 (ESF Interface Specification)
- Four onboard error counters
  - 16-bit bipolar violation
  - 8-bit CRC
  - 8-bit OOF
  - 8-bit frame bit error
- Indication of the following
  - yellow and blue alarms
  - incoming B8ZS code words
  - 8 and 16 zero strings
  - change of frame alignment
  - loss of sync
  - carrier loss
- Simple serial interface used for configuration, control and status monitoring
- Burst mode allows quick access to counters for status updates
- Automatic counter reset feature
- Single 5V supply; low-power CMOS technology
- Available in 28-pin DIP and 28-pin PLCC

PIN DESCRIPTION



DS2182 28-Pin DIP

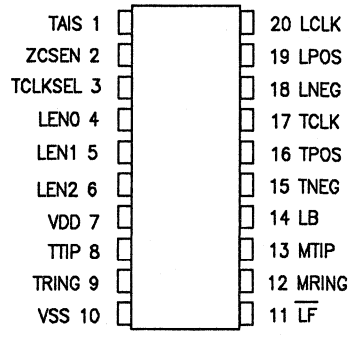
DESCRIPTION
The DS2182 T1 Line Monitor Chip is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182 frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. Large onboard counters allow the accumulation of errors for extended periods, which permits a single CPU to monitor a number of T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-Bits, FDL bits, signaling bits, and channel data.

DALLAS SEMICONDUCTOR

DS2186
T1/CEPT Transmit Line Interface Chip

FEATURES
- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- On-chip transmit LBO (line build out) and line drivers eliminate external components
- Programmable output pulse shape supports short-and long-loop applications
- Supports bipolar and unipolar input data formats
- Transparent B8ZS and HDB3 zero code suppression modes
- Compatible with DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2187 Receive Line Interface
- Single 5V supply; low-power CMOS technology

PIN CONNECTIONS



DS2186 20-Pin DIP

DESCRIPTION
The DS2186 T1/CEPT Transmit Line Interface Chip interfaces user equipment to North American (T1-1.544MHz) and European (CEPT-2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable waveshaping circuitry, line drivers, remote loopback, and zero suppression logic. A line-coupling transformer is the only external component required.

Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 dB, -7.5 dB and -15 dB) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI. The DS2186 supports ISDN -PRI (Primary Rate Interface) specifications.

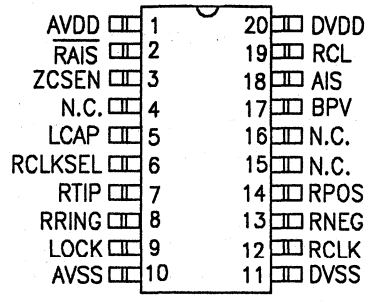
DALLAS SEMICONDUCTOR

DS2187
T1/CEPT Receive Line Interface Chip

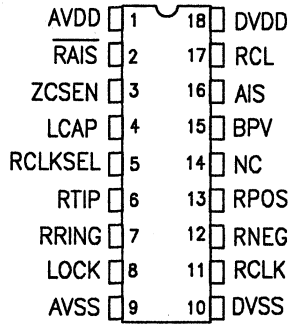
FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, PUB 62411, and applicable CCITT G.823
- Precision on-chip PLL eliminates external crystal or LC tank -- no tuning required
- Decodes AMI, B8ZS, and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1/ISDN Primary Rate and DS2181 CEPT Transceivers
- Companion to the DS2186 T1/CEPT Transmit Line Interface Chip
- Single 5V supply; low-power CMOS technology

PIN CONNECTIONS



DS2187 20-Plin SOIC



DS2187 18-Pin DIP

DESCRIPTION

The DS2187 T1/CEPT Receive Line Interface Chip interfaces user equipment to North American (T1 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks, and PABX-to-computer interfaces such as DMI and CPI.

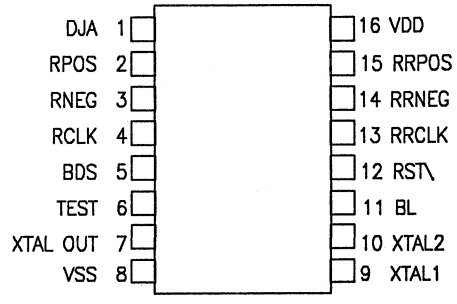
DALLAS SEMICONDUCTOR

DS2188
T1/CEPT Jitter Attenuator Chip

FEATURES

- Attenuates clock and data jitter present in T1 or CEPT lines
- Meets the jitter attenuation templates outlined in TR62411, TR-TSY-000170, G.735, and G.742
- Only one external component required; either a 6.176MHz (T1) or 8.192MHz (CEPT) crystal
- Selectable buffer size of 128 or 32 bits
- Jitter attenuation is easily disabled
- Single +5V supply; low-power CMOS technology
- Available in 16-pin DIP and 16-pin SOIC

PIN DESCRIPTION



DS2188 16-Pin DIP

DESCRIPTION

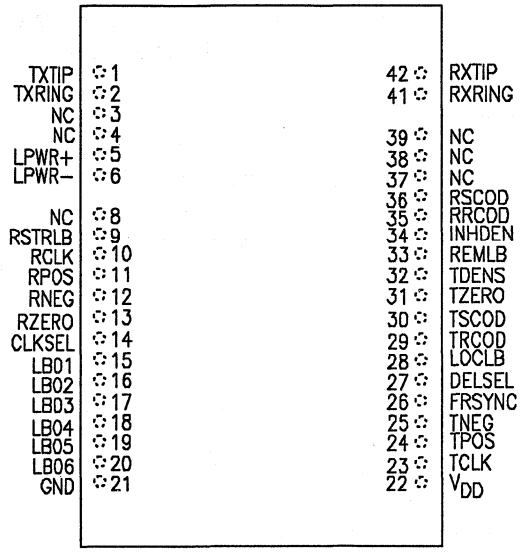
The DS2188 T1/CEPT Jitter Attenuator Chip contains a 128 X 2-bit buffer which, in conjuction with an external 4X crystal, is used to attenuate the incoming jitter present in clock and data. The device meets all of the latest applicable specifications including those outlined in TR 62411(ACCUNET* T1.5 Service Description and Interface Specifications, December 1988), TR-TSY-000170 (Digital Cross-Connect System Requirements and Objectives, November 1985), and the CCITT Recommendations G.735 and G.742. The DS2188 is compatible with the DS2180A T1/ISDN Primary Rate Transceiver and DS2181 CEPT Transceiver and it is the companion to the DS2187 T1/CEPT Receive Line Interface and DS2186 T1/CEPT Transmit Line Interface. It can also be used in conjunction with the DS2190 T1 Network Interface Unit.

DALLAS SEMICONDUCTOR

DS2190-003
T1 Network Interface Unit (NIU)

FEATURES
- Modularized network interface for 1.544 Mbps T1 services
- Network side connects directly to T1 line
- Compatible with DS2180A T1/ISDN Primary Rate Transceiver
- Small size--approximately six square inches--permits integration onto line cards
- Compatible with AT&T publication 62411
- FCC Part 68 and Part 15 pre-registration
- Extracts clock and data with no external components or tuning
- Detects and generates in-band loopback codes
- Assures proper ones density to network
- Powered by a local +5 volt supply

PIN CONNECTIONS



DESCRIPTION
The DS2190 T1 Network Interface Unit is a small sealed module designed to meet the recommendations of AT&T Publication 62411 for interfacing to T1 1.544 Mbps services (such as Accunet* T1.5, Skynet* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing cost and increasing total system performance. Basic functions of the DS2190 are: clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

*Service marks of AT&T Communications

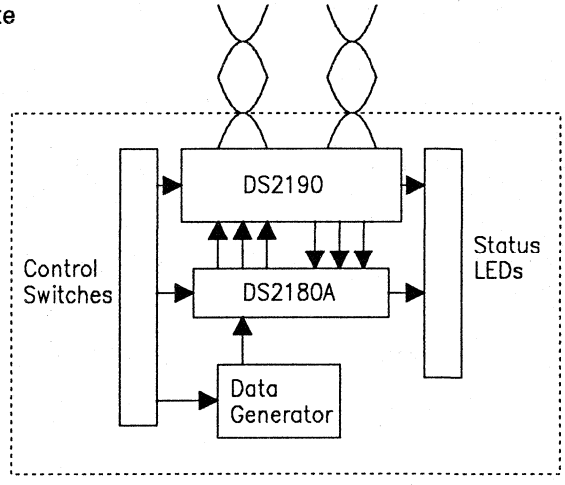
DALLAS SEMICONDUCTOR

DS2190DK
T1 Network Interface Unit Design Kit

FEATURES

- Self - contained system designed to evaluate the DS2190 T1 Network Interface Unit
- Includes the following:
  - DS2190 Network Interface Unit
  - DS2180A T1/ISDN Primary Rate Transceiver
  - Transmit Clock and Frame Sync Circuitry:
  - Status LEDs
  - Control DIP switches
  - Bantam Jacks
  - Documentation
- Kit comes completely assembled
- Easily accessable test points
- Onboard data generator capable of QRSS generation and channel data insertion
- Prototyping wire-wrap area for user customization
- Powered by a single +5V supply

DESIGN KIT LAYOUT



DESCRIPTION

The DS2190DK T1 NIU Design Kit contains all of the necessary support logic to completely evaluate the DS2190 T1 Network Interface Unit. The DS2190DK can be connected to either T1 test equipment, or a simulated T1 line, or back onto itself. The board is organized for simplicity of operation. It is controlled through DIP switches, and real-time status can be monitored through a set of LEDs. The DS2190DK allows the user to customize the kit to fit their needs. There is a prototyping wire-wrap area and all key signals are brought out to test points. An optional computer interface to control the DS2180A T1/ISDN Primary Rate Transceiver in the software mode is also available.

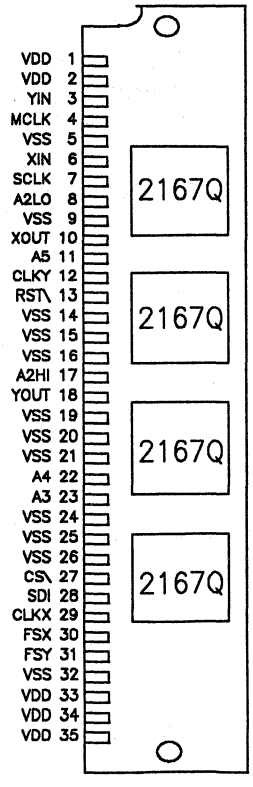
DALLAS SEMICONDUCTOR

DS2264
DS2268
ADPCM Stik

FEATURES

- Provides four channels (DS2264) or eight channels (DS2268) of parallel full-duplex APDCM processing in a pre-fabricated, snap-in module
- Based on the DS2167Q APDCM Processor Chip which implements the T1.301 and CCITT G.721 recommendations
- Occupies only 2 square inches of board space
- Conforms to popular JEDEC standard 35 position single in-line connector
- Easily cascadable up to 64 full-duplex channels in multiples of four or eight
- Both A-law and U-law compatible
- Utilizes serial interface port for microprocessor control of timeslot assignments
- Includes onboard buffers for all critical signals

PIN DESCRIPTION



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DESCRIPTION

The DS2264 and DS2268 ADPCM Stiks are complete, pre-fabricated cards that perform either four or eight channels of full-duplex ADPCM processing. The ADPCM algorithm compresses 64Kbps voice data to 32Kbps. The DS2264 is only populated on one side and offers four channels while the DS2268 is populated on both sides of the Stik and offers eight channels. Control of the Stiks is handled by an external microcontroller via a serial port. Both Stiks are based on the DS2167Q ADPCM Processor Chip. Specific details on the DS2167Q can be found in the DS2167 data sheet.

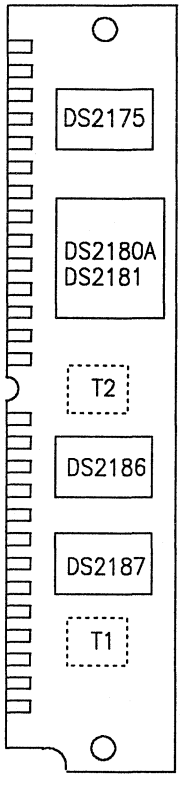
DALLAS SEMICONDUCTOR

DS2280/1
T1/CEPT Line Card Stik

FEATURES

- Pretested, snap-in T1 or CEPT line card
- DS2280 T1 Line Card
  DS2281-075 75 ohm CEPT Line Card
  DS2281-120 120 ohm CEPT Line Card
- Consumes only 2 square inches of board space
- Performs four functions:
  - line interface
  - framing
  - monitoring
  - buffering
- DS2280 and DS2281 share the same pinout
- Includes line interface transformers and termination resistors
- Connects to both 1.544MHz and 2.048MHz backplanes
- Operates off a single +5V supply

Stik LAYOUT



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DESCRIPTION

The DS2280 and DS2281 are T1 and CEPT line cards that consume only two square inches of printed circuit board space. The cards are designed to plug into standard 68-pin single in-line connectors. They have been arranged for maximum flexibility and contain all the necessary hardware to connect directly to either T1 or CEPT 75 ohm lines, or CEPT 120 ohm lines. The line interface function is performed by the DS2187 T1/Cept Receive Line Interface Chip and DS2186 T1/CEPT Transmit Line Interface Chip. The monitoring and framing functions are performed by the DS2180A T1/ISDN Primary Rate Transceiver on the DS2280 and by the DS2181 CEPT Transceiver Chip on the DS2281. The buffering function is handled by the DS2175 T1/CEPT Elastic Store Chip. The DS2280 and DS2281 provide all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). They also provide indication of frame errors, CRC-6 or CRC-4 errors, and bipolar violations.

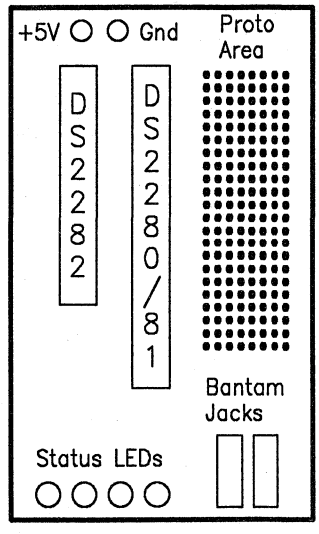
DALLAS SEMICONDUCTOR

DS2280DK
T1 Line Card Stik Design Kit

FEATURES

- Demonstrates Dallas Semiconductor's entire T1 chip set via the DS2280 T1/CEPT Line Card Stik and the DS2282 T1 FDL Controller/Monitor Stik
- Contains software that will enable an IBM- compatible PC to communicate with either the DS2280 or DS2282
- Contains SIP Stik connectors for the DS2280 and DS2282
- Eurocard size; can be mounted in the DS9005 Eurocard Enclosure
- Easily accessible test points
- Prototyping wire-wrap area for user customization
- Can also be used with the DS2281 T1/ CEPT Line Card Stik
- Powered by a single +5V supply

KIT LAYOUT



NOTE:
The DS2280DK does not contain the DS2280, DS2281, or DS2282.

DESCRIPTION

The DS2280DK T1 Line Card Stik Design Kit allows the user to evaluate Dallas Semiconductor's line of T1 products. The design kit is set up to demonstrate the DS2280 T1/CEPT Line Card Stik and the DS2282 T1 FDL Controller/Monitor. It is arranged to provide maximum flexibility and is easily customized to meet the user's needs. Software is provided to allow an IBM PC or compatible to communicate with the DS2280 and DS2282. Since the DS2281 T1/CEPT Line Card Stik shares the same pinout as the DS2280, the DS2280DK can be used to evaluate the DS2281 as well as the DS2280. Please contact Dallas Semiconductor for more information about this product.

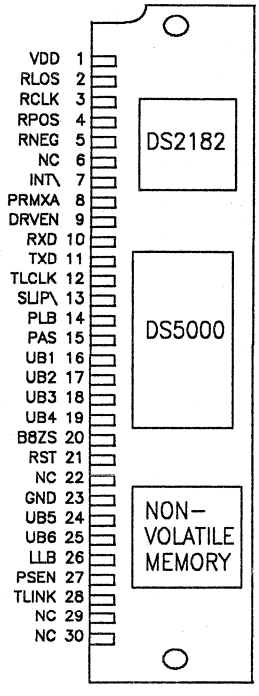
DALLAS SEMICONDUCTOR

DS2282
T1 FDL Controller/ Monitor Stik

FEATURES

- Fully implements the FDL message format as described in TR-TSY-000194 and T1.403-1989
- Supports both scheduled performance report messages and unscheduled messages
- Software implementation allows adaptation to evolving standards
- Provides high-level monitor counts, namely:
  - errored seconds
  - severely errored seconds
  - unavailable seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the DS2280 T1/CEPT Line Card Stik or DS2180A T1/ISDN Primary Rate Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

Stik LAYOUT



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DESCRIPTION

The DS2282 T1 FDL Controller/Monitor Stik completely controls the Facility Data Link (FDL) as described in the Bellcore document TR-TSY-000194 (Extended Superframe Format Interface Specification, December 1987) and the ANSI document T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). It also provides a number of important performance parameters involved in monitoring T1 lines. Since the DS2282 is implemented using the DS5000 Soft Microcontroller, it easily adapts to evolving T1 standards and can be customized to meet the user's needs. For example, the DS2282 can be modified to implement the TABS protocol as described in the AT&T Communications document PUB 54016.

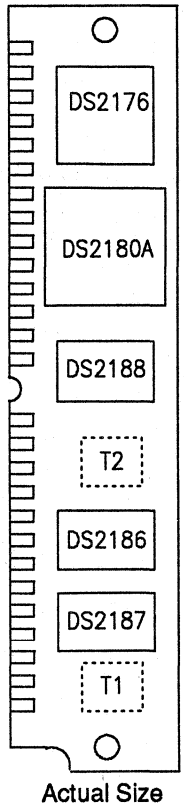
DALLAS SEMICONDUCTOR

DS2283
Enhanced T1 Line Card Stik

FEATURES

- Pretested, snap-in T1 line card
- Consumes only 2 square inches of board space
- Performs six functions:
  - line interface
  - clock and data dejittering
  - framing
  - monitoring
  - buffering
  - robbed-bit signaling extraction
- Includes line interface transformers and termination resistors
- Three separate loopback modes: payload, line, and local
- Connects to both 1.544MHz and 2.048MHz backplanes
- Fully CMOS for low power consumption
- Operates off a single +5V supply

Stik LAYOUT



Actual Size

DESCRIPTION

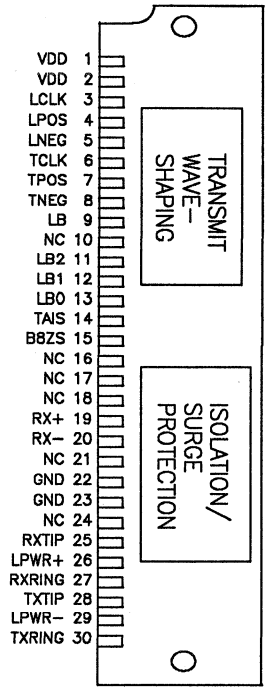
The DS2283 Enhanced T1 Line Card Stik is a T1 line card that consumes only two square inches of printed circuit board space. The card is designed to plug into standard 68-pin single in-line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to T1 DSX-1 twisted pair lines. The line interface function is performed by the DS2187 T1/CEPT Receive Line Interface Chip and DS2186 T1/CEPT Transmit Line Interface Chip. The dejittering of the clock and data is performed by the DS2188 T1/CEPT Jitter Attenuator Chip. The monitoring and framing functions are performed by the DS2180A T1/ISDN Primary Rate Transceiver. The buffering and robbed-bit signaling extraction functions are handled by the DS2176 T1 Elastic Store with Signaling Buffer Chip. The DS2283 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC-6 errors, and bipolar violations. Please contact Dallas Semiconductor for more information on this product.

DALLAS SEMICONDUCTOR

DS2290
T1 Isolation Stik

FEATURES
- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1500 volts of isolation
- FCC Part 68 registered
- Meets TR 62411 and T1.403-1989 for transmit pulse characteristics
- Line build outs of 0dB, -7.5dB, and -15dB
- Companion to the DS2291 T1 Long Loop Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION
The DS2290 T1 Isolation Stik provides all the surge and isolation protection that is necessary to connect a piece of equipment to a T1 line. It offers a function similar to that provided by a Data Access Arrangement (DAA) when a modem is connected to a phone line. The DS2290 is FCC Part 68 pre-registered so the user can connect equipment to T1 lines without any further testing or qualification. It contains onboard waveshaping circuitry that creates transmit pulses meeting the latest T1 specifications including TR 62411 (Accunet* T1.5 Service Description and Interface Specifications, - December 1988) and T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). Applications include Channel Service Units and similar equipment that requires a fully protected interface.

* Service mark of AT&T Communications

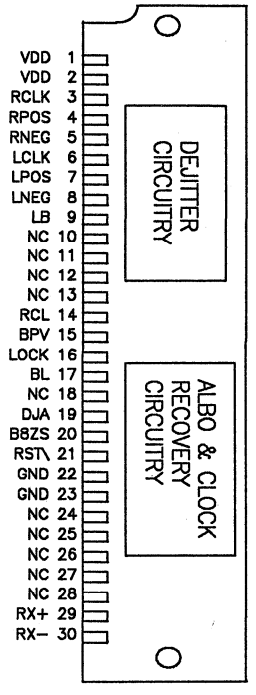
DALLAS SEMICONDUCTOR

DS2291
T1 Long Loop Stik

FEATURES

- Recovers clock and data off of T1 lines from 0 to 6000 feet in length
- +0 to -30dBSX receive sensitivity
- Built-in Automatic Line Build Out (ALBO) circuitry; no tuning or external components required
- Dejitters the recovered clock and data
- Meets TR 62411 for jitter tolerance and attenuation
- Companion to the DS2290 T1 Isolation Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION

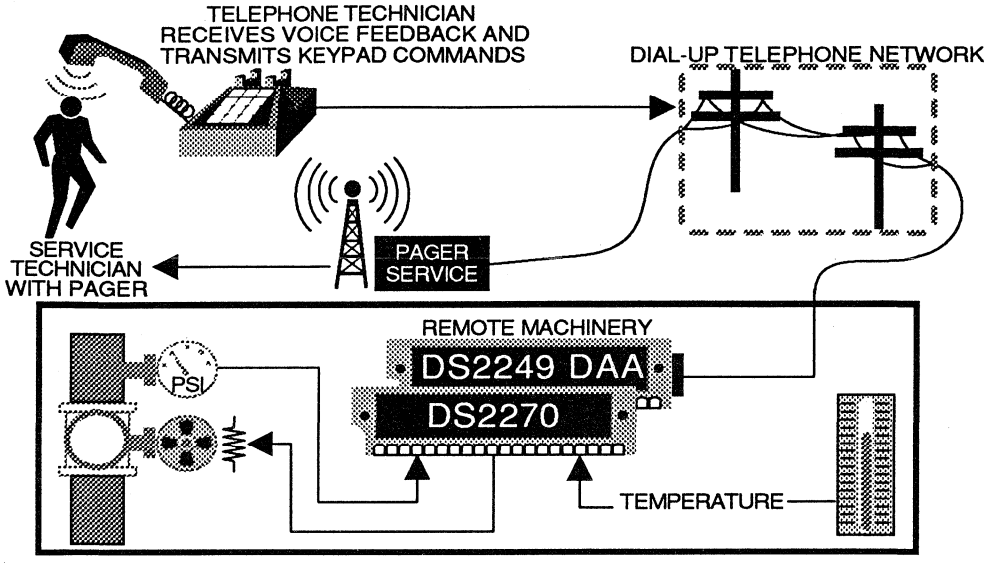
The DS2291 T1 Long Loop Stik contains all the circuitry necessary to recover clock and data off a T1 line. The DS2291 contains an Automatic Line Build Out (ALBO) circuit that allows it to adapt to T1 lines varying in length from 0 to 6000 feet. It will also dejitter the recovered clock and data according the jitter attenuation curves outlined in AT&T Communications Document TR 62411 (Accunet* T1.5 Service Description and Interface Specification, - December 1988). Applications include Channel Service Units (CSUs), T1 monitoring equipment, and T1 test equipment.

* Service marks of AT&T Communications

Teleservicing

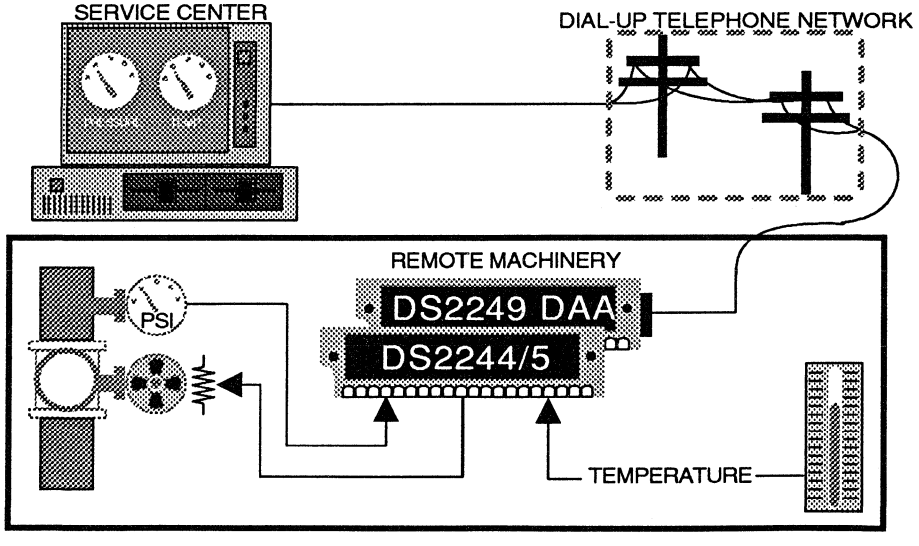
The following Teleservicing datasheets, with the exception of the DS1360 Phantom DAA Chip, are one-page overviews. For complete datasheets, please refer to the Dallas Semiconductor Teleservicing Data Book.

TELESERVICING WITH FIELD TECHNICIAN



A machine fitted with Teleservicing Stiks can automatically call a pager service to notify a repairman when equipment malfunctions. When the repairman goes to the phone, the machine annunciates what the problem is.

TELESERVICING WITH DESKTOP PC



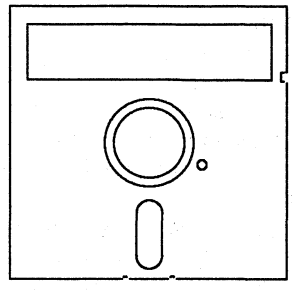
Data can be formatted graphically on a desktop PC to display machine performance. The PC maintains a history file to aid troubleshooting.

DALLAS SEMICONDUCTOR

DS0010
Teleservicing Toolbox 1.0 Software

FEATURES

- Transforms a desktop PC into an automated service manager
- Communicates with teleservicing components via the global dial-up phone network
- Requires a Hayes-compatible 2400 or 1200 bps modem
- Distributes remote embedded software updates electronically
- Toolbox utilities include:
  - Downloading of Intel Hex programs
  - Automatic error detection/correction
  - Unassembly of HEX to ASM utility
  - Editing of remote code or memory
  - Autodialing routines
  - Password identification
  - Batch command file creation
- Compatible with Dallas Semiconductor teleservicing components:
  - DS2245 Soft Modem Stik
  - DS2244 TeleMicro Stik
  - DS2230 Dual Port NV SRAM Stik
  - DS6070K TeleMicro Kit
  - DS6071K TeleMemory Kit
- Includes a terminal emulator for basic communication



DESCRIPTION

The DS0010 Teleservicing Toolbox software runs on an IBM PC or compatible and helps to supervise a network of remote teleservicing sites using normal dial-up phone lines. The main feature of the DS0010 is its ability to automatically distribute new software updates to remote systems that use embedded Dallas Semiconductor Teleservicing products. Electronic distribution of software updates for embedded processors eliminates the cost and inconvenience associated with the physical replacement of EPROM program memory. The DS0010 can automatically dial out to teleservicing sites with a user-provided Hayes-compatible modem, establish a data connection, download a system software update, and verify its integrity. Data can also be uploaded to the DS0010 from Teleservicing site. This data may represent remote system performance that the DS0010 can then archive on the PC hard disk to create a service history for future troubleshooting and repair.

In order to use the DS0010 software, remote sites must employ Dallas Semiconductor's teleservicing products. For example, the DS2245 Soft Modem Stik is a modem that, in addition to its normal communication functions, can also reload the nonvolatile program/data memory of a DS5000 Soft Microcontroller. The DS0010 Teleservicing Toolbox can be used to call the remote site, establish a modem connection with the DS2245, issue user-specified passwords, and then reload the new program code into the remote DS5000.

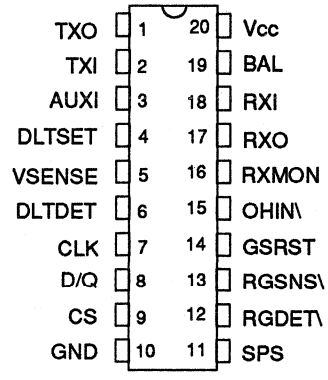
DALLAS SEMICONDUCTOR

DS1360/S
Phantom DAA Chip

FEATURES

- Single-chip DAA controller for:
  - Modems
  - Speech interfaces
  - FAX machines and boards
- Phantom operation reports loop current changes back to host
- Allows the DAA to use an existing phone line unobtrusively
- Transmit/receive interface connects directly to 600 ohm modem coupling transformers
- On-chip electronic 2- to 4-wire converter
- Integrates FCC Part 68 DAA requirements:
  - Ring detection
  - 2 second billing delay
  - Transmit power limiter
- Onboard low-pass filtering of transmit and receive signals
- Voice/data switching
- Software-controlled receive gain
- 3-wire serial control port
- +5 Volt single-supply operation
- DS1360S surface mount version available

PIN DESCRIPTION



DS1360 20-Pin DIP
(300 Mil.)

DESCRIPTION

The DS1360 Phantom DAA chip is a CMOS device that integrates FCC requirements for interfacing data and voice to the telephone network. The DS1360 meets FCC Part 68 specifications such as 2-second billing delay, transmit signal power limiting, and ringing detection. It also offers programmable transmit and receive gains and an on-chip 2- to 4-wire converter (hybrid). By adding a coupling transformer, a relay, and an optocoupler, a complete DAA circuit can be quickly designed.

A unique feature of the DS1360 is its ability to sense loop current using an on-chip 8-bit A/D converter. By using a external DC-biased optocoupler (for proper isolation), the phone loop current can be digitized and monitored through the serial port by a host processor. The DS1360 can also be programmed by external resistors to report when the current has changed by a certain percentage. Loop current sensing is important for monitoring the activity of extension phones or for determining loop length for cable compensation.

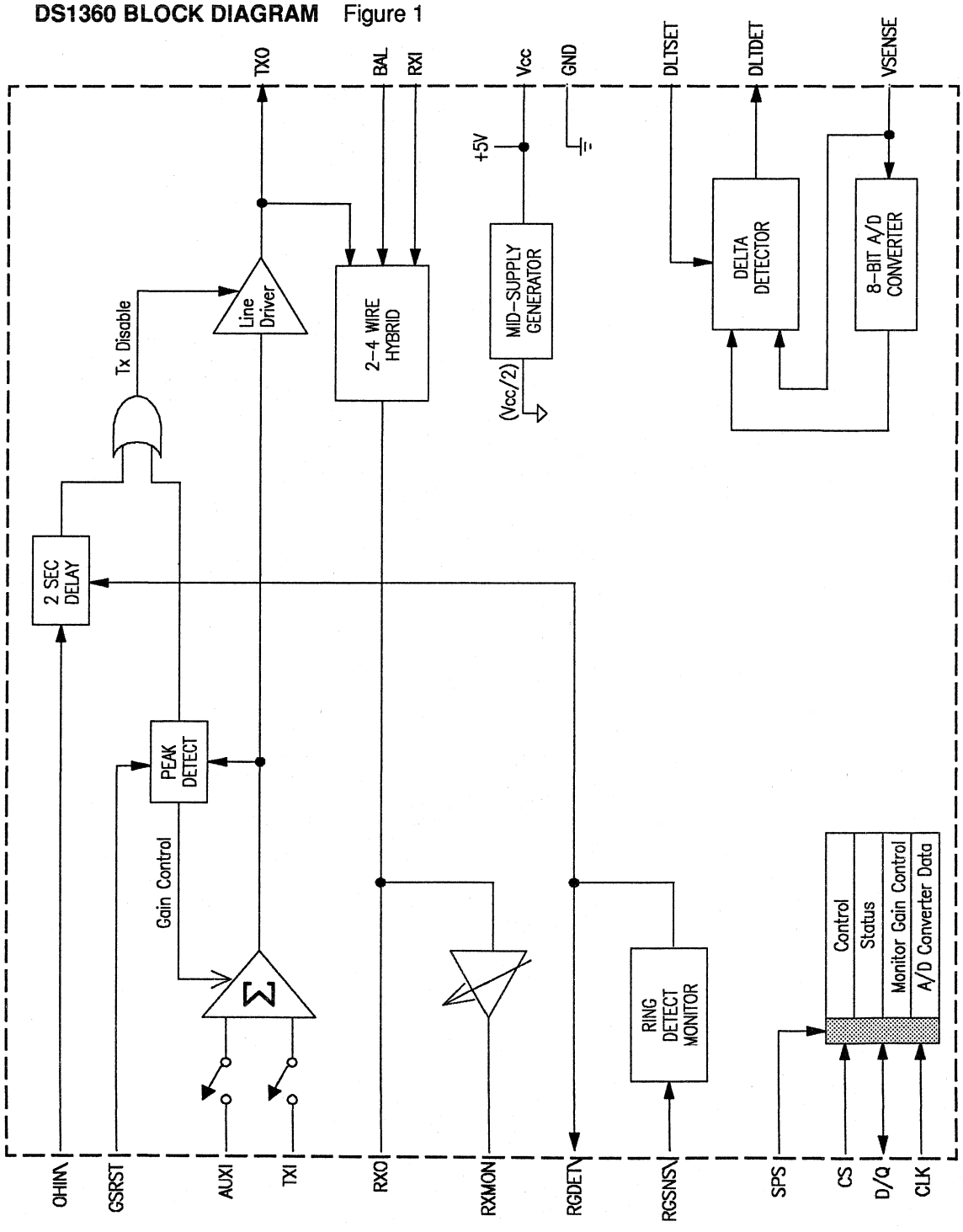
PIN DESCRIPTION Table 1 (\ Denotes Condition Low)

PIN	SYM	TYPE	DESCRIPTION
1	TXO	O	**Transmit Output.** This is the transmit output which is the sum of the signals at AUXI and TXI (minus any attenuation needed to prevent excessive power transmission). This output can be connected to a telephone coupling transformer through an appropriate line matching resistor (typically 600 ohms).
2	TXI	I	**Transmit Input.** This is the transmit analog signal input which can be AC-coupled to any low-impedance source such as a modem chip output or an op-amp. The transmit limiter circuit will gradually attenuate the sum of the TXI and AUXI signals until the level output at TXO is less than 0.5 Vrms. If the sum of TXI and AUXI is less than 0.5 Vrms, then no adjustment is made. If more than 10 dB of attenuation is required, the TXO output is disabled until GSRST is toggled or power is cycled. This input is also controlled by the Control Register in the software mode.
3	AUXI	I	**Auxiliary Input.** An auxiliary analog signal may be fed here to be summed with the TXI analog signal before transmission to the phone line. This input is controlled by the Control Register in the software mode. The auxiliary input operates identically to the TXI input with regard to signal limiting and gain.
4	DLTSET	I	**Delta Voltage Set.** This pin is used in conjunction with the VSENSE pin in programming the voltage percentage at which the delta detector trips (DLTDET goes high).
5	VSENSE	I	**Voltage Sense In.** This is the input to the A/D converter which is used for the delta detector circuit or for digitizing low-frequency signals in general.
6	DLTDET	O	**Delta Detect Out.** This output goes high when the voltage at VSENSE has changed by more than a percentage as determined by external resistors. The operation of the delta detect circuit is controlled by the Control Register in the software mode.
7	CLK	I	**Serial Clock In.** This input is used to clock serial port data in and out of the D/Q pin. The maximum clock

			frequency is 4 MHz. When SPS=0, this pin is used in conjunction with CS to program the RXMON gain.
8	D/Q	I/O	**Serial Port Data I/O.** This pin is used for transferring data to or from the serial port registers. Input data is sampled on rising edges of CLK; output data is updated on falling edges of CLK. When SPS=0, resampling of the DLTSET input is initiated by a rising edge at D/Q.
9	CS	I	**Chip Select Input.** This input should transition high to initiate serial port read or write operation. Returning CS to a logic 0 terminates a serial port operation. When SPS=0, this pin is used in conjunction with CLK to program theRXMON gain.
10	GND	--	**Ground.** This pin should be tied to system ground (0 volts).
11	SPS	I	**Serial Port Select.** This pin should be tied high in order to use the software mode; otherwise tie this pin low for the hardware mode. The function of pins D/Q, CS, and CLK are affected by this input.
12	RGDET\	O	**Ring Detect Out.** This open-drain output goes active low whenever a proper ring signal is detected at the RGSNS\ input. Otherwise, this pin will go to a high-impedance state unless pulled up by an external resistor to the V_{CC} supply.
13	RGSNS\	I	**Ring Sense In.** This pin can be connected to the output of an optocoupled ring detect circuit. The Ring Detect circuit in the DS1360 will integrate the signal at RGSNS\ over the 20 Hz ring cycles to present a continuous logic 0 at RGDET\ that lasts for the duration of the ring burst (typically 2 seconds in the U.S.).
14	GSRST	I	**Gain Setting Reset.** When this input is at a logic 1, the gain settings for the transmit limiter circuit are reset to their default state. The limiter circuit begins adjusting the transmit level at TXO (only if the level is too high) when this pin returns low. The limiter gain settings are also reset upon power-up. This pin should only be used to transmit DTMF signals at a

			level higher than the normal -9 dBm limit specified for voice and data.
15	OHIN\	I	**Off-Hook In.** This input should be connected to the off-hook relay signal from the host system. When this input transitions low, the TXO output is disabled (forced to mid-supply) for at least 2 seconds only if a ring signal was detected within the last 8 seconds. Otherwise, the TXO output is enabled except when the TXDIS bit = 1 or if in the power-down mode.
16	RXMON	O	**Receive Monitor Out.** This is a buffered, gain-selectable version of the receive hybrid output. The gain from RXI to RXMON is programmed using the Receive Monitor Gain Register. This signal can be routed to an external speaker amplifier or a handset for audio monitoring of the receive signal. The load impedance should be $\geq$ 5K ohms.
17	RXO	O	**Receive Out.** The receive output of the hybrid is present at this pin. The gain from the RXI input to RXO is 1.5 dB (to make up for the loss through a typical coupling transformer). The load impedance should be $\geq$ 5K ohms.
18	RXI	I	**Receive In.** This is the receive input to the internal hybrid circuit.
19	BAL	--	**Balance Network.** An optional balance network can be attached at this pin for adjusting the return loss of the hybrid. Normally, this pin should be left floating if not used.
20	Vcc	--	**Positive Supply In.** Tie this pin to +5 Volts.

DS1360 BLOCK DIAGRAM Figure 1



OVERVIEW

The DS1360 Phantom DAA (Data Access Arrangement) Chip is a CMOS monolithic device that integrates many of the functions required by FCC for interfacing voice and data to the telephone network. By adding a coupling transformer, an optocoupler, and an off-hook relay, an FCC Part 68-compatible DAA circuit can be quickly designed. Although the final system must still be tested and certified by an FCC approved testing lab, the DS1360 greatly reduces the design time as well as the component cost and board space for implementing the DAA function. A block diagram of the DS1360 is shown in Figure 1.

An integral 2- to 4-wire converter or hybrid circuit isolates transmit and receive signals for use with a telephone coupling transformer. The transmit output is specifically designed to drive telephone line impedances with low distortion using a single +5 volt supply. Voice and data signals can be multiplexed under software control to feed the transmit output. Automatic power limiting and a 2-second billing delay are included in the transmit path in order to meet FCC Part 68 requirements.

The receive section of the DS1360 is split into two paths. One path feeds the RXO output which is normally connected to the input of a modem or FAX device. The other path is routed to a gain-programmable op-amp which then feeds the RXMON output. This output can be used to drive an external speaker or handset, although it to can also be used with modem devices.

The ring detection circuit can take the raw output of an external optocoupled ring sensor and process it into a glitchless square wave that corresponds to the ring burst duty cycle. Ring detection is reported at both the RGDET\ pin and in the Status Register.

An on-board 8-bit analog-to-digital (A/D) converter is used to digitize and process external low-frequency signals such as loop current, receive power level, or analog sensor outputs. Conversion samples are accessible through the serial port. The conversion time is typically 80 usec. The DS1360 also includes a Delta Detector circuit that optionally reports when the input signal to the A/D converter has changed by a certain percentage.

Control of the DS1360 is accomplished using either the software or hardware modes. In the hardware mode (SPS = 0), device operation is controlled by tying certain pins high or low. The software mode (SPS = 1) uses a 3-wire serial interface for accessing internal registers. These registers provide control and monitoring information for use by a external microcontroller or microprocessor.

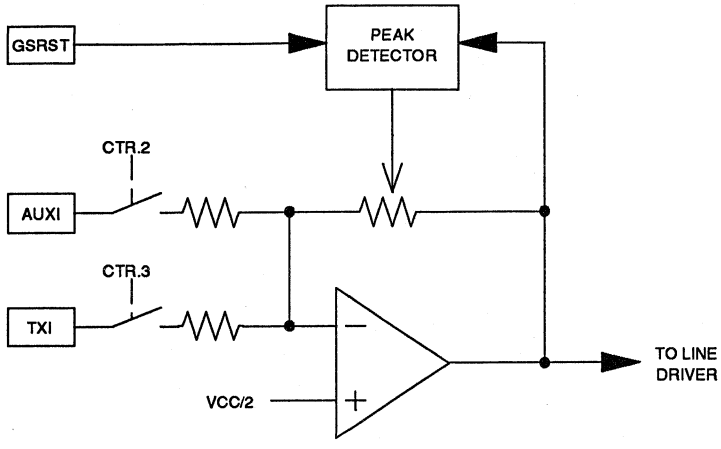
A power-down mode is included for reducing power dissipation in low-power applications. The power-down mode is controlled by the PD bit in the Control Register. The power-down mode is exited by either clearing the PD bit or by a high-to-low transition on RGSNS\.

TRANSMIT INPUT

A block diagram of the the transmit input circuitry is shown Figure 2. The analog signals at AUXI and TXI are summed together and sent on to the line driver unless disabled by bits CTR.2 and CTR.3 in the Control Register. These bits can be used as a mux for switching between voice and data when using the software mode (SPS = 1). In the hardware mode, AUXI and TXI are always enabled and switching must be done externally.

The peak detector circuit continuously samples the output of the input summing op-amp to determine if the level is too high. Signals routed on to the line driver must be less than -4dBm (0.5 Vrms) to meet FCC Part 68 limits for maximum transmission level (the line driver itself has unity gain). If the level to the line driver is higher than

TRANSMIT INPUT SECTION Figure 2



-4 dBm, the peak detector begins to attenuate the signal until it is in compliance (adjustment is only in the direction of increasing loss). The attenuation range is 10 dB; if more than 10 dB of loss is needed, the peak detector will disable the signal path to the line driver. Once the attenuation has reached a stable setting, it can only be reset by either taking GSRST high or by cycling the power. Taking GSRST high resets the attenuation setting back to 0 dB (no loss), effectively disabling the signal limiting function for as long as GSRST is high. The peak detector returns to normal operation once GSRST goes low again.

The GSRST input may also be taken high to transmit DTMF tones at the higher level of +2 dBm, resulting in -4 dBm on the telephone line. Part 68 permits a level of 0 dBm maximum for DTMF tone transmission. Once the DTMF digits have been sent, GSRST should be returned low to limit normal data transmission levels to -4 dBm maximum at the TXO output. Improvements in transmission quality throughout the telephone network has greatly reduced the need to transmit at such higher levels; therefore using GSRST in this manner is usually not necessary.

The attenuation steps are as follows: 0, -0.25, -0.5, -1.0, -2.0, -3.0, -6.0, -10.0, and infinite (signal path disabled). The initial steps are gradual to permit transmission near the maximum of -4 dBm at TXO. The limit of -4 dBm was chosen since the matching resistor to the telephone line will normally introduce another 6 dB of loss. Therefore, the resulting power on the line will be -10 dBm which is 1 dB less than the maximum level allowed by Part 68 of -9 dBm for data signals. The 1 dB margin is necessary for variations in the absolute accuracy of the peak detector due to changes in process, temperature, and supply voltage. The peak detector steps through the attenuation values until a level less than -4 dBm is reached.

It is important to note that the peak detector monitors and attenuates the sum of TXI and AUXI. If TXI and AUXI are both enabled and their respective signal levels are at -6 dBm, the sum may exceed -4 dBm which will cause the

peak detector to introduce the appropriate amount of attenuation.

BILLING DELAY

An on-chip billing delay circuit is provided to meet Part 68 requirements to provide the network adequate time for billing information before modem data is sent. The billing delay is nominally set to 2.25 seconds, well within the 2 seconds required. The billing delay timer is triggered by a negative transition on OHIN\ which causes the TXO output to be squelched for at least 2 seconds. Afterwards, the TXO output begins to respond to signals at the TXI and AUXI inputs as described previously.

The billing delay only operates when going off-hook in answer to a ring signal. Specifically, if a ring burst has not been received in the 8 seconds preceding OHIN\ going low, the billing delay is unused and TXO is enabled immediately. This permits the host system to go off-hook when needing to immediately dial a number. It is then the responsibility of the answering modem to provide a 2-second delay before sending data.

TRANSMIT LINE DRIVER

The transmit line driver takes the output of the input summing op-amp and buffers it to TXO pin. Normally, TXO would be connected through a line matching resistor to a telephone coupling transformer. The resulting impedance attached to TXO is the matching resistor plus the telephone line impedance -- typically 1.2K ohms (600 + 600 = 1.2K ohms). The line driver will actually drive up to 600 ohms without significant distortion up to the point of clipping. Clipping typically occurs when the signal at TXO is within 0.25 volt of either power supply rail.

The line driver also removes extraneous high-frequency signals using a 1-pole low-pass filter with a break point at 12 KHz. This filter attenuates the clock switching noise that modem devices typically add to the modulated data signal as well as any coupled noise from the power supply. A typical clock switching frequency of 128 KHz would be attenuated by 20 dB before transmission out to TXO. A spectrum analyzer should be used to look at the TXO output to check that attenuation of out-of-band signals conforms to Part 68 requirements. Typically, the internal low-pass filter provides adequate attenuation.

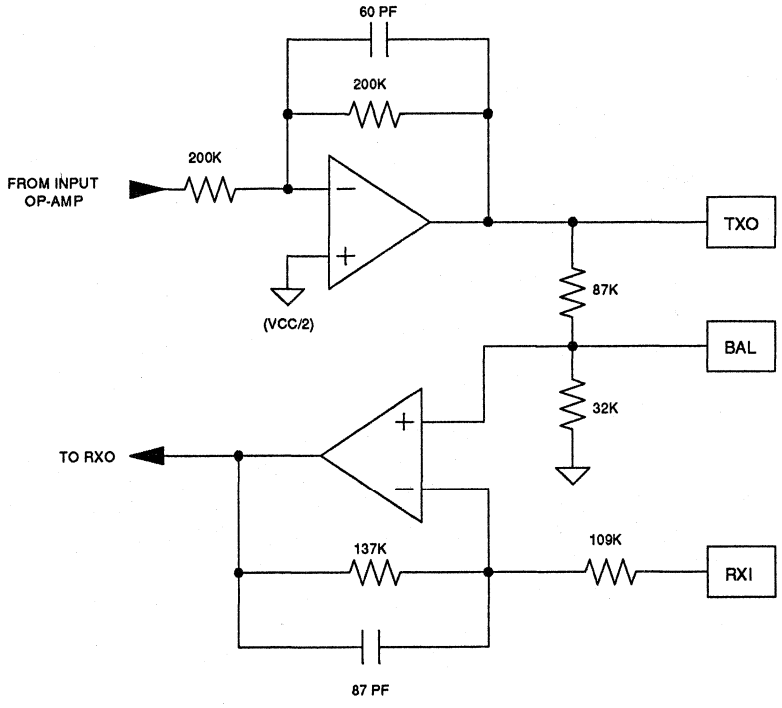
The TXO output has a DC offset of $V_{cc}/2$ volts (2.5 volts if Vcc = 5 volts) and usually should be AC-coupled with a capacitor when connecting to a transformer. Typically one leg of the transformer is hooked to ground which means that TXO would have to drive 2.5 volts into the large DC load of the line matching resistor if not AC-coupled. A value of 1 uF or more is usually adequate; lower values may introduce in-band attenuation of the transmit and receive signals. If a low impedance mid-supply is available in the system, then it may be tied to the transformer in lieu of ground. In that case, the coupling capacitor is not needed.

When the power-down mode is entered (PD=1 in the Control Register), the TXO output is tri-stated to help conserve power. Note that the off-hook relay should disconnect the phone line connection when using the power-down mode since the TXO output is now in a high-impedance state (i.e., the reflected impedance back to the line is no longer 600 ohms).

2- to 4-WIRE HYBRID

The internal electronic 2- to 4-wire hybrid circuit splits the signal to/from the telephone line into separate transmit and receive signals. As illustrated in Figure 3, the hybrid consists of an op-amp which sums a portion of the TXO signal with the signal at RXI which is usually tied to the external coupling transformer. The receive gain from RXI to the output of the hybrid is about 1.5 dB to make up for the typical insertion loss of a coupling transformer. The hybrid assumes that

TRANSMIT DRIVER/ RECEIVE HYBRID SECTION Figure 3



the TXO component at RXI will be 6 dB lower than that at the TXO pin. As a result, the sum of the TXO signal through the inverting and non-inverting gain paths of the hybrid op-amp is theoretically 0, which means that only the receive signal from the other end of phone line should be present at the hybrid output (RXO). However, due to variations in the phone line impedances, the signal at RXI varies in phase and amplitude from the the ideal case; consequently the TXO component is not completely cancelled by the hybrid. Typically, the return loss (the loss of the transmit signal through the hybrid) varies from 10 to 16 dB.

The return loss of the hybrid can be adjusted by an external compensation network attached to the BAL pin. External balancing is optional and in most cases the user can simply float this pin. The amplitude and phase of the signal routed to the non-inverting terminal of the hybrid op-amp can be programmed using external resistors and capacitors. When using external resistors make sure to use values low enough to swamp out the internal resistor divider.

Another way to balance the hybrid is to change the external line matching resistor (nominally 600 ohms) until the TXO component at RXI is exactly 6 dB lower than at TXO. Phase compensation may be added by tying a capacitor from either TXO or GND to the BAL pin. *Note that the absolute values of the internal resistors connected to the BAL vary ± 20% while their ratio varies only ± 0.1%.*

The output of the hybrid is sent on to the RXO pin and to a programmable gain op-amp which feeds the RXMON pin. RXO and RXMON are both designed to drive ≥ 5K ohm loads.

RECEIVE MONITOR OUTPUT

The RXMON output is a gain-programmable version of the signal at RXO (RXMON is also 180 degrees out of phase with RXO). In the software mode, the gain from the hybrid output to RXMON can be programmed using the Receive Monitor Gain register. As shown in Table 4, eleven gain values ranging from +9.0 to -21 dB can be selected. An additional value (OFF) can be used to completely mute the RXMON output. This might be useful when using the DS1360 with a handset for voice/data switching. RXMON can also be connected to a speaker buffer amp for use with a monitor speaker. A monitor speaker is normally included in Hayes™ compatible modems; the AT command set in such modems specifies programmable speaker levels which can be easily implemented using RXMON.

In the hardware mode (SPS = 0), the gain for RXMON is programmed by using the CS and CLK multifunction pins. The 4 gain values supported are shown below:

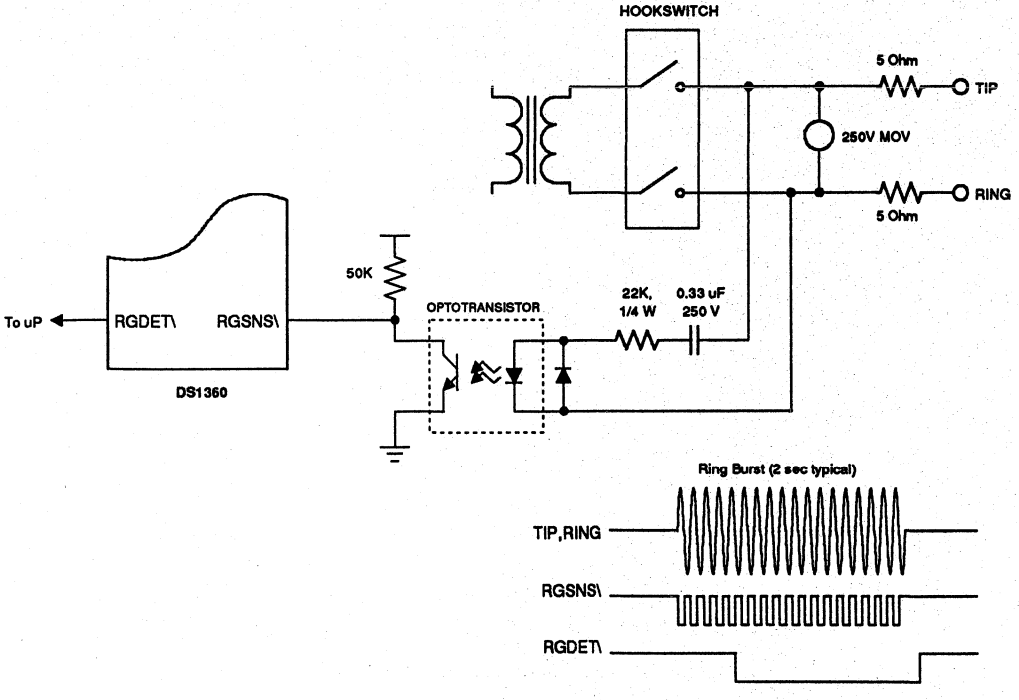
HARDWARE MODE GAIN Table 2

CS	CLK	Gain (dB)
0	0	+6.0
0	1	0.0
1	0	- 6.0
1	1	off

RING DETECTION

Ring detection can be accomplished using the RGSNS\ and RGDET\ pins with an external optocoupler sensor circuit (see Figure 4). The RGSNS\ input digitally integrates low-going

RING DETECTION OPERATION Figure 4



pulses output from a ring sensing optocoupler. The integrated signal is then fed to the RGDET\ output which goes to a logic 0 when a valid ring signal has been received at RGSNS\. RGDET\ is an open-drain output and should be pulled up by an external resistor to define the off-state (logic 1). The RGDET\ state is also reported by the Status Register in the software mode; each ring occurrence is latched by the RGDET bit; a read operation of this register clears the RGDET bit until the next valid detection of a ring burst.

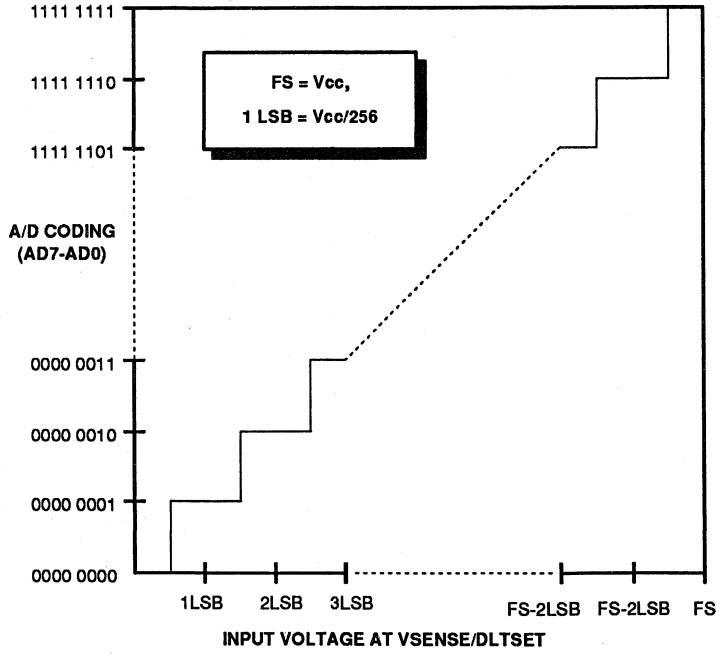
Ringing on the telephone line can be 15 to 68 Hz in frequency and 40 to 150 Vrms in amplitude. The task of the ring sensor circuit is to provide the RGSNS\ pin with low pulses corresponding to the ring signal exceeding some voltage threshold. Figure 4 shows a recommended circuit which provides the ring sensing as well as the 1000 Vrms isolation required by Part 68. The final processed ring detect signal is presented at RGDET\ which can then be used by a microprocessor. This circuit in Figure 4 also presents an on-hook AC impedance that complies with Part 68.

Low-going signals at RGSNS\ also cause the DS1360 to exit the power-down mode. The purpose of this feature is to allow a ring signal to wake up a system that is in a low-power state. Once powered-up, the DS1360 internally clears the PD bit in the Control Register.

A/D CONVERTER OPERATION

The DS1360 includes an 8-bit linear A/D converter for use with low-frequency and DC signals. The converter can sample either the VSENSE or DLTSET inputs, depending upon the mode the DS1360 is in. The result of the A/D conversion is placed in the A/D Data Register (ADR) which can be read through the serial

A/D CONVERTER TRANSFER FUNCTION Figure 5



port. The coding for the 8-bit data sample is shown in Figure 5.

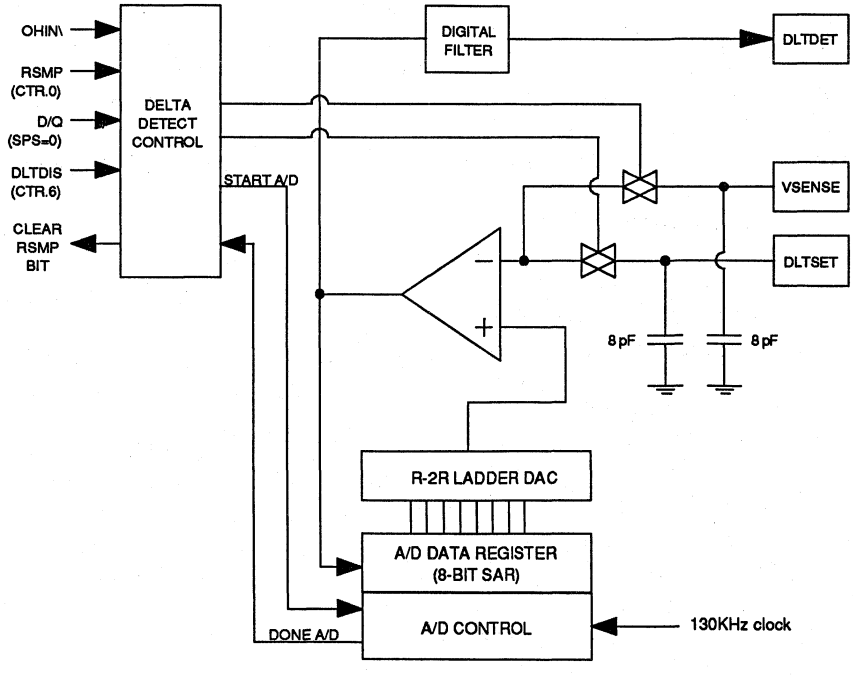
Input signals at VSENSE or DLTSET may be anywhere in the range from GND to Vcc; each step of the A/D converter is then Vcc/256 volts. For a typical Vcc = +5V, the A/D converter can resolve down to 20 mV. The absolute accuracy of the converter is entirely dependent upon Vcc; no internal reference is used. Signals connected to VSENSE should use the Vcc supply so that the changes in Vcc will not affect the A/D conversion accuracy. The input impedance is typically 8 pF to ground (GND).

The converter architecture uses a successive-approximation register (SAR) approach with an R-2R ladder DAC. This approach lends itself to quick conversion times (80 usec typically) with excellent accuracy and linearity. The converter does not include a sample-and-hold stage since the intended use is with slowly varying or DC signals (this does not preclude the use of an external sample and hold circuit). The clocking for the conversion process is derived from an internal 130 KHz oscillator that is also used for the billing delay timing.

DELTA DETECTOR

The delta detector is for use in a phantom modem by sensing changes in the DC loop current. Loop current sensing is important for detecting when extension devices on the telephone line go off-hook. For example, the DS1360 could be used in a FAX or modem application to know when the telephone handset was picked up. A teleservicing application can use the phantom feature to non-intrusively borrow the phone line when it is free and to release it when someone picks up an extension phone set.

DELTA DETECTOR SCHEMATIC Figure 6



In the hardware mode (SPS = 0), the delta detect circuit reports changes in the voltage at VSENSE using the A/D converter. In this mode, the signal at DLTSET is automatically sampled 250 msec after each falling edge at OHIN\; this sample is stored in the R-2R DAC and then continuously compared to the voltage at VSENSE. When the voltage at VSENSE is lower than the old sample of DLTSET, the DLTDET pin transitions to a logic 1. DLTDET stays high until the DLTDET input goes back to a higher voltage or when OHIN\ goes high. To resample DLTSET after the automatic sample is taken, the D/Q pin can be used. A rising edge at D/Q in the hardware mode causes a new sample to be taken of DLTSET.

A resistor divider can be placed between the VSENSE and DLTSET inputs to program where the DLTDET triggers. For example, to detect a 50% change at VSENSE, both resistors of the divider should be equal. Figure 6 illustrates the operation of the delta detector.

In the software mode, the delta detector can be controlled using the DLTDIS bit in the Control Register. When DLTDIS = 1, the delta detector circuit is disabled (DLTDET is forced to a 0). An 8-bit A/D conversion of the signal on the VSENSE pin is initiated by setting the RSMP bit to a 1; when the conversion is complete, this bit is automatically cleared internally (the host can poll this bit to see when the conversion is done). Each conversion result is written into the ADR register which can then be retrieved by the host.

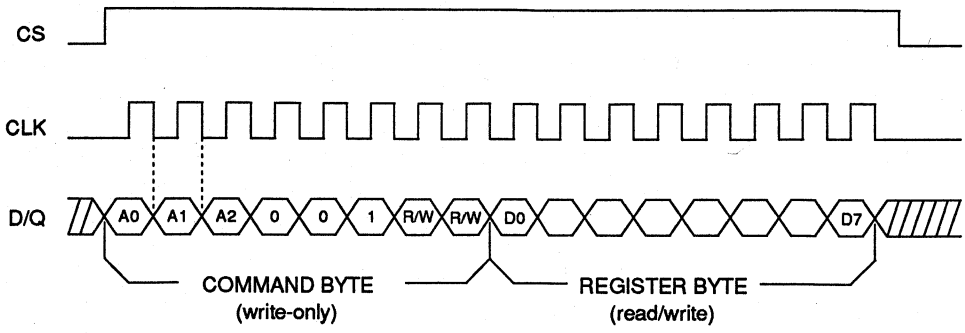
If the DLTDIS = 0, the delta detector is enabled and a sample of the DLTSET input is automatically taken after each high-to-low transition at OHIN\ (just as in the hardware mode). Setting the RSMP bit high in this mode initiates resampling of the DLTSET signal (not VSENSE) which is then continuously compared to the VSENSE signal. The DLTSET samples are stored in the ADR register. The DLTDET output can be used as an interrupt to alert the host microprocessor of voltage changes as an alternative to polling of the serial port.

SERIAL PORT OPERATION

The serial control port of the DS1360 consists of 3 pins: CS, CLK, and D/Q. These 3 signals provide synchronous access of internal control and status registers. To use the serial port, the DS1360 must be placed in the software mode by tying the SPS (Serial Port Select) pin high. The host can then access the internal registers by transferring a 2-byte sequence; the first byte is write-only and provides command and register address information, while the second byte is the actual register data that is either read or written by the host. Data bytes to/from the DS1360 are always transferred LSB first. The serial port can be operated at any time even when the DS1360 is in the power-down mode. As shown in Figure 7, a serial port operation is initiated by first taking CS (Chip Select) high. The host then clocks in the command byte using a clock supplied to the CLK pin. Data written to the D/Q pin is sampled on rising edges of CLK. The first 3 bits indicate register address information, the next 3 bits device selection bits, and the last 2 bits the type of operation (read or write). There are 4 registers available for host use.

The next 8 clock cycles at CLK transfer data into or out of a particular register within the DS1360. For a write operation, the DS1360 samples data at D/Q on rising clock edges; for a read operation, data at D/Q is updated on falling clock edges. Note that for a read operation the DS1360 will drive the D/Q line after the eighth falling edge of CLK. Once the last bit has been transferred, the CS line should be taken low to terminate the operation.

SERIAL PORT OPERATION[1] Figure 7



1. Command and register bytes are always read/written LSB first.

REGISTER ADDRESSES Table 3

REGISTER	ADDRESS[1] (A2,A1,A0)
CONTROL REGISTER	000
STATUS REGISTER	001
RECEIVE MONITOR GAIN	010
A/D DATA REGISTER	011

1. Address values 100 through 111 should are used for factory test and should never be used.

REGISTER POWER-ON DEFAULT VALUES Table 4

REGISTER	VALUE
CTR	0000 0100 (AUXI input disabled)
STR	0000 0000
RMR	1111 1111 (RXMON off)
ADR	0000 0000

COMMAND BYTE (Write-Only) Table 5

R/W	R/W	1	0	0	A2	A1	A0
(MSB)							(LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
R/W	CB.7	Determines read or write operation.
R/W	CB.6	00 = write operation 11 = read operation 10,10 = undefined
1	CB.5	Device select bits.
0	CB.4	
0	CB.3	
A2	CB.2	MSB of Register Address
A1	CB.1	
A0	CB.0	LSB of Device Address

CONTROL REGISTER (Read/Write) Table 6

0	TXODIS	DLTDIS	PD	TXE	AUXE	RSTPK	RSMP
(MSB)							(LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
0	CTR.7	Unused; must be zero for proper operation.
TXODIS	CTR.6	Three-states TXO output and disconnects TXO from the internal hybrid. 0 = normal operation 1 = TXO high-impedance
DLTDIS	CTR.5	Delta Detect Disable. 0 = Delta detector enabled 1 = Delta detector disabled This bit is used to disable the operation of the delta detector circuit. The 8-bit A/D converter continues to operate in response to sample requests via the RSMP bit.

PD	**CTR.4**	Power Down control. 0 = normal operation 1 = power down When this bit is set to a 1, the DS1360 enters a low power mode. All analog outputs (TXO, RXO, and RXMON) are disabled and the internal processing clock is halted. Power-Down mode is exited by either: 1) the PD bit being cleared by software or a power-up on Vcc or 2) a falling edge on the RGSNS\ pin.
TXDIS	**CTR.3**	Transmit input signal enable. 0 = TXI signal path enabled 1 = TXI signal path disabled
AUXDIS	**CTR.2**	Auxiliary input signal enable. 0 = AUXI signal path enabled 1 = AUXI signal path disabled
RSTPK	**CTR.1**	Reset transmit signal limiter peak detector. 0 = normal operation 1 = peak detector in reset state This bit must be cleared by the host to a 0 for proper operation of the transmit limiter function; otherwise, the transmit signal will pass through unattentuated.
RSMP	**CTR.0**	Resample signal present at VSENSE or DLTSET pin. 0 = normal operation 1 = take new sample (cleared internally) The 8-bit sample is stored in the the ADR register which can be read by the host. This bit is cleared internally after ADR is loaded with a new sample. RSMP resamples the VSENSE pin when DLTDIS=1 and the DLTSET pin when DLTDIS=0.

STATUS REGISTER (read only) Table 7

1	1	1	1	TXSQU	TXLVL	DLDET	RGDET

(MSB) (LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
1	STR.7	Unused.
1	STR.6	Unused.
1	STR.5	Unused.
1	STR.4	Unused.
TXSQU	STR.3	Transmit output squelched due to excessive signal power. 0 = TXO output active 1 = TXO output squelched This bit latches to a 1 whenever the transmit attenuator is at its maximum loss. At this time, the transmit output (TXO) is squelched until GSRST or RSTPK is toggled.
TXLVL	STR.2	Transmit level adjustment. 0 = no level adjustment made 1 = level adjustment made This bit latches to a 1 whenever the transmit peak detector has forced the transmit signal limiter to increase its loss by a step. A read of the Status Register clears this bit.
DLDET	STR.1	Delta detect at VSENSE pin. 0 = no delta change detected 1 = delta change detected This bit latches to a 1 whenever the voltage at VSENSE changes by the a certain percentage (see "DELTA DETECTOR" section). A read of the Status Register clears this bit unless the condition still exists.
RGDET	STR.0	Ring detect. 0 = no ringing detected 1 = ring burst detected This bit latches to a 1 when a valid ring signal has been received at RGSNS\ (also indicated by the RGDET\ pin going low). A read of the

Status Register clears this bit until the next valid ring burst.

RECEIVE MONITOR GAIN (Read/Write)[1] Table 8

0	0	0	0	G3	G2	G1	G0

(MSB) (LSB)

SYMBOL	POSITION	NAME AND DESCRIPTION
0	**RMR.7**	Unused.
0	**RMR.6**	Unused.
0	**RMR.5**	Unused.
0	**RMR.4**	Unused.
G3-G0	**RMR.3-0**	Receive monitor output gain. These bits select the amount of gain from the output of the internal hybrid to the RXMON output. The mapping of these bits is shown below.

1. Unused bits RMR.7-RMR.4 will read back as 1's; however, it is recommended that these bits always be written as 0's to maintain compatibility with future options.

RECEIVE MONITOR GAIN MAPPING Table 9

G3 - G0	GAIN/LOSS
0000	+ 9.0 dB
0001	+ 6.0
0010	+ 3.0
0011	0.0
0100	- 3.0
0101	- 6.0
0110	- 9.0
0111	- 12.0
1000	- 15.0
1001	- 18.0
1010	- 21.0
1011-1111	OFF[1]

1. The OFF selection means that the RXMON output is forced to low-impedance mid-supply. It is also recommended that the 1111 selection be used for turning RXMON off since selections 1010-1110 may be used for additional gain settings on future versions of the DS1360.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0° C to +70° C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{cc}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{CC}	4.5		5.5	V	3

CAPACITANCE

(t_A= +25° C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS

(0° C to +70° C; V_{cc}=5V ±10%)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CCA}		5		mA	1
Power-Down Supply Current	I_{CCPD}		1	5	uA	2
Input Leakage	I_{ILK}	-1.0		+1.0	uA	
Output Leakage	I_{OLK}	-1.0		+1.0	uA	
Output Current (@2.4V)	I_{OH}	-1.0			mA	
Output Current (@0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. Analog outputs unloaded.
2. PD bit = 1 (CTR.4).
3. Decouple with 10uF and 0.1uF capacitors.

TRANSMIT ANALOG CHARACTERISTICS (0° C to -70° C; Vcc = +5V ± 10%)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Input AC Impedance (AUXI, TXI)		10.0		Kohms	1
Input Level Before TXO Squelched (GSRST=0)		± 2.00		Vpk	2
Input Level Before Clipping (GSRST=1)		± 2.25		Vpk	2
TXO Billing Delay		2.25	2.1	sec	3
TXO Output Level		0.475	0.540	Vrms	2
Transmit Attenuator Range (Before TXO squelched)	10			dB	2
TXO Harmonic Distortion			-55	dB	4
TXO Output Offset Voltage		± 50		mV	
Output AC Impedance (TXO)		25		Ohms	1

NOTES:

1. Vtest = sine wave, 0.25 Vrms, @ 1 KHz.
2. Vtest = sine wave @ 1 KHz. Squelched refers to TXO being disabled.
3. Measured from falling edge of OHIN\. Ring must have been detected in previous 8 seconds.
4. TXO load = 600 ohms. TXI or AUXI = sine wave, 0.25 Vrms, 1 KHz.

RECEIVE ANALOG CHARACTERISTICS (0° C to 70° C; Vcc = +5V ±10%)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Input AC Impedance (RXI)		110		Kohms	1
Input Level Before Clipping (RXI)		± 2.0		Vpk	2
Output Offset Voltage (RXO, RXMON)		± 50		mV	
Ring Detect Delay		100		msec	3

NOTES:
1. Vtest = sine wave, 0.707 Vrms, @ 1 KHz.
2. Clipping observed at RXO.
3. RGSNS\ = 20 Hz square wave.

A/D CONVERTER CHARACTERISTICS (0° C to 70° C; Vcc = +5V ±10%)

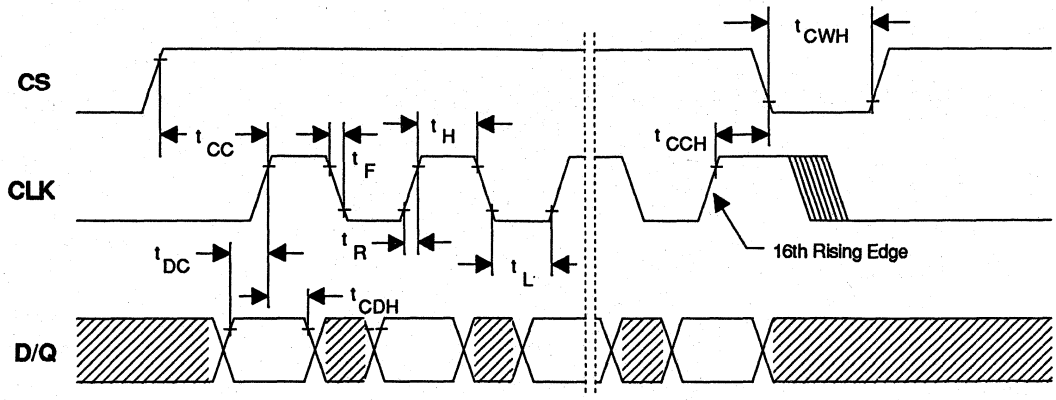
PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Input AC Impedance (DLTSET, VSENSE)		500		Kohms	
Input Voltage Range (DLTSET, VSENSE)	0.0		Vcc	V	
Total Conversion Error			± 1	LSB	
Conversion Time		80		usec	

SERIAL PORT TIMING CHARACTERISTICS (0° C to +70° C; V_{cc}=5V ±10%)

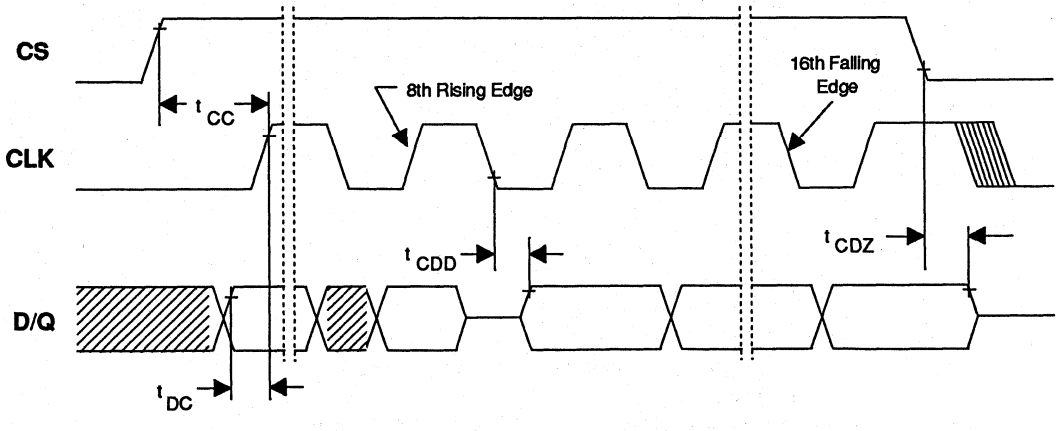
PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
D/Q to CLK Set-Up	t_{DC}	35			ns	1
CLK to D/Q Hold	t_{CDH}	40			ns	1
CLK Low Time	t_{CL}	125			ns	1
CLK High Time	t_{CH}	125			ns	1
CLK Rise and Fall Times	t_R, t_F			100	ns	1
CS to CLK Set-Up	t_{CC}	250			ns	1
CLK to CS Hold	t_{CCH}	40			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
CLK to D/Q Delay	t_{CDD}			75	ns	1
CS to D/Q High Z	t_{CDZ}					

NOTES:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.

SERIAL PORT TIMING -- WRITE REGISTER OPERATION Figure 8



SERIAL PORT TIMING -- READ REGISTER OPERATION Figure 9



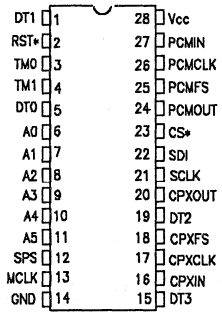
DALLAS SEMICONDUCTOR

DS2130
Voice Messaging Processor Chip

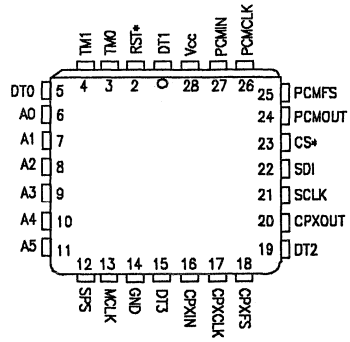
FEATURES

- Per-channel voice messaging processor for digitized voice storage and retrieval
- High fidelity speech recording and playback at 8, 12, 16, 24, and 32 Kbits/sec
- Integral DTMF transceiver for remote touch tone control and dialing
- Connects to popular PCM codec/filters for analog interfacing
- Direct PCM serial data bus interfaces to any of 32 possible TDM time slots
- Monitors and reports audio energy levels for call progress and voice detection
- Selectable beep generator for sound prompts
- 3-wire synchronous serial control port
- 28-pin DIP or PLCC (DS2130Q) packages

PIN CONNECTIONS



DS2130 28-Pin DIP



DS2130Q 28-Pin PLCC

DESCRIPTION

The DS2130 Voice Messaging Processor is a CMOS digital signal processor (DSP) that serves as a voice messaging engine for digitized voice storage and retrieval applications. It offers half-duplex speech compression or expansion at either 16, 24, or 32 Kbps; lower rates are available with reduced bandwidth. The advanced speech compression algorithm maintains excellent audio clarity even at low bit rates. The algorithm also incorporates a DTMF transceiver for decoding or generating touch tone signals for remote control and automatic dialing. The tone generator can be used to create single-tone beeps used in answering machines. Voice and call progress detection can be easily implemented using the energy threshold detect outputs.

The DS2130 can be used together with a low-cost codec/filter device for analog interfacing in stand-alone applications such as answering machines or feature phones. It can also interface directly to a serial PCM bus on any of up to 32 possible time slots using an internal software-selectable time slot assigner circuit (TSAC). This configuration can be used in digital switching systems for adding voice messaging services to existing backplane designs.

Applications include digital answering machines, embedded voice response, speech annunciators, voice mail, key telephone systems, and automatic operator services.

DALLAS SEMICONDUCTOR

DS2244T
TeleMicro Stik

FEATURES
- Embedded 8-bit controller subsystem with integral 1200/2400 bps modem
- Can be reprogrammed for customer-specific applications using 8051 instruction set
- Comes installed with basic AT compatible command set
- Up to 32Kx8 of onboard read/write nonvolatile program/data memory for use by application software
- Full-duplex asynchronous/synchronous serial interface
- Onboard real-time clock (RTC) with alarm wake-up output
- 21 customizable I/O port pins for dedicated system control and monitoring
- Bell 212A/103 and CCITT V.22 bis/V.22/V.21 compatible versions available
- Call progress detection
- DTMF generation and detection
- Low-power CMOS operation at +5 volts
- 10 year RTC operation and program/data memory nonvolatility
- Mates with JEDEC-standard 30-pin SIMM connectors (right angle and vertical)

PIN DESCRIPTION
(\ Denotes Condition Low)

NAME	PIN	NAME	PIN
P0.0	20	T1	1
P0.1	22	TXD	2
P0.2	23	RXD/T0	18
P0.3	24	RD\	15
P0.4	25	WR\	16
P0.5	26	ALE	17
P0.6	27	OH\	3
P0.7	29	RI\	4
P2.0	5	INT0\	19
CD\ (P2.1)	6	PROG\	30
DSR\ (P2.2)	7	AIN	21
CTS\ (P2.3)	8	AOUT	28
DTR\ (P2.4)	9	V_{CC}	12
RTS\ (P2.5)	10	GND	14
P2.6	13		
P2.7	11		

STANDARD PART NUMBERS
DS2244T-12U	1200bps, RTC, US only, 8Kx8 NVSRAM
DS2244T-24	2400bps, RTC, US&Europe, 32Kx8 NVSRAM

DESCRIPTION
The DS2244T TeleMicro Stik is an embedded 8-bit microcontroller subsystem that includes a Bell/CCITT compatible 1200 or 2400 bps modem, a DTMF receiver, a DS5000FP Micro Chip, a real-time clock/calendar, and up to 32Kx8 of nonvolatile read/write program or data memory. The microcontroller offers 21 I/O port pins for dedicated system control or monitoring. Peripheral devices such as A/D converters, keypads, and LCD displays may be memory-mapped onto the I/O ports. The DS2244T may be used with the DS2249 DAA Stik for directly connecting to dial-up telephone lines. A high-performance intelligent terminal with advanced communication features can be quickly designed by adding an LCD display, a keypad, and a power source.

The DS2244T is intended for applications in which the system intelligence is the embedded application software. As such, AT commands are installed within the DS2244T primarily for evaluation purposes. Reprogramming of the DS2244T is accomplished using the asynchronous serial load mode of the DS5000FP Micro Chip. More information is provided in the 1990 Teleservicing Design Handbook.

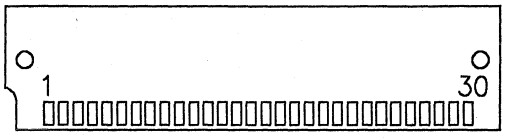
DALLAS SEMICONDUCTOR

DS2245
Soft Modem Stik

FEATURES

- Reprogrammable, +5V modem subsystem available in 1200 or 2400 bps versions
- User-transferable FCC modem registration when used with DS2249 DAA Stik
- Bell 212A/103 and CCITT V.22 bis/22/21-compatible versions available
- Parallel interface connects to PC/XT/AT bus
- Implements Hayes AT command set
- User-defined I/O port for remote control of external system
- "Softness" allows program upgrades without hardware modifications
- Interprets DTMF signals
- Employs popular JEDEC standard 30-pin SIMM connection scheme

PIN DESCRIPTION



SIP Stik

ORDERING INFORMATION:

DS2245-12U	-1200 bps, U.S. only
DS2245-12	-1200 bps, U.S. & Europe
DS2245-24	- 2400 bps, U.S. & Europe, 2K x 8 NVRAM

DESCRIPTION

The DS2245 Soft Modem Stik is a microcommunication subsystem that, in conjunction with the DS2249 DAA Stik, forms a complete 2400/1200/300 bps modem that can be directly connected to the public switched telephone network. Included in the DS2245 is all the modulation/demodulation and filtering circuitry necessary for compatibility with Bell 212A/103 and CCITT V.22 bis/V.22/21 type modems. Embedded software responds to the industry standard Hayes AT command set for modem control. The parallel interface can connect directly to a PC/XT/AT bus or to any other general-purpose bus architecture.

Special features of this modem family include nonvolatile data archiving, DTMF tone detection, a user-defined I/O port that can be accessed by the remote modem, and a "soft" reload function that permits the user to install program updates without hardware changes.

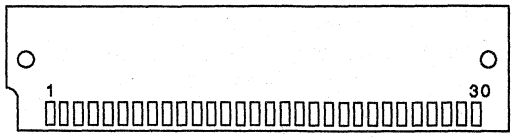
Applications include laptop computers, debit card terminals, pay telephones, or any other system requiring communication over the public telephone network. More information is available in the 1990 Teleservicing Design Handbook.

DALLAS SEMICONDUCTOR

DS2249
Data Access Arrangement (DAA) Stik

FEATURES
- Interfaces voice/data to the public switched telephone network
- FCC Part -68 compatible
  - 1000 Vrms isolation
  - 800 volt surge protection
- User-transferable FCC modem registration when used with DS2245 Soft Modem Stik
- Employs popular JEDEC standard 30-pin SIMM connection scheme
- Single +5 volt supply operation
- Ring detection
- 2- to 4-wire converter
- Audio monitor output

PIN CONNECTIONS



SIP Stik

PIN NAMES (\ Denotes Condition Low)

1	- OH\
2	- AUDIO
3	- TXA
4	- RXA
5-9	- NC
10	- Vcc
11	- GND
12	- RI\
13-26	- NC
27	- RINGO
28	- TIPO
29	- RING
30	- TIP

DESCRIPTION
The DS2249 Data Access Arrangement (DAA) Stik is designed to connect directly to the public switched telephone network through an appropriate mechanical connector such as an RJ11 jack. It is FCC Part 68 -registered when used with the DS2245 Soft Modem Stik as a complete modem meeting hazardous voltage, surge, and leakage current specifications. The DS2249 is easily registered with other voice/data circuitry as long as output level and billing protection requirements for the resulting system are satisfied at an FCC testing laboratory.

Included in the DS2249 is a ring detect output and a 2- to 4-wire converter for use with modem components such as the DS2245. It operates from a single +5V supply and uses CMOS circuitry for low power consumption.

Applications include laptop computers, remote data collection, pay phones, or any application where data or voice needs to be sent over the telephone network.

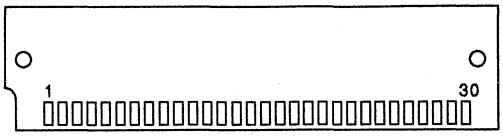
More information is available in the Teleservicing Design Handbook.

DALLAS SEMICONDUCTOR

DS2249PH
Phantom DAA Stik

FEATURES
- Interfaces voice/data to the public switched telephone network
- Phantom operation senses DC loop current and reports changes back to host
- Allows unobtrusive access to existing phone lines
- Onboard 8-bit A/D converter
- Programmable receive gain
- Meets FCC Part 68 DAA requirements:
  - 1000 Vrms isolation
  - 800 Volt surge protection
  - 2 second billing delay
  - Output power limiting
- User-transferable FCC Part 68 DP registration
- Transmit and receive high-frequency noise filters
- Ring detection
- 2- to 4- wire converter with tunable return loss
- Audio monitor output
- Low-power sleep mode
- Mates with popular JEDEC standard 30-pin SIMM connectors (vertical and right angle)
- Single +5 volt supply operation

PIN CONNECTIONS



SipStik

DESCRIPTION
The DS2249PH Phantom DAA Stik is a Data Access Arrangement designed to connect directly to the public switched telephone network (through an appropriate mechanical connector such as an RJ11C jack). It is FCC Part 68 DP registered, meeting hazardous voltage, surge, and leakage current specifications. The DS2249PH achieves phantom operation by sensing the DC loop current on the phone line and reporting changes back to the host. This enables an external modem to cease data transmission when an extension phone is picked up, thereby borrowing existing phones non-intrusively.

Included in the DS2249PH is a ring detect output and a 2- to 4-wire converter for use with modem components such as the DS2245 Soft Modem Stik or the DS2244T TeleMicro Stik. It operates from a single +5V supply and uses CMOS circuitry for low power consumption.

Applications include laptop computers, FAX boards, remote data collection, pay phones, or any application where data or voice needs to be sent over the telephone network.

The Phantom feature is especially suited to teleservicing remote equipment, thus avoiding the cost of dedicated phone lines.

DALLAS SEMICONDUCTOR

DS2270/E
Speech Recorder Stik

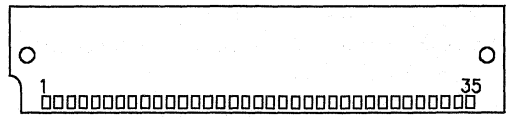
FEATURES

- Solid-state audio recording/reproducing subsystem with DTMF detection/generation
- 50 seconds of recording capacity at 8 Kbps, expandable with external memory
- Selectable record and playback rates from 8 to 32 Kbps
- Uses ADPCM compression/expansion algorithms for high fidelity record/playback
- Digital audio level monitoring
- Instant random-access playback of recorded messages
- Programmable input/output gain for optimum record/playback levels
- Nonvolatile SRAM retains speech data for 10 years (DS2270 only)
- Mates with JEDEC-standard 35-pin SIMM connectors (right angle and vertical)

DESCRIPTION

The DS2270 Speech Recorder Stik is a complete solid-state audio recording/reproducing subsystem that replaces mechanical tape-based recording for embedded applications. An advanced audio compression/expansion DSP engine provides excellent playback quality even at low bit rates. Selectable compression bit rates permit the user to trade off audio fidelity against storage capacity. Gains for the audio input and outputs are software programmable for providing optimum record and playback levels. DTMF detection and generation is also available under software control.

PIN CONNECTIONS



ORDERING INFORMATION

DS2270	64Kx8 onboard SRAM; expandable with external memory.
DS2270E	8Kx8 onboard program SRAM; all speech memory provided externally by user.

A synchronous 3-wire serial interface provides the means for external control by a host microcontroller such as the DS5000 Soft Microcontroller. Speech data can also be loaded or retrieved through this port.

The DS2270 comes standard with 64Kx8 of nonvolatile SRAM which provides up to 50 seconds of speech capacity at a bit rate of 8 Kbps. Additional external memory can be easily attached for increasing the recording time capacity. The DS2270E is a lower-cost version without onboard speech RAM; the user supplies memory using the serial expansion memory port.

DALLAS SEMICONDUCTOR

DS6070K
TeleMicro Kit

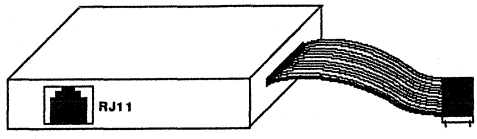
FEATURES

- Retrofit kit for teleservicing existing 8031/ 8051 microcontroller designs
- Enables electronic reloading of application programs via dial-up phone lines
- Internal Hayes-compatible 1200 bps modem
- FCC Part 68 pre-registered
- Connects to 40-pin DS5000/8051 socket with a ribbon cable
- Eurocard box includes teleservicing SIP Stiks:
  - DS2249 Data Access Arrangement (DAA) Stik
  - DS2245-12U Soft Modem Stik
  - DS2259T Time Micro Stik
- DS2259T features:
  - 32K x 8 nonvolatile program/data RAM
  - Real-time clock/calendar
  - 32 programmable I/O lines
  - Bytewide address and data bus
  - 100% 8051 instruction set-compatible
- Includes DS0010 Teleservicing Toolbox 1.0 software for communication from a remote IBM PC
- Direct RJ11 connection to telephone line
- +5 volt operation from ribbon cable

DESCRIPTION

The DS6070K TeleMicro Kit is a retrofit kit for teleservicing existing 8051-based designs. The TeleMicro Kit instantly retrofits any 40-pin 8051 socket with a DS2259T Time Micro Stik and an embedded Hayes-compatible 1200 bps modem. The modem permits remote reloading of 8051 application code using the Intel Hex file format. A remote PC equipped with a Hayes-compatible 1200 bps modem can dial into the TeleMicro Kit, establish a modem connection, and then with special commands reload the DS2259T's 32K x 8 nonvolatile program/data memory. Also included is a demonstration version of the DS0010 Teleservicing Toolbox software which runs on an IBM PC, XT, AT, or compatible and manages the downloading/ uploading of data to/ from a remotely located TeleMicro Kit.

PACKAGE OUTLINE



The DS6070K consists of a plastic Eurocard-sized box containing three Dallas Semiconductor Stiks: the DS2249 DAA, the DS2245-12U 1200 bps Soft Modem Stik, and the DS2259T Time Micro Stik. An RJ11 telephone jack can be directly connected to the phone line. A flat ribbon cable terminates into a 40-pin DIP plug which should be mated with a 40-pin 80C51 socket. All power for the DS6070K is derived from the +5 volts at pin 40 of the socket.

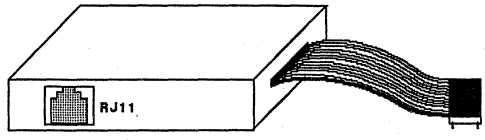
DALLAS SEMICONDUCTOR

DS6071K
TeleMemory Kit

FEATURES

- Retrofit kit for teleservicing a bytewide memory socket
- Enables electronic distribution of software updates by using normal dial-up phone lines
- Provides remote system monitoring and control
- Eurocard box includes teleservicing SIP Stiks:
  - DS2249 Data Access Arrangement (DAA) Stik
  - DS2245-12U Soft Modem Stik
  - DS2230 Dual Port NV SRAM Stik
- Includes DS0010 Teleservicing Toolbox 1.0 software for communication from a remote IBM PC
- Retrofits existing bytewide sockets with 32K x 8 of reloadable nonvolatile memory
- Nonvolatile memory can be uploaded/ downloaded via internal 1200 bps modem
- Resets outputs for halting external processor operation when reloading memory
- Powered from +5V of the bytewide socket
- Direct RJ11 connection to telephone line
- Status LED indicators

PACKAGE OUTLINE



DESCRIPTION

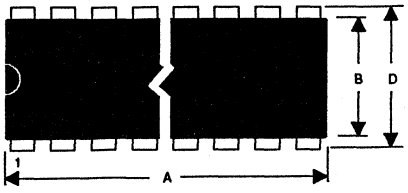
The DS6071K TeleMemory Kit is a retrofit kit for teleservicing bytewide sockets. The TeleMemory Kit instantly retrofits any 28-pin bytewide memory socket in a host system with 32K x 8 of nonvolatile SRAM. The memory offered by the DS6071K can be used by the host system for either program code or data as with normal ROM or RAM devices; all 32K x 8 of memory can subsequently be uploaded or downloaded from a remote IBM PC using the internal 1200 bps modem (consisting of the DS2245 Soft Modem and DS2249 DAA Stiks).

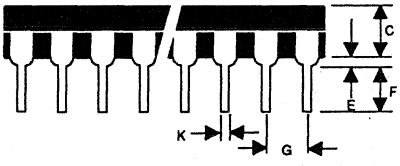
A remote PC equipped with a Hayes-compatible modem can dial the TeleMemory, establish a modem connection, and, with special commands, reload the 32K x 8 nonvolatile memory with new program code or data information. Reset outputs are available for patching into the system reset signal for halting processor operation during reload sessions. Also included is a demonstration version of the DS0010 Teleservicing Toolbox software which runs on an IBM PC, XT, AT, or compatible and manages the uploading/downloading of data to and from a remotely located TeleMemory Kit.

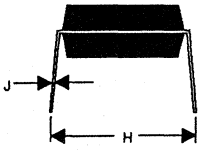
Packages

DUAL IN-LINE PACKAGES

8- to 24-Pin (300 mil)

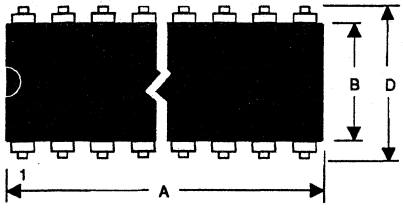


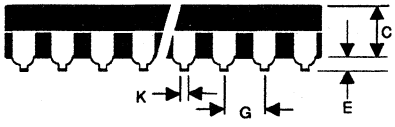


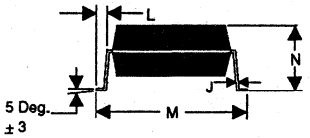


PKG	8-PIN		10-PIN		14-PIN		16-PIN		18-PIN		20-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.345	0.400	0.480	0.520	0.740	0.780	0.740	0.780	0.860	0.940	0.960	1.040	1.150	1.260
MM	8.76	10.16	12.19	13.21	18.80	19.81	18.80	19.81	21.84	23.88	24.38	26.42	29.21	32.00
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.290	0.310	0.290	0.310	0.290	0.310	0.290	0.310	0.290	0.310	0.290	0.310	0.290	0.310
MM	7.37	7.87	7.37	7.87	7.37	7.87	7.37	7.87	7.37	7.87	7.37	7.87	7.37	7.87
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.110	0.130	0.110	0.130	0.110	0.130	0.110	0.130	0.110	0.130	0.110	0.130	0.110	0.130
MM	2.79	3.30	2.79	3.30	2.79	3.30	2.79	3.30	2.79	3.30	2.79	3.30	2.79	3.30
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN.	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

DUAL IN-LINE PACKAGES
8- to 20-Pin Gullwing (300 mil)

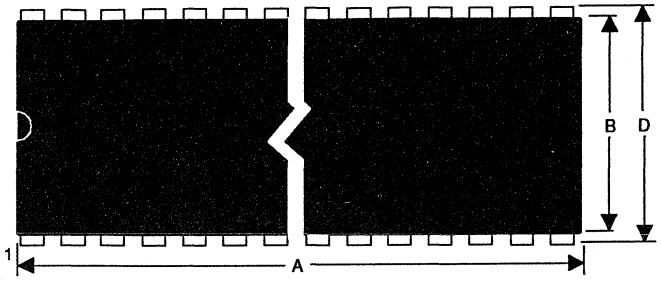


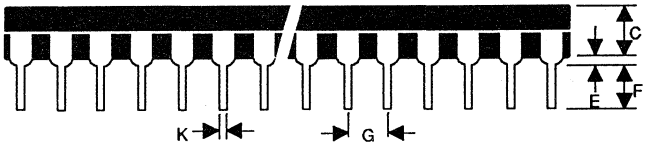


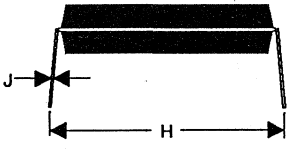


PKG	8-PIN		14-PIN		16-PIN		20-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.345	0.400	0.740	0.780	0.740	0.780	0.960	1.040
MM	8.76	10.16	12.19	13.20	18.79	9.81	24.38	26.41
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.290	0.310	0.290	0.310	0.290	0.310	0.290	0.310
MM	7.34	7.87	7.34	7.87	7.34	7.87	7.34	7.87
E IN.	0.020	0. 040	0.020	0. 040	0.020	0. 040	0.020	0. 040
MM	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02
F IN.	0.110	0.130	0.110	0.130	0.110	0.130	0.110	0.130
MM	2.79	3.30	2.79	3.30	2.79	3.30	2.79	3.30
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN.	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53
L IN.	0.040	0.060	0.040	0.060	0.040	0.060	0.040	0.060
MM	1.02	1.52	1.02	1.52	1.02	1.52	1.02	1.52
M IN.	0.370	0.420	0.370	0.420	0.370	0.420	0.370	0.420
MM	9.40	10.67	9.40	10.67	9.40	10.67	9.40	10.67
N IN.	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180
MM	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57

DUAL IN-LINE PACKAGES
24- to 40-Pin (600 mil)

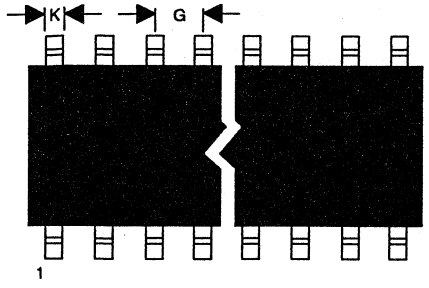


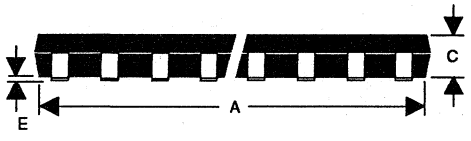


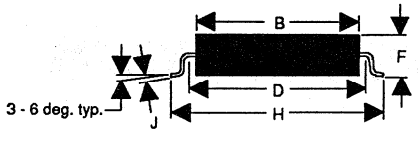


PKG	24-PIN		28-PIN		32-PIN		40-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	1.220	1.260	1.440	1.460	1.640	1.660	2.040	2.060
MM	30.99	32.00	30.99	32.00	30.99	32.00	30.99	32.00
B IN.	0.540	0.560	0.540	0.560	0.540	0.560	0.540	0.560
MM	13.72	14.22	13.72	14.22	13.72	14.22	13.72	14.22
C IN.	0.140	0.160	0.140	0.160	0.140	0.160	0.140	0.160
MM	3.56	4.06	3.56	4.06	3.56	4.06	3.56	4.06
D IN.	0.590	0.625	0.590	0.625	0.590	0.625	0.590	0.625
MM	14.99	15.88	14.99	15.88	14.99	15.88	14.99	15.88
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.380	1.02	0.380	1.02	0.380	1.02	0.380	1.02
F IN.	0.110	0.135	0.110	0.135	0.110	0.135	0.110	0.135
MM	2.79	3.43	2.79	3.43	2.79	3.43	2.79	3.43
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN.	0.625	0.675	0.625	0.675	0.625	0.675	0.625	0.675
MM	15.88	17.15	15.88	17.15	15.88	17.15	15.88	17.15
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

SMALL OUTLINE ICs
8- and 16-Pin (150 mil)

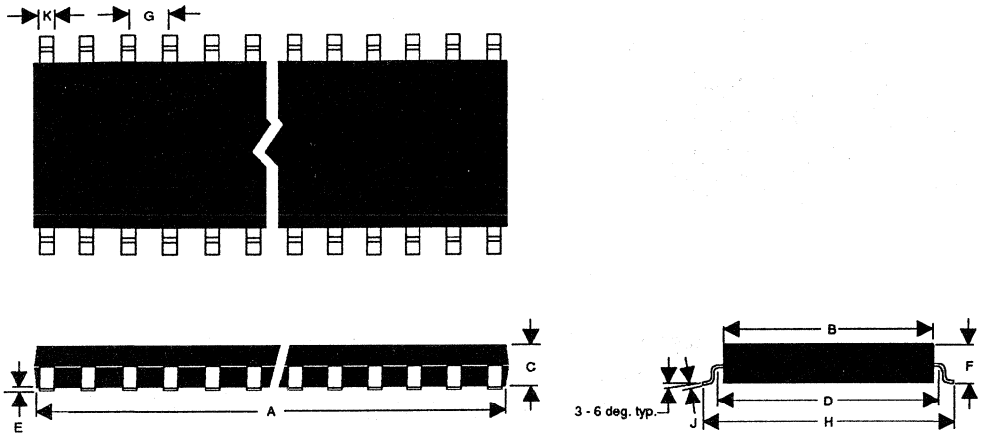






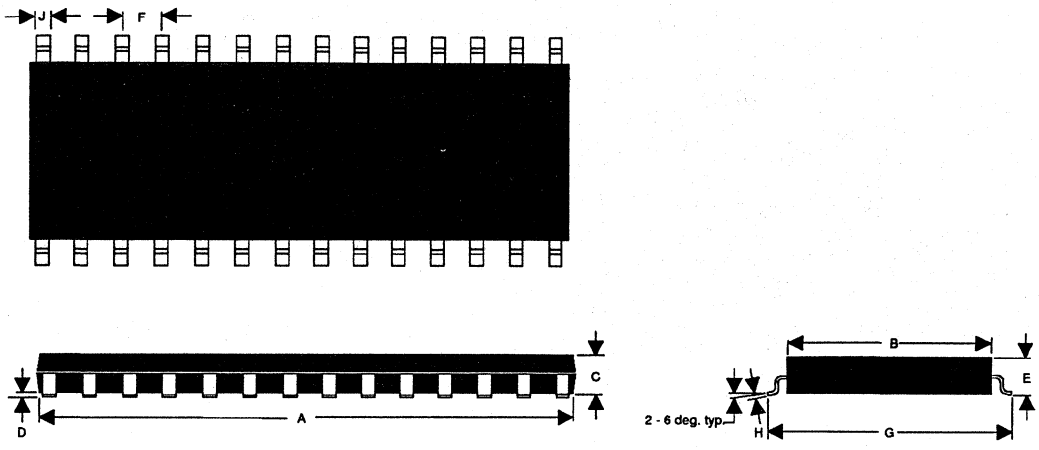
PKG	8-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.188	0.195	0.386	0.393
MM	4.78	4.95	9.80	9.98
B IN.	0.151	0.157	0.151	0.157
MM	3.84	3.99	3.84	3.99
C IN.	0.052	0.061	0.052	0.061
MM	1.32	1.55	1.32	1.55
D IN.	0.175	0.193	0.175	0.193
MM	4.45	4.90	4.45	4.90
E IN.	0.004	0.010	0.004	0.010
MM	0.10	0.25	0.10	0.25
F IN.	0.058	0.068	0.058	0.068
MM	1.47	1.73	1.47	1.73
G IN.	0.046	0.054	0.046	0.054
MM	1.17	1.37	1.17	1.37
H IN.	0.228	0.244	0.228	0.244
MM	5.79	6.20	5.79	6.20
J IN.	0.006	0.011	0.006	0.011
MM	0.15	0.28	0.15	0.28
K IN.	0.013	0.019	0.013	0.019
MM	0.33	0.48	0.33	0.48

SMALL OUTLINE ICs
16-, 20- and 24-Pin (300 mil)



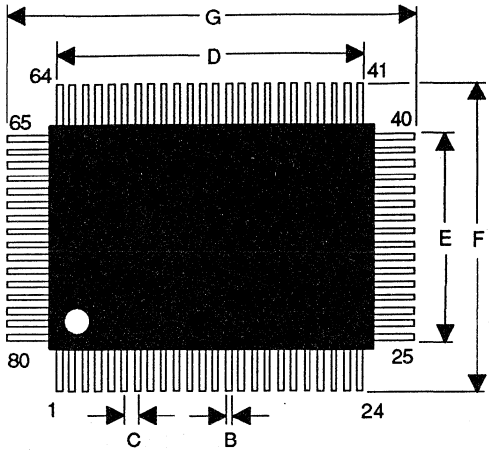
PKG	16-PIN		20-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.402	0.412	0.500	0.511	0.602	0.612
MM	10.21	10.46	12.70	12.99	15.29	15.54
B IN.	0.290	0.300	0.290	0.300	0.290	0.300
MM	7.37	7.62	7.37	7.62	7.37	7.62
C IN.	0.089	0.095	0.089	0.095	0.089	0.095
MM	2.26	2.41	2.26	2.41	2.26	2.41
D IN.	0.325	0.330	0.325	0.330	0.325	0.330
MM	8.26	8.38	8.26	8.38	8.26	8.38
E IN.	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30
F IN.	0.097	0.105	0.097	0.105	0.097	0.105
MM	2.46	2.68	2.46	2.68	2.46	2.68
G IN.	0.046	0.054	0.046	0.054	0.046	0.054
MM	1.17	1.37	1.17	1.37	1.17	1.37
H IN.	0.400	0.410	0.400	0.410	0.400	0.410
MM	10.16	10.41	10.16	10.41	10.16	10.41
J IN.	0.006	0.011	0.006	0.011	0.006	0.011
MM	0.152	0.28	0.152	0.28	0.152	0.28
K IN.	0.013	0.019	0.013	0.019	0.013	0.019
MM	0.33	0.48	0.33	0.48	0.33	0.48

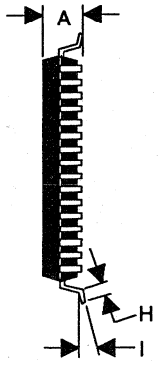
SMALL OUTLINE ICs
28-Pin (330 mil)



DIM	MIN	MAX
A IN.	0.716	0.736
MM	18.19	18.69
B IN.	0.330	0.350
MM	8.38	8.89
C IN.	0.090	0.100
MM	2.29	2.54
D IN.	0.008	0.012
MM	0.20	0.30
E IN.	0.100	0.110
MM	2.54	2.79
F IN.	0.050BSC	
MM	1.27	
G IN.	0.460	0.480
MM	11.68	12.19
H IN.	0.008	0.012
MM	0.20	0.30
J IN.	0.016TYP	
MM	0.41	

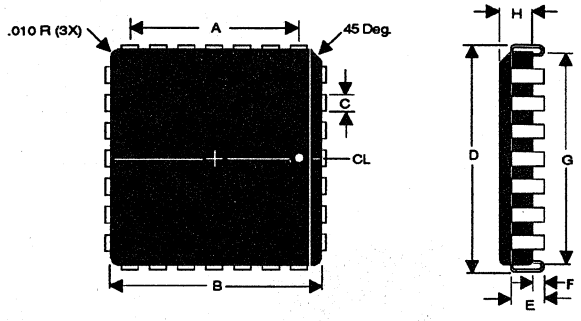
QUAD FLAT PACK
80-Pin (14.0 mm x 20.0 mm)





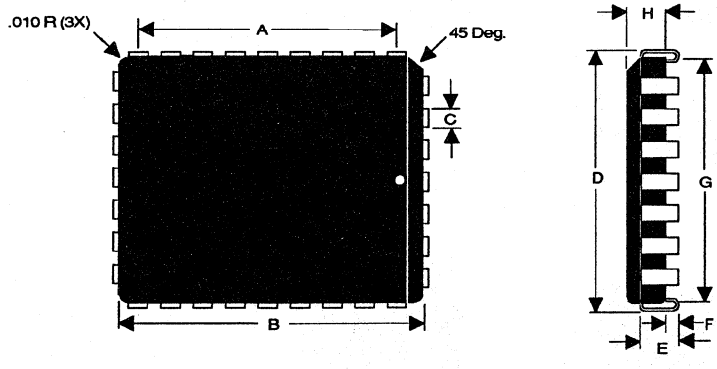
DIM	MIN	MAX
A IN.	0.115	0.124
MM	2.91	3.15
B IN.	0.010	0.020
MM	0.25	0.45
C IN.	0.031	---
MM	0.80	---
D IN.	0.781	0.793
MM	19.85	20.15
E IN.	0.545	0.557
MM	13.85	14.15
F IN.	0.685	0.717
MM	17.40	18.20
G IN.	0.921	0.953
MM	23.40	24.20
H IN.	0.016	0.051
MM	0.40	1.30
I DEG.	0	10

PLASTIC LEADED CHIP CARRIERS
28- and 44-Pin



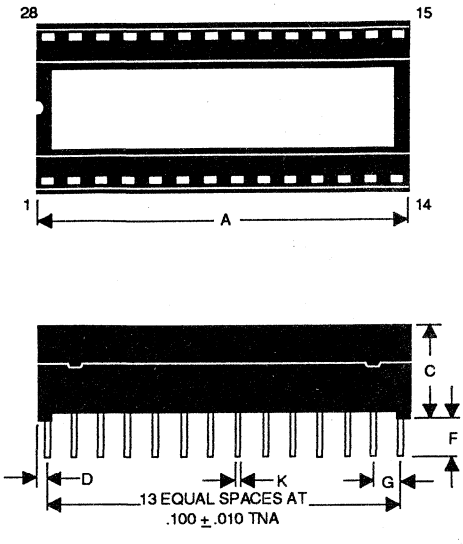
PKG	28-PIN		44-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.300 REF		0.500 REF	
MM	7.62		12.7	
B IN.	0.442	0.462	0.642	0.662
MM	17.68	11.73	16.31	16.81
C IN.	0.010	0.015	0.010	0.015
MM	0.25	0.31	0.25	0.31
D IN.	0.480	0.500	0.680	0.700
MM	12.2	12.7	17.27	17.78
E IN.	0.096	0.106	0.096	0.106
MM	2.44	2.69	2.44	2.69
F IN.	0.015	0.025	0.015	0.025
MM	0.38	0.64	0.38	0.64
G IN.	0.390	0.430	0.590	0.630
MM	9.91	10.92	14.99	16.00
H IN.	0.142	0.162	0.142	0.162
MM	3.61	4.11	3.61	4.11

PLASTIC LEADED CHIP CARRIERS
32-Pin



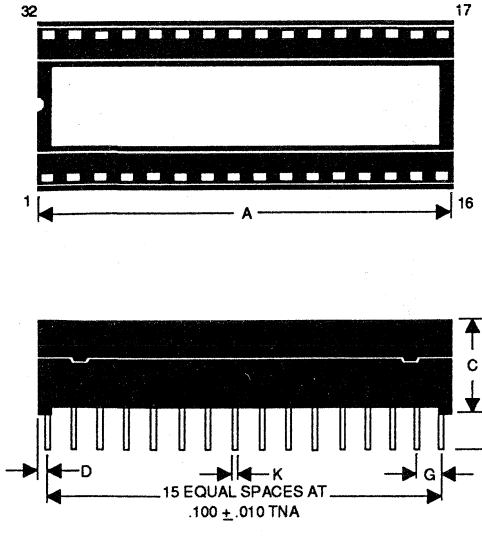
DIM	MIN	MAX
A IN.	0.390	0.410
MM	9.91	10.41
B IN.	0.580	0.600
MM	14.73	15.24
C IN.	0.010	0.015
MM	0.25	0.38
D IN.	0.480	0.500
MM	12.19	12.70
E IN.	0.075	0.095
MM	1.91	2.41
F IN.	0.015	0.025
MM	0.38	0.64
G IN.	0.450	0.470
MM	11.43	11.94
H IN.	0.105	0.115
MM	2.67	2.92

INTELLIGENT SOCKET
28-Pin (For 600 mil DIP)



DIM	MIN	MAX
A IN.	1.380	1.420
MM	35.05	36.07
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.390
MM	8.89	9.91
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.025	0.035
MM	0.64	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.97	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

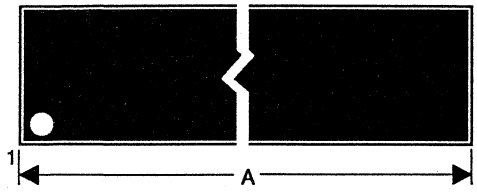
INTELLIGENT SOCKET
32-Pin (For 600 mil DIP)

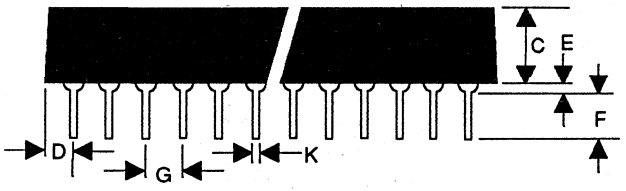


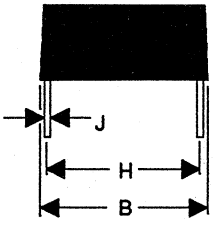
DIM	MIN	MAX
A IN.	1.580	1.620
MM	40.13	41.15
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.410
MM	8.89	10.4
D IN.	0.035	0.065
MM	0.89	1.65
E IN.	0.025	0.035
MM	0.64	0.89
F IN.	0.120	0.160
MM	3.04	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.97	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

ENCAPSULATED PACKAGES

16- and 24-Pin Flush Bottom
400 mil Body Width (dimension "B")





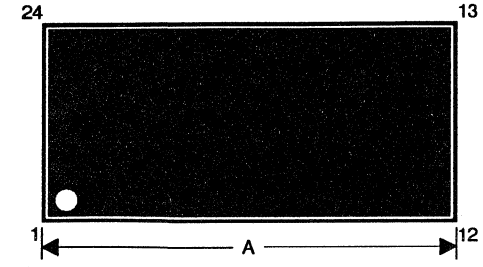


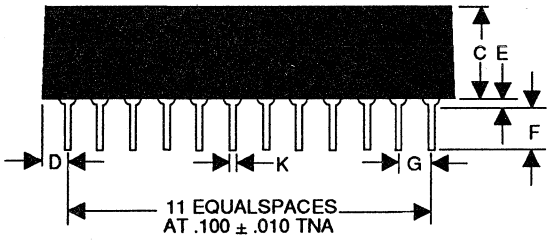
PKG	16-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.840	0.860	1.236	1.330
MM	21.36	21.84	31.40	33.78
B IN.	0.440	0.460	0.440	0.460
MM	11.18	11.68	11.18	11.68
C IN.	0.330	0.370	0.330	0.370
MM	8.38	9.40	8.38	9.40
D IN.	0.290	0.310	0.290	0.310
MM	7.37	7.87	7.37	7.87
E IN.	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02
F IN.	0.115	0.135	0.115	0.135
MM	2.92	3.43	2.92	3.43
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.320	0.370	0.320	0.370
MM	8.13	9.39	8.13	9.39
J IN.	0.008	0.012	0.008	0.012
MM	0.20	0.31	0.20	0.31
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53

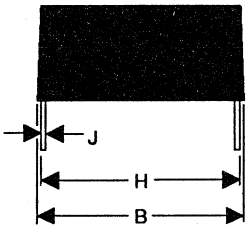
Packages designated for:
DS1290
DS1291

ENCAPSULATED PACKAGES

24-Pin Flush Bottom
700 mil Body Width (dimension "B")





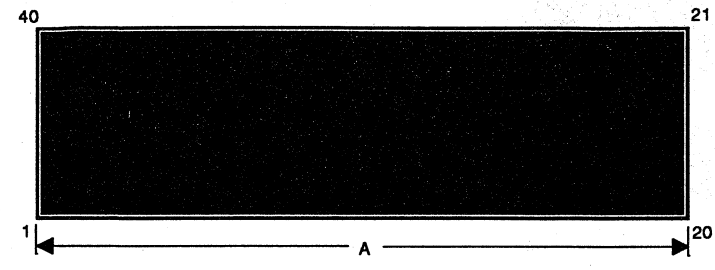


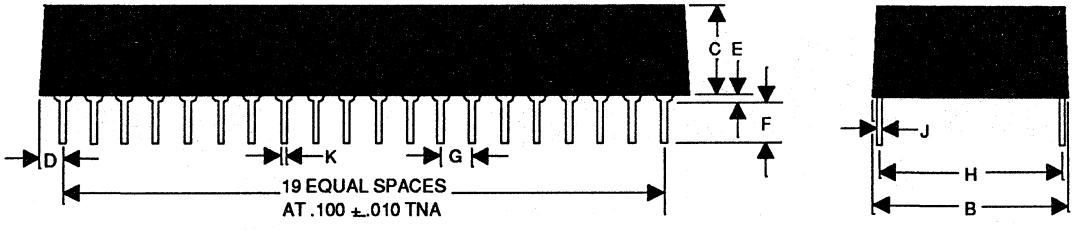
DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.680	0.700
MM	17.27	17.78
C IN.	0.345	0.360
MM	8.76	9.14
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.035
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.600	0.630
MM	15.24	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

Package designated for:
DS1187
DS1287
DS1287A

ENCAPSULATED PACKAGES

40-Pin Flush Bottom
700 mil Body Width (dimension "B")



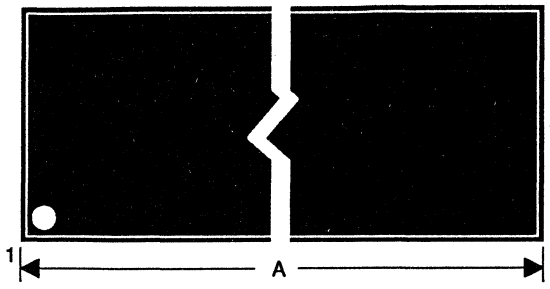


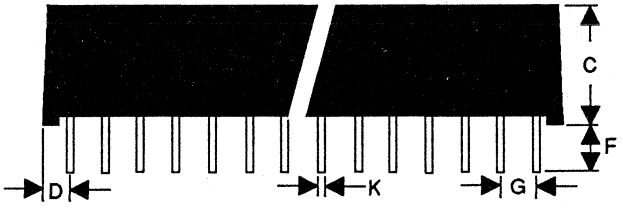
DIM	MIN	MAX
A IN.	2.080	2.100
MM	52.83	53.34
B IN.	0.680	0.700
MM	17.27	17.78
C IN.	0.340	0.360
MM	8.64	9.14
D IN.	0.090	0.110
MM	2.29	2.79
E IN.	0.040	0.060
MM	1.02	1.52
F IN.	0.165	0.185
MM	4.19	4.70
G IN.	0.016	0.020
MM	0.41	0.51
H IN.	0.590	0.610
MM	14.10	15.50
I IN.	0.009	0.012
MM	0.23	0.31

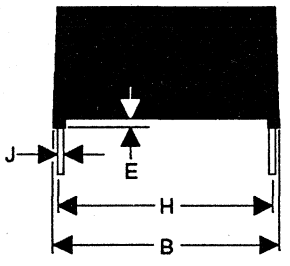
Packages designated for:
DS5000
DS5000T

ENCAPSULATED PACKAGES

24- and 28-Pin Extended Bottom
720 mil Body Width (dimension "B")





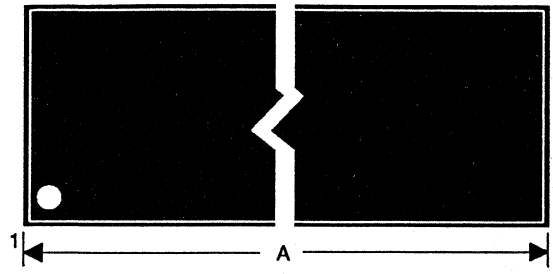


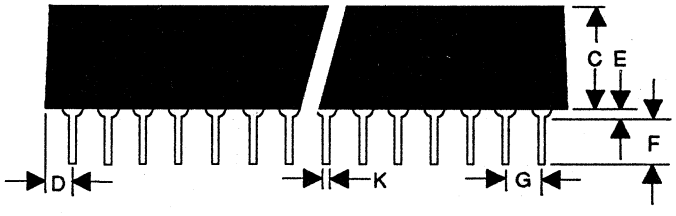
PKG	24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	1.320	1.340	1.520	1.540
MM	33.53	34.04	38.61	39.12
B IN.	0.695	0.720	0.695	0.720
MM	17.65	18.29	17.65	18.29
C IN.	0.395	0.415	0.395	0.415
MM	10.03	10.54	10.03	10.54
D IN.	0.090	0.120	0.090	0.120
MM	2.29	3.05	2.29	3.05
E IN.	0.017	0.030	0.017	0.030
MM	0.43	0.76	0.43	0.76
F IN.	0.120	0.160	0.120	0.160
MM	3.05	4.06	3.05	4.06
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.600	0.640	0.600	0.640
MM	15.24	16.26	15.24	16.26
J IN.	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.053

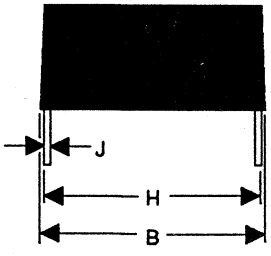
Packages designated for:
DS1220Y
DS1225AB/AD
DS1235Y
DS1243Y

ENCAPSULATED PACKAGES

24- and 28-Pin Flush Bottom
740 mil Body Width (dimension "B")





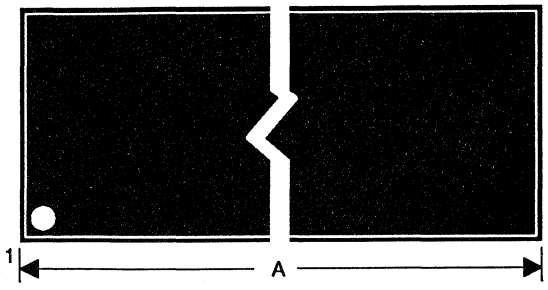


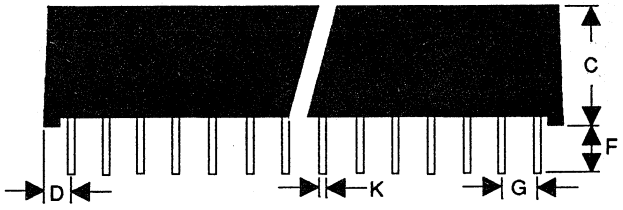
PKG	24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	1.320	1.335	1.520	1.540
MM	33.53	33.11	38.61	39.12
B IN.	0.720	0.740	0.720	0.740
MM	18.29	18.80	18.29	18.80
C IN.	0.345	0.360	0.340	0.360
MM	8.76	9.14	8.64	9.14
D IN.	0.100	.130	0.100	.120
MM	2.54	3.30	2.54	3.05
E IN.	0.015	0.035	0.015	.035
MM	0.38	0.89	0.38	0.89
F IN.	0.110	0.140	0.110	0.140
MM	2.79	3.56	2.79	3.56
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.600	0.630	0.600	0.630
MM	15.24	16.00	15.24	16.00
J IN.	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53

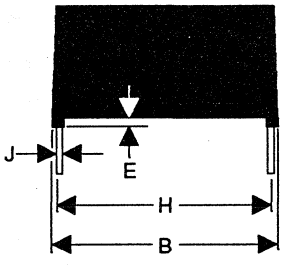
Packages designated for:
DS1286
DS1387
DS1397

ENCAPSULATED PACKAGES

28- and 32-Pin Extended Bottom
740 Mil Body Width (Dimension "B")







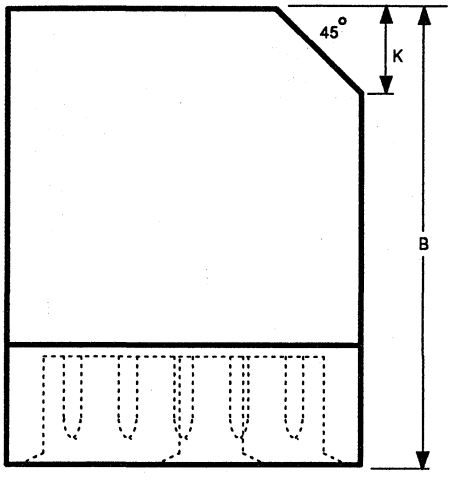
PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	1.520	1.540	1.720	1.740
MM	38.61	39.12	43.69	44.20
B IN.	0.720	0.740	0.720	0.740
MM	18.29	18.80	18.29	18.80
C IN.	0.395	0.415	0.395	.415
MM	10.03	10.54	10.03	10.54
D IN.	0.090	0.120	0.090	0.120
MM	2.29	3.05	2.29	3.05
E IN.	0.020	0.030	0.020	0.030
MM	0.51	0.76	0.51	0.76
F IN.	0.120	0.160	0.120	0.160
MM	3.05	4.06	3.05	4.06
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN.	0.600	0.640	0.600	0.640
MM	15.24	16.26	15.24	16.26
J IN.	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	.053

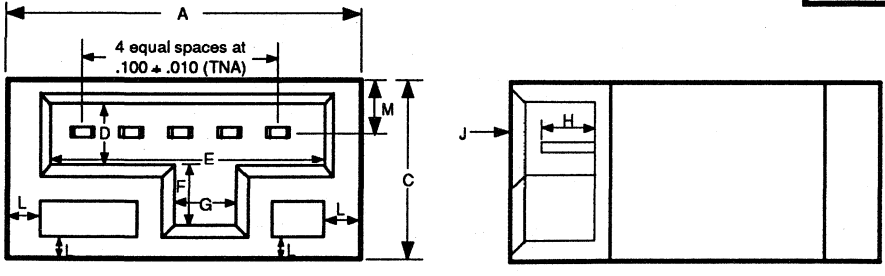
Packages designated for:
DS1230Y/AB
DS1245Y

ELECTRONIC KEY/TAG

Designated for:

DS1201
DS1204
DS1207



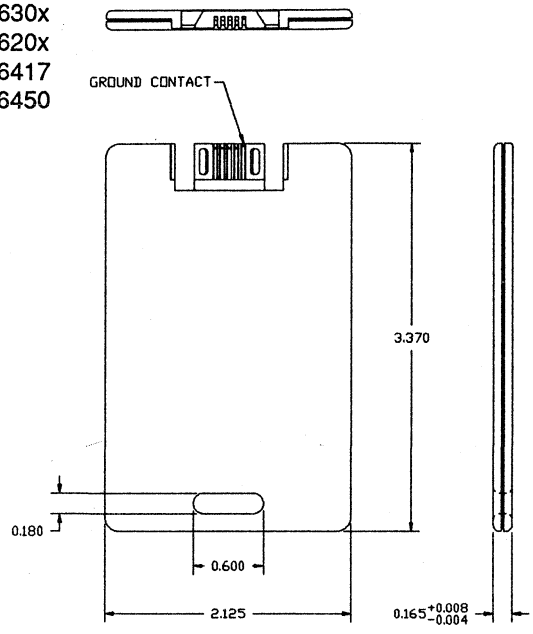


DIM	MIN	MAX
A IN.	0.610	0.630
MM	15.50	16.00
B IN.	0.740	0.760
MM	18.80	19.30
C IN.	0.310	0.330
MM	7.87	8.38
D IN.	0.100	0.110
MM	2.54	2.79
E IN.	0.515	0.525
MM	13.08	13.34
F IN.	0.100	0.110
MM	2.54	2.79
G IN.	0.100	0.110
MM	2.54	2.79
H IN.	0.100	0.130
MM	2.54	3.30
J IN.	0.030	0.060
MM	0.76	1.52
K IN.	0.045	0.055
MM	1.14	1.40
L IN.	0.045	0.055
MM	1.14	1.40
M IN.	0.100	0.110
MM	2.54	3.30

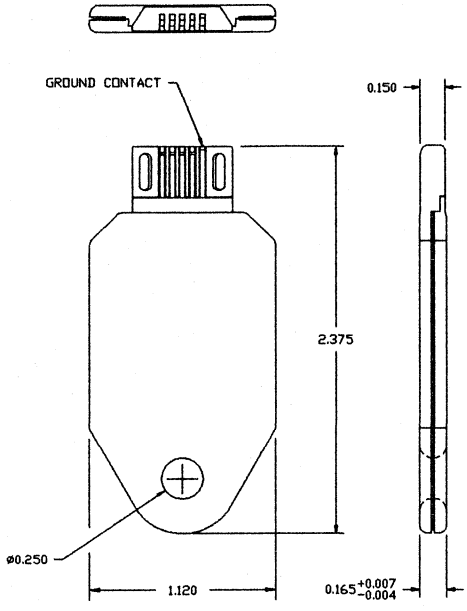
CYBERKEY/CYBERCARD

Package designated for:

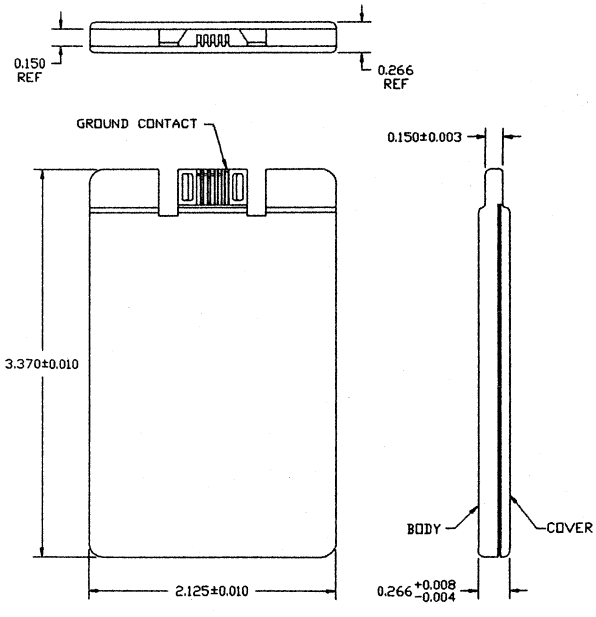
DS630x
DS620x
DS6417
DS6450



DS630x



DS620x



DS6417/DS6450

DALLAS
SEMICONDUCTOR

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